White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements

Industry Council on ESD Target Levels

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Abstract

CDM has become the primary real-world ESD event metric describing ESD charging and rapid discharge events in automated handling, manufacturing, and assembly of IC devices. Its importance has dramatically increased over the years as package feature sizes, capacitance, and pin count have scaled upward. In years past, arbitrary CDM protection levels had been specified as IC qualification goals with little background information available on actual/realistic CDM event levels and the protection methods available in manufacturing controls and device design for the safe production of IC components. The rapid advancement of IC technology scaling, coupled with the increased demand for high-speed circuit performance, made it increasingly difficult to guarantee a customer-specified "500 volts" CDM specification and as this update will discuss, even 250 volts can create challenges. At the same time, the required static control methods available for production area CDM protection at each process step have not been fully outlined. Therefore, a realistic CDM specification target must be defined in terms of available and commonly practiced CDM control methods and must reflect current ESD design constraints. Additionally, as technology scaling continues, very high-speed I/Os are being introduced which demand the need for lower CDM target levels in order to achieve the needed I/O performance. This is the scope of this latest update to White Paper 2.

By balancing improved static ESD controls specific to CDM, and limited ESD design capability in today's leading technologies, we recommend a CDM specification target level of 250 volts with consideration for lower CDM target levels in unique cases where very high-speed I/O performance is needed. These target levels are a realistic and safe CDM level for manufacturing and handling today's products using basic CDM control methods, or advanced CDM control techniques as needed based on the target level.

At the same time, we show that the current trend of silicon technology scaling will continue to place further restrictions on achievable CDM levels. It is, therefore, necessary that the Industry Council presents a realistic CDM roadmap for consideration by the industry moving forward to 7 nm technologies and beyond, including 2.5D and 3D technologies.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements on IC products for safe handling and mounting in ESD protected areas while addressing the constraints from silicon technology scaling and IC design. The Council now consists of representatives from active full member companies and numerous associate members from various support companies.

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Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for the future ESD target levels. The Council Members and Associates will promote these recommended targets for adoption as company goals. Being an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Preface

This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD CDM level requirements. We will show through this document why a more realistic definition of the ESD CDM target levels for components is not only essential but is also urgent. The document is organized in different chapters with additional information in the appendices to give as many technical details as possible to support the purpose given in the abstract. We begin the paper with an Executive Summary and chapter/appendix highlights followed by frequently asked questions (FAQ) so that the reader can readily find critical information without having to scan through the whole document. Additionally, these FAQs are intended to avoid any misconceptions that commonly occur while interpreting the data and the conclusions herein. All component-level ESD testing specified within this document adheres to the methods defined in the appropriate ANSI/ESDA/JEDEC or JEITA specifications.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies and contract manufacturers. The data represents CDM and field failure information collected from a large variety and volume of IC products; no specific components are identified. The readers should not construe this information as evidence for unrelated field failures resulting from electrical overstress events or system-level ESD incidents. The document only refers to component-level ESD recommendations which should have no impact on system-level ESD requirements.

The Industry Council, while providing these recommendations, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Glossary of Terms

AEC	Automotive Electronics Council
BGA	ball grid array
CBE	charged board event
CBM	charged board model
CCD	charged coupled device
CC-TLP	capacitively-coupled transmission line pulse
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
CPM	charge plate monitor
DC	direct current
DDR	double data rate
DIP	dual-in-line package
DPM	defects per million
DRAM	dynamic random-access memory
DSP	digital signal processor
DUT	device under test
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EOS	electrical overstress
EPA	ESD protected area
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association
ESDS	electrostatic discharge sensitive
ESVM	electrostatic voltmeter
FA	failure analysis
FAR	failure analysis report
FAQ	frequently asked question
FCDM (FICDM)	field-induced charged device model
FIM	field-induced model
FinFET	Fin field-effect transistor
FWHM	full width at half maximum
GND	ground, negative voltage supply
GPIO	general purpose I/O
GSA	Global Semiconductor Alliance
HBM	human body model
HDMI	high-definition multimedia interface
HSS (HSSL)	high-speed serial link
IC	integrated circuit
ICT	in-circuit test
IP	intellectual property
I/O	input/output
IEC	International Electrotechnical Commission
JEDEC	JEDEC Solid State Technology Association
JEITA	Japan Electronics and Information Technology Industries Association
LGA	land grid array
LICCDM	low-impedance contact charged device model

LNA	low noise amplifier
LV	low voltage
MCM	multichip module
MIPI	mobile industry processor interface
MM	machine model
MV	medium voltage
NFET	N-type field-effect transistor
NMOS	N-channel metal-oxide-semiconductor
NPN	negative-positive-negative (transistor)
PAM	pulse-amplitude modulation
PCB	printed circuit board
PCTA	process capability and transition analysis
PFET	P-type field-effect transistor
PMOS	P-channel metal-oxide-semiconductor
QFP	quad flat pack
RC	resistor-capacitor network
RLC (LRC)	resistor-inductor-capacitor network
RLDRAM	reduced latency DRAM
RF	radio frequency
SATA	serial advanced technology attachment
SBLK	silicide blocked
SCR	silicon-controlled rectifier
SDM	socketed device model
SERDES	serializer/deserializer transceiver that converts parallel data to serial data
SMT	surface mount technology
SoC	system-on-chip
TIVA	thermally induced voltage alteration
TLP	transmission line pulse
TQFP	thin quad flat pack
USB	universal serial bus
ULSI	ultra-large-scale integration
VDD	positive voltage supply
Vds	drain/source voltage
VF-TLP	very fast transmission line pulse
VSS	negative voltage supply
WCDM	wafer-level charged-device model
WSP	wafer-scale package
ZIF	zero insertion force

ESD Design Window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent technology node.

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional.

I_{t2}: The current point where a transistor enters its second breakdown region under ESD pulse conditions, and it is irreversibly damaged.

Node: Within a circuit, a point of interconnection between two or more components.

Executive Summary

It is well understood in the IC industry that the charged device model (CDM) is the ESD model that best describes real-world component-level ESD events during IC manufacturing and handling. See Chapter 1 for details. In contrast to HBM, where basic ESD control measures in manufacturing ensure a safe and realistic specification level (i.e. 1000 volts HBM as reported in White Paper I [1]), CDM protection requires these basic ESD controls as well as additional ESD controls such as managing against the charging of insulators, at specific process steps, to ensure safe and realistic levels for all product designs below 200 volts. Some of these additional process assessment techniques that may need to be involved are detailed out in a recently released standard practice from the ESDA entitled "Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques", ANSI/ESD SP17.1. As IC applications have moved towards ultra-high-speed I/O interfaces (> 200 Gb/s) over the last decade, this CDM threat has been further exacerbated in terms of qualification levels to achieve design performance. This has driven the need for advanced control methods to be implemented for safe manufacturing in the production area. Combined with these new developments the sensitivity and accuracy for CDM testing have become more critical than ever. This update to White Paper 2 addresses the current requirements for CDM presenting a holistic view of the CDM roadmap including both standard and advanced high-speed products.

Some important aspects of the CDM challenge must be understood:

IC Design / Development Constraints: Constraints from silicon technology scaling, IC high-speed circuit design requirements, and larger IC package size trends are impacting ESD protection capability, see Chapter 2 for details. These constraints can inhibit the ESD design methodology required to meet the customer-specified 500 or 250 volt CDM levels. This is especially true for very high-speed high-performance pin design types, which have limitations in CDM discharge peak current. As a result, practical designs are restricted to 2-6 amperes of peak CDM current, which translates to a CDM target level of 125-400 volts for many advanced technology products (depending on pin-count). In the same vein, ultra-high-speed designs > 200 Gb/s in the sub-10 nm technologies can be constrained by even tighter CDM peak currents in the range of 2 to 3 amperes for non-RF I/O.

Evolution of Perceived CDM Requirements: 500 volts can no longer be routinely met for the reasons discussed above, often leading to delays in qualification and time-to-market. The more important focus should be that the designs can no longer support these previous levels and that with the available CDM control methods there is no need for higher CDM levels ($\geq$ 500 volts) that make the designs nearly impossible to meet circuit performance. In addition, even if only a small portion of the IC products are designed to be in the market with a high-speed interface, these high-speed interfaces now require consideration for even lower CDM targets compared to most products without these interfaces. Estimates from the ESD Association's Technology Roadmap [2] do show an expected increase in the number of products that are predicted to have CDM levels below 125 volts by 2025 as shown in Figure 1.

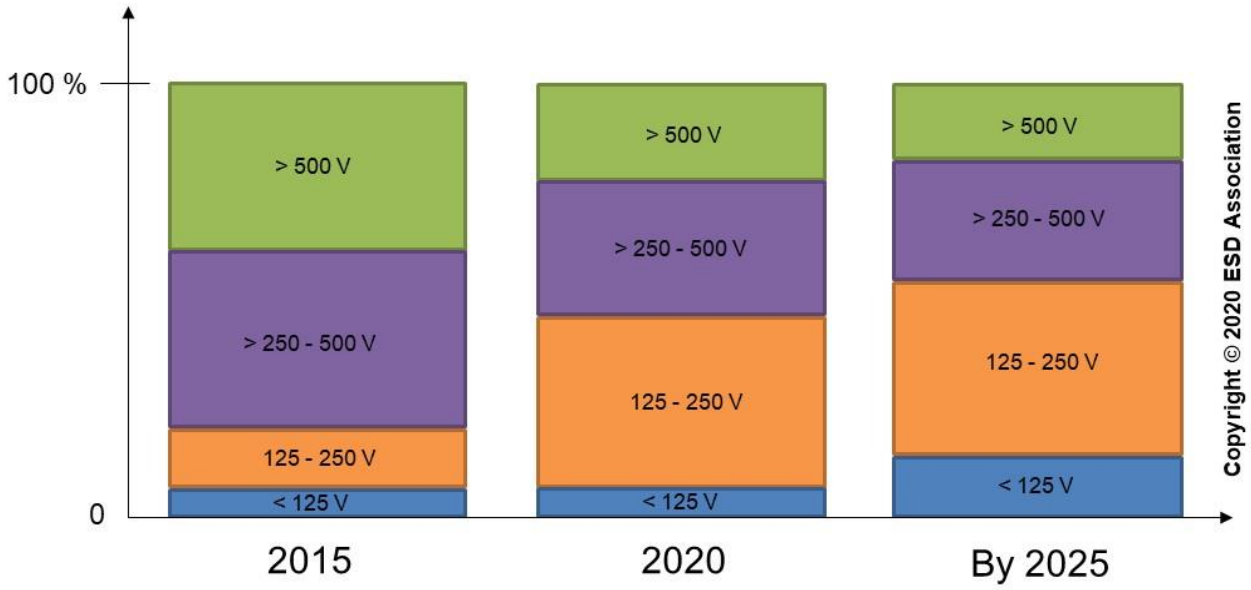

Figure 1: Forward-Looking Charged Device Model Sensitivity Distribution Groups

Improved state-of-the-art CDM ESD control methods in practice in the industry today. Basic controls allow safe handling for devices with CDM pass voltage levels as low as 200 volts and with process assessment techniques as discussed in Chapter 3 and further in ANSI/ESD SP17.1 enabling lower levels. This work has revealed several important findings that need to be considered.

A. Field return data from 11 billion IC devices show that customer returns can occur for products with CDM pass levels from 200 volts to 2000 volts, meaning control of CDM at production sites is more important than a specific performance target level. See Chapter 4.
B. Field failures also can occur when proper CDM control is not established during a product ramp-up (pre-qualification), meaning that production failures must be addressed by correcting the CDM control methods at critical process steps rather than requiring the designs to pass at higher voltages than are achievable by design. See Chapter 3.
C. CDM control measures are available throughout the industry to meet safe manufacturing and handling of products at 200 volts or above, meaning that products designed for CDM levels at 250 volts or 500 volts can be equally safe and reliable. Process assessment techniques as discussed in Chapter 3 and further in ANSI/ESD SP17.1 can be used to address even lower CDM target levels.
D. Thus, any product with a CDM passing level of 250 volts or higher can be handled safely and reliably in a facility with basic CDM control measures. This level of protection should result in minimal impact on design and IC circuit performance requirements and make them compatible with current technology trends. See Chapter 5.
E. As future IC technologies are enabled, there should be a continuous improvement of CDM control with even more advanced methods coming into practice.
F. Recently, a standard practice document ANSI/ESD SP17.1 [3] was developed by the ESD Association introducing advanced process assessment techniques valuable for assessing risks below 200V and which can be utilized for dealing with CDM at or below 125 volts. See Chapter 3.

Recommended CDM Levels: Based on this extensive study, a safe and practical CDM passing level of 250 volts is recommended as outlined in Table I below. Products with a CDM target level lower than 250 volts should implement additional process-specific measures for CDM control, especially during product ramp-up. For products in this category, process-specific techniques, as described in ANSI/ESD SP17.1, are mandatory.

Table I: Recommended CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to ANSI/ESDA/JEDEC JS-002)	ESD Control Requirements
$V_{CDM} \geq 200$ V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators according to standards like ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625
$V_{CDM} < 200$ V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators **+** • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads) **+** • **Charging/discharging measurements at critical process steps following ANSI/ESD SP17.1**

Updated Roadmap for continued silicon technology scaling. With more recent developments requiring ultra-high-speed interface designs in technologies of sub-10 nm, the CDM Roadmap has been revised as shown in Figure 2. This was driven by targets for 5 nm SoCs and beyond for operations @ 56 GHz (Nyquist) or 224 Gb/s PAM4. As designs are now limited to 75 fF of ESD loading capacitance, a target level of 125 volts has become necessary (as indicated by the red bar in the figure) for this ultra-high-speed interface. Package sizes for large ICs, such as microprocessors, at these performance levels, dictate the CDM peak discharge current. To recognize this constraint, the Industry Council is also recommending that the max target peak current of associated 224 Gb/s PAM4 high-speed IP blocks be 2.5 amperes. Advanced process assessment techniques as specified in ANSI/ESD SP17.1 can enable a path to safe manufacturing at these lower target levels. At the same time, lower performance I/Os such as standard GPIO interfaces should still be targeted at 250 volts leveraging basic control methods as described in ANSI/ESD S20.20 [4], IEC 61340-5-1 [5], and JEDEC JESD625 [6] this will help minimize the manufacturing risks on products that may have a high-performance I/O. This is explicitly shown in the figure at the 7 to 5 nm node with the green bar at 250 volts in the figure for standard I/Os, and the red bar at 125 volts for ultra-high-speed 224 Gb/s PAM4 I/O interfaces. The choice of qualification thus depends on the I/O applications.

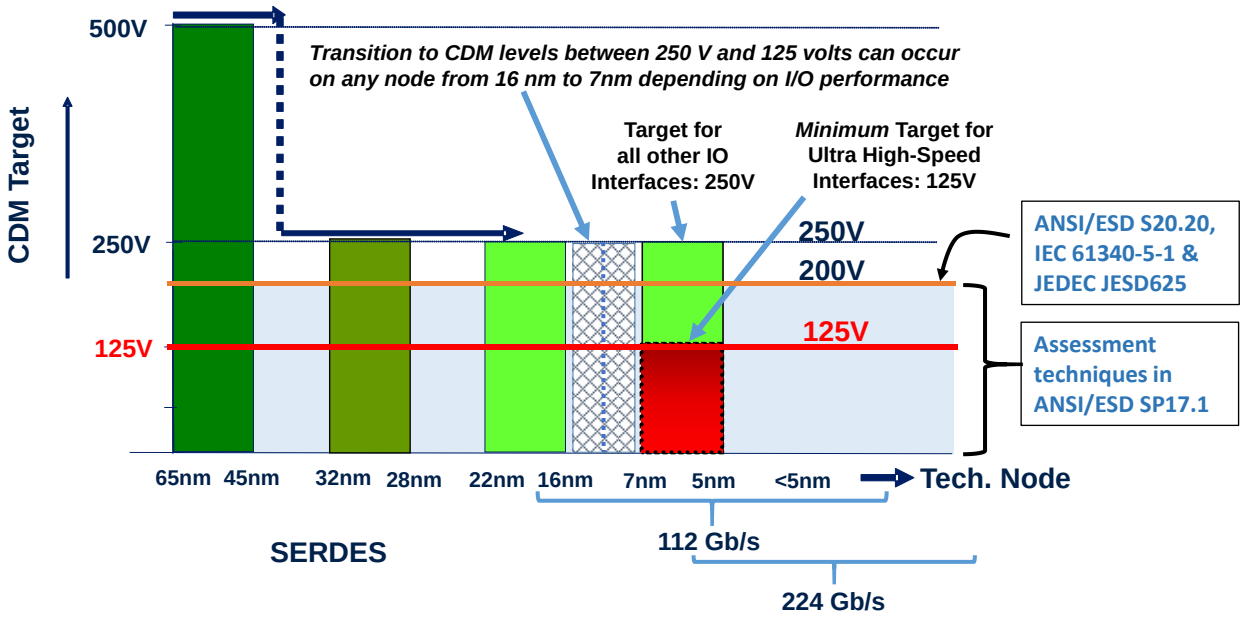

Figure 2: Technology scaling effects on practical CDM levels and the associated CDM control requirements

As I/O performance levels increase above 56 Gb/s PAM4, a reduction in the maximum peak current design target will be needed for CDM due to reductions in the ESD design window based on technology, package size, and I/O performance. This means that even 250 volts may not be achievable and still meet performance requirements. However, care should be taken on the design side to ensure that if a target level of 250 volts cannot be met as a function of the ESD window, package size, and performance reasons, as discussed in Chapter 2, that the achievable target level is *maximized* to reduce manufacturing risks. The designed target level for the product must also be in line with the manufacturing capability. Simply reducing the target level directly to 125 volts may not be prudent for the manufacturing capability. It should be noted that as CDM target levels drop below 200 volts, data, as shown in Chapter 4 is limited, and proper manufacturing ESD controls may not have been implemented yet. Care should also be taken to ensure that proper ESD controls are in place and that the proper process assessments have been made in the manufacturing flow as per ANSI/ESD SP17.1 for whatever CDM target level is achievable. This will ensure the manufacturing environment can manage the risks with component target levels moving towards 125 volts.

3D IC CDM Targets: As described in the GSA roadmap [7] for 3D ICs, in 2.5D and 3D packaging processes, with die stacking some micro-bumps are not connected to the external package ball, but can experience ESD exposure during a few process steps of the manufacturing process. In these packaging technologies, the number of micro-bumps can range from hundreds up to tens of thousands, a CDM target I_{PEAK} range from 100 milliamps to 1 ampere is discussed for qualification. Careful consideration of ESD controls in a few critical process steps will guarantee the safe handling of these micro-bumps in manufacturing. The qualification can be done by assessing these internal bumps with very fast TLP (VF-TLP) or wafer-level CC-TLP equipment.

External/Internal High-Speed I/Os: Externally exposed high-speed I/Os require extra ESD control precautions in the handling, manufacturing, assembly, testing, and system installation phases. At the same time, internal I/O are not immune to ESD risks. Appendix A explains how the

risk of CDM events is limited with a product's internal I/O but can exist especially during printed circuit board (PCB) and system assembly if ESD control precautions are not fully implemented, while external I/O have extra precautions that may need to be taken to ensure these I/O are safe in real-world environments.

CDM Qualification of Interface IP: Determining whether an IP, when integrated into the product, is expected to pass the product's classification level is uncertain at best for the end-user. This is because the standard CDM qualification of an IP interface to a voltage class is not practical as products are qualified for a given package type or package size. For this purpose, a qualification method for IP based on a CDM peak current as a qualification parameter is suggested as guidance in Appendix B.

Test Methods for Sensitive CDM Targets: As the CDM target levels are reduced to below 250 volts, proper test methods and accuracy of the test will become critical. See Appendix C. Various techniques are being investigated to improve the present air discharge test method for its fidelity. At the same time, there is a much more serious effort to introduce contact-based testers for better reliability at lower CDM test voltages. It is likely a standard will be developed allowing for both air discharge and contact-based testers to be used alternatively. Currently, a method for contact based CDM testing called low-impedance contact CDM has been released as a standard practice [8]. These critical developments are concurrently taking place as CDM targets below 250 volts and as low as 125 volts are recommended.

Final Words: This revision of White Paper 2 addresses the critical need for CDM targets for ultra-high-speed I/O interfaces operating at data rates > 200 Gb/s and establishes that a safe level of 125 volts CDM can be recommended. At very high-speed I/O interface data rates > 56 Gb/s, a combination of factors, including the ESD design window for the technology, package size, and I/O performance can drive a reduction in the designed peak current target, meaning 250 volts may not be achievable, but design efforts should focus on maximizing the achievable peak current level to minimize manufacturing risk. Various process assessment techniques (as described in ANSI/ESD SP17.1) are necessary to address the added risks in manufacturing below 200 volts. It is important to emphasize again that all products with standard, lower performance I/Os, should still target 250 volts with manufacturing using known basic control methods such as described in ANSI/ESD S20.20, IEC 61340-5-1, and JEDEC JESD625. Better I_{PEAK} control for accuracy at lower voltages in the CDM standard test methods to validate these CDM target levels is in progress. Although not previously considered for any packaged product, interface IP qualification needs to be addressed and this can be achieved by using a recommended standard for peak current as the target. Finally, it is also recognized that exposed high-speed interface I/Os in a system need special ESD protection requirements, whether they are considered external to the system or not.

References

[1] White Paper 1: "A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," June 2018, http://www.esdindustrycouncil.org/ic/en/documents

[2] ESD Technology Roadmap from the ESD Association, https://www.esda.org/standards/

[3] ANSI/ESD SP17.1-2020 "For the Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques", 2020 http://www.esda.org/standards/esda-documents.

[4] ANSI/ESD S20.20-2014, “Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment”, July 2014 http://www.esda.org/standards/esda-documents.

[5] IEC 61340-5-1:2016, “Protection of Electronic Devices from Electrostatic Phenomena – General Requirements”, May 2016 http://webstore.iec.ch

[6] JEDEC JESD625B “Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices”, January 2012 http://www.jedec.org.

[7] Global Semiconductor Alliance, “Electrostatic Discharge (ESD) in 3D-IC Packages”, Version 1.0, January 2015 http://www.gsaglobal.org/working-groups/3d-ic-packaging/.

[8] ANSI/ESD, SP5.3.3-2018. “Low Impedance Contact CDM as an Alternative CDM Characterization Method”, February 2019.

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Chapter Summary

Chapter 1: History of charged device model since the initial 1974 publication is reviewed and major developments, mostly concerning CDM testers, are noted chronologically. No significant changes have been made since the 2010 release, minor updates, and realignment only.

Chapter 2: This chapter outlines the protection design limitations associated with silicon technology scaling and the demand for high-speed circuit performance. These protection design limitations become more pronounced with the trend for larger area, high pin count packages. With these constraints in view, the chapter points out the realistic CDM target levels that can be achieved in design today. These limits are recommended for two different applications: general I/O applications versus high-speed applications. Significant changes have been made to this chapter since the 2010 release, many figures have been updated with recent trends and Section 2.9 added.

Chapter 3: The chapter describes two similar methods to analyze an assembly area for CDM risk and explains how to use these methods in actual production lines with examples. The field problems presented also show that if such a CDM risk analysis is not performed, even devices considered CDM robust may fail during assembly or testing since the board can get charged and discharges with a higher discharge current than a single device at the same voltage level. A risk analysis performed following the described methodologies enables the manufacturer to handle even very CDM sensitive devices. Significant changes have been made since the 2010 release with the overall chapter updated to introduce techniques discussed in ANSI/ESD SP17.1 and new examples added.

Chapter 4: The field return data of 11 billion shipped parts consolidated from numerous IC manufacturers are analyzed. The device types range from discretes to ULSI system-on-chip parts. Primarily field returns from the board manufacturers and end-customers have been considered. There is a weak dependence on the combined EOS and ESD failure return rate on the CDM qualification level. In a data subset of 1.5 billion parts, it is demonstrated that EOS-related fails (not CDM-related fails) are dominating the failure statistics. Typical examples confirm that CDM-related returns are usually caused by problems in the ramp-up phase of a manufacturing process. Minor yet critical changes in the ESD control of the manufacturing process solve these problems immediately as shown in Chapter 3. No significant changes have been made since the 2010 release, minor updates, and realignment only.

Chapter 5: This chapter presents a total perspective on CDM control techniques available for production areas and based on this, recommends a realistic yet safe categorization of target levels that are linked to the required degree of CDM control methods. Considering all aspects from design capability to field reliability and combined with the currently practiced CDM control methods, it is proposed that a CDM level of 250 volts is a safe qualification level for the vast majority of integrated circuits in manufacture today. ICs with ultra-high-speed interface pins (> 200 Gb/s) require a qualification level of 125 volts due to design constraints. As the electronics industry progresses to even higher performance products and technologies it is expected that the proportion of products requiring CDM levels below 250 volts will increase. Consequently, continuously improved and monitored CDM control at the production areas must become a routine practice. Significant changes made since the 2010 release, updating and adding many sections as well as outlook and roadmap to align with today's technology trends for high-speed IOs.

Appendix Summary

Appendix A: This appendix discusses how to classify high-speed I/Os as internal or external based on the accessibility during various processing and handling phases. This helps to estimate what type of I/Os have a higher probability to be exposed to ESD stress during processing, installation, and use. This is a new appendix introduced with this release of the white paper.

Appendix B: This appendix addresses how the specific nature of CDM demands a dedicated methodology to assess the CDM robustness of sub-circuits, like interface IP, and describes a proposal for an appropriate CDM qualification method for these IPs. In order to enable a valid assessment of the CDM robustness that holds equally for both test chip and product, the CDM discharge peak current is proposed as a measure of the CDM robustness, instead of the voltage. This is a new appendix introduced with this release of the white paper.

Appendix C: This appendix describes existing CDM ESD test methods and standards and summarizes the differences between them. The challenges of air discharge testing are discussed, especially for low voltage testing. New test methods, which show great promise for extending reliable CDM testing to lower stress levels, are introduced. This is a significant rewrite of the appendix since the 2010 release to align with the state of CDM test standards today.

Appendix D: Simple circuit models can explain the major features of charged device model (CDM) non-socketed ESD testers as specified in the ANSI/ESDA/JEDEC JS-002-2018 CDM standard. A simple lumped series LRC model is estimated, and it explains features observable up to 1-2 GHz. This includes all major trends for peak current (I_{PEAK}), which is plotted in the plane of effective L and C for a given value of spark resistance R. Extensions of this basic circuit model to a distributed one explain many reported high-frequency CDM effects. No significant changes have been made since the 2010 release, minor updates, and realignment only.

Appendix E: A comparison between the CDM events in the real world and those in the tester world is presented along with descriptions of some typical cases. This appendix shows that the peak CDM discharge current from a high capacitance device in the real world is typically not as high as that in the tester world except on a power pin (bus). No significant changes have been made since the 2010 release, minor updates, and realignment only.

Appendix F: It is shown that no correlation of CDM to any other stress types (e.g. HBM, EOS, and CBE) can be expected. Therefore, CDM cannot be replaced by, nor replaces, any of the other stress types. Consequently, a reduction in CDM target levels should not lead to a lower performance for other stress types. No significant changes have been made since the 2010 release, minor updates, and realignment only.

Appendix G: This appendix outlines charged board events (CBE) that result in damage to IC devices placed on printed circuit boards. The various charge/discharge mechanisms are described. Charged board events are higher energy counterparts to CDM for IC components, but different IC failure mechanisms result which do not correlate to other ESD event methods. A literature review is given along with techniques to evaluate CBE on systems. Recommendations to reduce CBE impact include improved ESD control and circuit board design/implementation guidelines. No significant changes have been made since the 2010 release, minor updates, and realignment only.

Appendix H: A review of the current CDM goals for IC's from a manufacturer and customer view and the impacts that the current goals have on the manufacturer and end customer. The costs to the manufacturer of the current CDM target levels are highlighted in terms of design revision and time to market delay; the benefits of a new target level are similarly highlighted. This appendix was the previous Chapter 4 in the 2010 release (moved to Appendix H in this revision of the white paper) and has been updated with an updated roadmap and minor updates since the 2010 release.

Frequently Asked Questions

FAQ on CDM Qualification

Q1: Customers did not specify CDM levels before. Why are they asking for it now?

Answer: As the importance of HBM diminishes (even for units shipped below specification levels) as demonstrated by a lack of field returns, customers are focusing more on CDM-based field failure signatures, which are distinct from HBM.

Q2: If CDM methodology and levels are modified would there be more fallout for EOS at the component or System Level?

Answer: CDM and EOS failures are completely different in total energy and time duration. Effective CDM protection does not guarantee EOS protection. EOS protection must be provided at the system level. There is no correlation between component CDM failures and system EOS failures. The fallout rate due to EOS would not change as a result of modifying CDM methodology and levels.

Q3: As products with low CDM values have an increased risk for problems at introduction, shouldn't we aim for larger CDM levels?

Answer: Where a target level of 250 volts can be achieved in design without degrading electrical performance or incurring additional product cost, this level of CDM should continue to be implemented. However, Chapter 2 clearly shows that for several applications even 250 volts may not be feasible. Chapter 3 shows that solving the problems by CDM control measures is much more efficient than increasing the CDM robustness level at the cost of functional performance.

Q4: How is it determined that CDM levels lower than 500 volts are safe?

Answer: It has been proven that even 200 volt CDM can safely be manufactured if appropriate CDM control measures are taken (see Chapter 3). The assessment of ESD control measures and the field return data show that devices with 250 volts are equally as safe as 500-volt CDM parts in typical modern manufacturing sites.

Q5: When and where do classic CDM failures happen?

Answer: The classic CDM failure mechanism is a dielectric breakdown failure signature happening mainly in the ramp-up phase of a new product in the test area for a semiconductor manufacturer. This can also happen in PCB assembly lines or system assembly lines especially when new process steps are introduced.

Q6: If the specifications are meant for all pins on a package, would it not make more sense to require higher levels for the corner pins?

Answer: With the automated pick and place tools today, any of the pins could make first contact. All of the pins need to be considered, the corner pins should not be treated any differently.

Q7: The council made a case about lowering HBM levels. Will CDM levels follow automatically?

Answer: It has been shown that the HBM and CDM fail levels are largely uncorrelated. This is demonstrated in Appendix F, Section F.2. This is mainly due to the completely different physical discharge mechanisms and failure modes between the two models.

Q8: Should CDM qualification levels be uniform for different I/O interfaces?

Answer: Naturally one would assume that the CDM target would be independent of I/O interfaces. However, for high-speed applications above 56 Gb/s, target levels below 250 volts may be necessary depending on the package size, I/O performance, and technology but not necessarily stepping directly to 125 volts, as discussed in this document. Simply reducing the target level directly to 125 volts may not be prudent for the manufacturing capability. Care should be taken to ensure that proper ESD controls are in place and that the proper process assessments have been made in the manufacturing flow as per ANSI/ESD SP17.1 for whatever CDM target level is achievable. However, lower performance I/O interfaces than mentioned above should still be targeting 250 volts to minimize manufacturing risks.

Q9: Are the CDM target levels for all interfaces with a data rate above 56 Gb/s lowered?

Answer: The lowering of the CDM target levels is driven by the need of exploiting the high-speed performance per lane. Any interface where the speed per lane exceeds 56 Gb/s can apply a reduction below 250 volts. How far below 250 volts the target level needs to go is a function of how far the performance is pushed above 56 Gb/s. See Chapter 2.

FAQ on CDM Control

Q10: If the production areas have basic controls for ESD would these methods also provide the necessary protection for CDM?

Answer: If basic ESD controls as defined in ANSI/ESD S20.20 or equivalent are used, production areas should be able to handle CDM target levels of 250 volts – this has been proven out over the past 10+ years since the release of this white paper in 2009. As targets levels are reduced to levels below 200 volts CDM, care should be taken to minimize the number of pins being reduced to these lower levels as more advanced process assessment techniques such as those called out in ANSI/ESD SP17.1 may need to be employed to assess the risk in the production area. Not every production area is ready to handle target levels below 200 volts today.

Q11: Many products that have been shipped at CDM levels of 250 volts or even 125 volts seem to be safe. Is it fair to say that CDM is well controlled with the basic methods or do they need special care for the 125-250 volt range?

Answer: Basic ESD controls, including the control of insulators and E-fields, as called out in ANSI/ESD S20.20, IEC 61340-5-1, and JEDEC JESD625 should be able to handle 250-volt sensitive devices. Following the above controls and using assessment techniques as called out in ANSI/ESD SP17.1 can enable manufacturing to manage devices with sensitivity levels even in the 125-volt range.

Q12: What are the main weak points for CDM ESD control in manufacturing?

Answer: In contrast to controls for HBM, ESD controls for CDM rely on controlling the charge on insulators and controlling the discharge to the conductors of the manufactured devices. Chapter 3 gives more detailed information.

Q13: Defining a maximum current level as a CDM target seems to be a good solution for the challenges with the design of CDM ESD protection and also a good way to overcome the issues with variations in stress between different CDM testers and different CDM testing standards. However, how does a current level as the CDM target translate into a sensitivity level that is meaningful for the manufacturing environment?

Answer: While peak current makes sense from a device design point of view, the industry views sensitivity in terms of voltage. The experience both in the ESD control field and the qualification of devices is based on voltage values of the long-standing standards. Changing this to current would confuse both the end customer and contract manufacturers. The translation from the voltage level to current stays with the ESD protection designer. Knowing the product portfolio and typical packages, an estimate of the required withstand peak current can be made (see Chapter 2).

FAQ on CDM Requirements

Q14: Although your target level recommendations seem to be valid from your analysis and the collected data, our customers are not yet confident that our subcontractors have the measures to match the new requirements. How do we proceed?

Answer: By simply staying at the old levels, we will not address the design challenges which are discussed in Chapter 2. Additionally, the Industry Council believes that customer demands for improved I/O performance will only increase in the future, putting even more stress on the ability to achieve the current CDM target levels. Efforts to improve CDM protection in our manufacturing facilities must continue to be a focus area if we are to be prepared for these future challenges. As discussed in Chapter 3, basic CDM protection measures are implemented when the international standards are followed. The issue is that many are not aware of this as they do not perceive these measures as CDM protection measures. In addition to these basic CDM protection measures, an analysis of your production lines with the methods as described in Chapter 3 should be completed. This is especially true during the introduction of new process steps and during the production ramp-up phase as it has been found that CDM failures can occur for products with even higher CDM passing levels.

Q15: Chapter 1 covers highlights of CDM from the US and Europe but does not mention the Far East. Weren't there some significant developments in Japan in the same time frame?

Answer: Yes, there were significant developments, and the authoritative summary is given as part of this White Paper. The essentials are as follows:

1. The first CDM paper in Japan was presented at the Electronics and Communication Conference with the title "Proposal of Charged Package Method", which influenced EIAJ Test Method IC121, Technical notes in 1988. Related EOS/ESD Symposium presentations from Japan were given in 1986, 1990, and 1992.

2. The EIAJ Semiconductor Reliability Sub-committee began standardizing CDM test methods in 1990; the Tentative CDM Test Method, EDX4702-01 was established in 1994.
3. The JEDEC Semiconductor Reliability Sub-committee (succeeding EIAJ Semiconductor Reliability Sub-committee) adopted EIAJ ED4701/300-2 (JEITA Standard) in April 2006, aligning approximately with JEDEC JESD22-C101D. The committee is now examining differences among the CDM specs and is looking for further improvements.

Q16: With the roadmap shown for CDM, will there be a corresponding roadmap for HBM?

Answer: HBM levels are not package dependent, and sufficient ESD controls exist in manufacturing to achieve 500 volts HBM today, so a roadmap for further reducing HBM levels is less necessary. This is explained in Chapter 2. Also, with today's modern packages with high pin counts, the HBM pin combination stress scenario in the real world is less meaningful. Therefore, CDM trends will be the most important and will dominate the achievable ESD levels.

FAQ on CDM Design

Q17: Why is the technology scaling such a severe issue for CDM design? If it is only related to gate oxide breakdown voltage limits, shouldn't the technology development engineers make the process more robust, since otherwise the transistors might get damaged during routine signal applications?

Answer: The gate oxide scaling continues for improved transistor performance. But it is about to reach a limit of tunneling effects and consequently, the actual transistors are not easily damaged under normal circuit operating voltage conditions, which also scale. However, CDM stress does not scale and gets worse for larger devices, and the breakdown voltage condition/charge trapping effects continue to take place at lower voltages. This results in major challenges for CDM protection design.

Q18: Why are designs facing such severe restrictions for CDM as opposed to HBM? Do you not use the same protection concepts?

Answer: While HBM designs also face restrictions as described in White Paper 1, the impact on CDM is much harsher because of the relatively higher current levels involved in this stress test at levels close to spec targets. As a result, secondary stage protection is needed for additional voltage drops. But this secondary stage results in a drastic reduction in the high-speed circuit performance and therefore CDM design is a bigger challenge. The details are presented in Chapter 2.

Q19: If the design is such a critical issue for CDM performance is there an effort to develop more advanced protection concepts?

Answer: What we learned is that no matter which design is implemented, the fundamental nature of the capacitive loading, and its impact on circuit speeds does not change much. Some might claim that they have a more sophisticated design but eventually, the physics of the limitations would take over.

Q20: Would the technology shrinks and the package size increases ever come to a saturation point such that a minimum CDM target would level off?

Answer: They could and most likely would. That is why we project a minimum CDM level of 50 volts could always be designed but this would depend on the eventual trends for circuit speed performance.

Q21: What are the driving factors behind reducing CDM levels from 250 volts for high-speed IOs?

Answer: Several factors are driving the CDM reduction. First, the increasing package size driving increased CDM peak currents. Technology scaling, which drives reductions in the ESD design window (as discussed in Chapter 2), and finally, high speed/RF frequencies are increasing rapidly requiring lower ESD device capacitance values. As is noted though, this need for a reduction to a target level below 250 volts applies to very high-speed IOs (> 56 Gb/s). Lower performance IO, such as general-purpose IO, must still be designed for 250 volts as today's manufacturing is not yet ready for all pins to be below 200 volts.

FAQ on CDM FAR

Q22: You claim in Chapter 4 that a CDM testing level of >1000 volt cannot reliably be tested. Why do you include >1000-volt numbers in the analysis of Appendix F?

Answer: First of all, some product datasheets state > 1000-volt performance. This is because the product sustained >1000-volt discharge. Appendix F details that such stress is not always more severe than stress at a lower level. Secondly, Chapter 4 clearly shows that at those levels no dependence on the CDM level is observed. This supports the earlier remark.

Q23: Why did you choose to remove products with more than 100 fails?

Answer: The analysis of the FARs revealed that the statistics were dominated in all voltage classes by just a few designs showing EOS failure signatures. Therefore, these outliers have been removed to show that without them there is a relatively equal distribution across all classes with a failure rate below 1 DPM.

Q24: Is the connection between the return rate and failure rate known for the studied population? Often, the customer does not return all failures and/or does not divulge the actual failure rates

Answer: Failure rate and return rate might not be equivalent in general. Typically, the number of fails that get returned to the IC supplier is very high for automotive applications, while for consumer ICs customers there may not be as much interest in clarifying each fail. However, as also found in White Paper 1, the statistics of both consumer and automotive parts follow the same trend.

FAQ on CDM Test Methods

Q25: For CDM, is there a difference in the waveforms for inputs versus supply pins? Does this have an impact on qualification?

Answer: The CDM waveform is dominated by the capacitance between the device under test and the field plate. The total charge in the stress current is determined by this capacitance and is independent of the type of pin being stressed. Some differences in the waveform will occur due to differences in the impedance between inputs and supply pins. Comparisons of pulse shapes between ground, power, and input pins on specific examples show that input pins have a slightly lower peak current and a slightly wider pulse width. The amount of peak reduction will vary from design to design. This difference in peak current and pulse width is not a concern in qualification. Real-world CDM events will be modified by the impedance of the stressed pin in the same way as in the CDM test.

Q26: How will the CDM tester variations be addressed?

Answer: The standards bodies are always reviewing the standards to improve them. The data presented in this white paper will provide these organizations with considerable data to aid them in improving the standards. However, the standards bodies are encouraged to proceed with caution. The industry has considerable experience with today's test methods which gives users of the data a degree of confidence in the meaning of a particular pass or failure level. It is likely that any change in the standards to reduce variations will also produce a discontinuity in the measured CDM robustness levels. The standards bodies will therefore proceed with improvements cautiously.

Q27: Will the Industry Council address the Standards and tester variations in the future?

Answer: No. As stated previously, the Industry Council is not a standards body. We have set the recommended target levels based on the existing standards. Standard bodies have the responsibility to define physically consistent and practical standards. Test equipment vendors have the responsibility to produce testers that comply with the standards. Our conclusions in this document do not change any of these responsibilities.

Q28: Our Company is just starting CDM testing. Which CDM standard should we use for qualification and why?

Answer: This question has become much easier in the last few years. The ANSI/ESDA/JEDEC JS-002 CDM test standard has replaced the separate JEDEC and ESDA CDM test methods. Additionally, the Automotive Electronics Council (AEC) now uses ANSI/ESDA/JEDEC JS-002 as the base document for both its CDM standards, AEC - Q100-011 Rev-D for integrated circuits and AEC - Q101-005 - REV-A for discrete components. ANSI/ESDA/JEDEC JS-002 has therefore become the default CDM test method for most products other than automotive. For automotive products, the AEC documents have some additional requirements, but the CDM tester is identical. Products sold in Japan may require the use of the JEITA CDM test method, EIAJ ED-4701/300-2 Test Method 305. It is important to remember that all of these standards address the same failure issues.

Q29: If our company has a 500-volt CDM part with the ANSI/ESDA/JEDEC JS-002 test method, what does this mean for the JEITA method?

Answer: A 500 volt CDM part using ANSI/ESDA/JEDEC JS-002 will likely pass at a higher voltage with the JEITA test due to the lower currents in the JEITA standard for the same voltage. It is not possible to strictly scale the passing voltage between the two test methods.

Q30: Why are there two different CDM standards? Is there a customer perception of a differing performance of one model over another? Which features of the CDM environment require three different standards?

Answer: The existence of two CDM standards, ANSI/ESDA/JEDEC JS-002 and JEITA is largely due to the different organizational structures and history and not due to an effort to model a different physical mechanism. Some people indeed prefer one standard over another. It may be due to a preference for one calibration method over another or a preference over how one standard explains the measurement procedure. Often it is due to familiarity. The use of a particular test method for an extended time will bring a level of confidence in the results. A change to a different test method will require a rebuilding of confidence.

Q31: If the IC device fails CDM due to charge/rapid discharge, shouldn't the charge on the device be included in a CDM metric?

Answer: Charge is certainly an important quantity in the CDM test method. The CDM test method, however, is built on the assumption that different integrated circuits will charge to similar voltages if handled in the same way, without regard to the size of the integrated circuit. The amount of charge needed to reach a particular voltage will scale with the capacitance of the circuit to its surroundings. If the capacitance of the device to the field plate is known, it is then straightforward to calculate the charge on the device. This charge will relate to the size of the current pulse and therefore has a bearing on the protection design required for a particular size device.

FAQ on Charged Board Events and EOS

Q32: Are charged board events (CBE) related to CDM and hence the IC pins should be designed to CBE?

Answer: The CBE discharge mechanism is conceptually related to CDM for a single component. However, the board level aspect of CBE (much greater capacitance of supply/ground planes and reduced inductance of the supply/ground path) makes the CBE failures much more severe in comparison with CDM. They are easily mistaken for EOS. Component IC pin ESD protection cannot be designed to protect against CBE, which can be quite large and can vary considerably from application to application. Additional system-level EOS protection must be provided. See Appendix G.

Q33: If CDM methodology and levels are modified would there be more fallout for EOS at the component or System Level?

Answer: CDM and EOS failures are completely different in total energy and time duration. Effective CDM protection does not guarantee EOS protection. EOS protection must be provided

at the system level. There is no correlation between component CDM failures and system EOS damage. Please refer to Appendix F.1 and Appendix F.1.3 for details. The fallout rate due to EOS would not change as a result of modifying CDM methodology and levels.

Q34: Can CDM replace or be replaced by any of the other ESD standards?

Answer: No. The energy, time duration, and nature of the discharge are so different that CDM is complementary to the other standards. Appendix F addresses this question.

Q35: I often hear that the IEC61000-4-2 pulse is a superposition of a CDM and an HBM pulse. Can IEC 61000-4-2 ESD testing replace CDM and HBM testing?

Answer: No. Looking at the two peaks in an IEC 61000-4-2 pulse the time duration is indeed comparable to a CDM and HBM pulse. However, the required levels and discharge nature are completely different. This is because CDM is intended for component-level testing and the IEC 61000-4-2 standard is intended for system-level testing. See Appendix F, Sections F.1 and F.1.2. for details.

FAQ on CDM Phenomena

Q36: How does CDM discharge occur in the real world or the factory?

Answer: CDM discharge occurs when the voltage difference between a charged device and another metal body exceeds the breakdown voltage of the small air gap between them. If the voltage difference is high, discharge begins at a wider gap distance and spark resistance is higher. If the voltage difference is lower, the discharge does not occur until the gap distance becomes small enough and spark resistance is lower. See Appendix E for more detail.

Q37: Why and how is the device statically charged?

Answer: E-Field charging and tribocharging are the main methods of device charging. Changes in the electric field around a device change the potential of the device without changing the net charge on the device. The change in potential makes the device vulnerable to a rapid current pulse or CDM event when it contacts a conductor at a different potential. Tribocharging occurs if a device slides across the surface of another object. Other examples of tribocharging are picking up a device from a tray or carrier tape and peeling a cover sheet or tape from a tray or reel. See Appendix E, Section E.1.2.

Q38: Does CDM stress in the real world depend on the device package?

Answer: CDM stress in the real world is changed by the device package and many other conditions such as relative humidity, temperature, contact surface, and contact speed. The package is the major part that defines the capacitance of the charged device and the capacitance of the discharging object, as well as affecting the inductance and resistance of the discharge path. The package type also decides the handling method in the manufacturing environment that is most likely to cause charging and discharging effects. More details are given in Appendix E.

Q39: What are the major differences between real-world CDM and tester world CDM?

Answer: The purpose of the tester world CDM is to give the most stable and repeatable charging and discharging of the device because it is a qualification tool. The tester keeps parameters such as charging voltage, device charging capacitance, contact speed, device discharging capacitance, and discharging resistance as repeatable as possible. Discharging inductance should be reasonably low to meet the requirements of the test standard. In real-world CDM events, on the other hand, most of these parameters cannot be easily controlled. The only thing one can do is to eliminate operations that charge or discharge a device or reduce the charge on a device. In the real world, device capacitance at charging and discharging is typically very different (capacitance at charging << capacitance at discharging). More details are given in Appendix E.

Q40: How do I use the analysis of Appendix D to calculate the now-familiar plots of I_{PEAK} vs. package size or I_{PEAK} vs. effective capacitance?

Answer: Start with the simple 3-capacitor model in Appendix D.1. Package dimensions, plus probe lengths, dielectric properties, and other features of the CDM machine are sufficient to calculate the three capacitances and solve the network to give the effective capacitance C_{eff}. This can be set up on a spreadsheet with the variables easily controlled. A larger package size will make for a larger C_f and C_g but will subtract from C_{frg}. Fringing fields always enter in, but their effect can be estimated easily enough. Notice that as package size grows, the C_{eff} will grow sub linearly due to the limiting effect of C_{frg}, which depends on field plate, upper ground plate, and declines with package size as noted above.

Once you have a C_{eff} for the package, the inductance values L_p and L_d can be estimated from Table D-I for the simple 2-pole model (i.e., forget C_d and C_p) and the I_{PEAK} expression(s) can be used to calculate I_{PEAK}. Again, this is easily captured in a spreadsheet. A resistance, R, of 25 Ω for the ANSI/ESDA/JEDEC JS-002 CDM machine spark fits well in most comparisons to measured data. In most cases $R<2\sqrt{(L/C)}$, so you will use the inverse tangent expression, underdamped (i.e. Equation 9). Remembering the relation between package size and C_{eff} for a particular package design and presumed inductance values, you can now plot I_{PEAK} vs. package size or C_{eff} as measured by the charge in the CDM pulse. It is evident from Figure D7 in Appendix D that I_{PEAK} goes up as C_{eff} goes up, although the increase is sub linear, as expected.

Q41: Can the analysis of Appendix D also be used to find the effect of package trace length on peak current?

Answer: Yes. This is only a little more subtle than I_{PEAK} vs. package size or C_{eff}. Once C_{eff} is determined for a particular package, package trace length affects the inductance, as the package trace behaves like a nearly shorted transmission line of a particular length. Table D-I in Appendix D gives an approximation of the inductance, L_d, of package traces of various lengths. These inductances are added to the L_p values in Table D-I for the test head, giving a total inductance for the simple 2-pole model. Again, for that model, we must overlook distributed capacitance C_p and C_d, but that can be done if you're looking for a simple waveform and a single I_{PEAK}. Figure D7 again is helpful, and it is clear that I_{PEAK} goes down as total inductance goes up, with trace length being some fraction of that total inductance.

Chapter 1: CDM Background and History

Tim Maloney, Intel Corporation (retired)

Since the 1970s, the charged device model (CDM) has been associated with the mechanical handling of integrated circuits (ICs) and is cited as a reason for the failure of those ICs. Much of the early work was done at Bell Laboratories [1, 2]. Some of this very useful early work at Bell used a simple vacuum relay to switch stored charge from a component to a nearby ground plane. This was simple but effective and allowed many designers (at many locations, due to Bell's willingness to talk and write about it) to improve their semiconductor components. Bell continued its work on CDM in the late 1980s and early 1990s in their development of a machine [3,4] that evolved into the commercial testers of today. In the past, these CDM testers were usually built to be in agreement with CDM test standards by the ESD Association and JEDEC [5,6], first released in the mid-1990s. Today the testers are built to meet the joint JEDEC/ESDA CDM standard, ANSI/ESDA/JEDEC JS-002-2018 [7]. We will call these CDM testers ns-CDM or non-socketed CDM testers.

Components become charged during handling because of triboelectrification or because of being discharged while in the presence of an electric field. Triboelectric charging results from frictional contact by dissimilar materials, while E-field induction takes place near a surface (e.g., nonconductive plastic) that is already charged. CDM ESD stress results when a component under such influence connects to a conductive surface (e.g., a pin touching grounded metal in a socket) at a different potential. For either the triboelectric or the E-field charging, the effective component area figures heavily in the total amount of CDM charge. For triboelectricity, the charge is expected to be proportional to the interfacial contact area with the other surface, while for E-fields, Gauss's Law (normal E-field proportional to surface charge per unit area) indicates that charge goes as component area.

The Bell Labs CDM tester [3,4] for semiconductor components, a non-socketed CDM tester, was developed in order to duplicate real CDM events as closely as possible. These machines were set up so that the CDM stress depends on the semiconductor package being used, the charge scales with package area, and so on. The standards adopted by ESDA and JEDEC [5,6,7] allow a field-induced CDM test system, so called because it uses a field plate to induce a high potential on the component, although charge does not flow onto the component until the discharge event. Figure 3 is a sketch of the ns-CDM tester from several Bell publications that was reproduced in the original JEDEC CDM spec. This method is equivalent to the direct charging CDM method, whereby a single pin (usually a substrate pin) charges the device with respect to a ground plane located under the dielectric, and the CDM discharge is applied with the discharge probe. The ESDA CDM spec [5] allowed for both direct charging and field-induced test methods, with several commercial versions of the tester allowing for both kinds of CDM testing. The joint JEDEC/ESDA standard ANSI/ESDA/JEDEC JS-002 only supports field induction. Figure 4 shows a CDM waveform as sketched in the original CDM standards document, in this case, JEDEC. See Appendix C for more details on CDM testing.

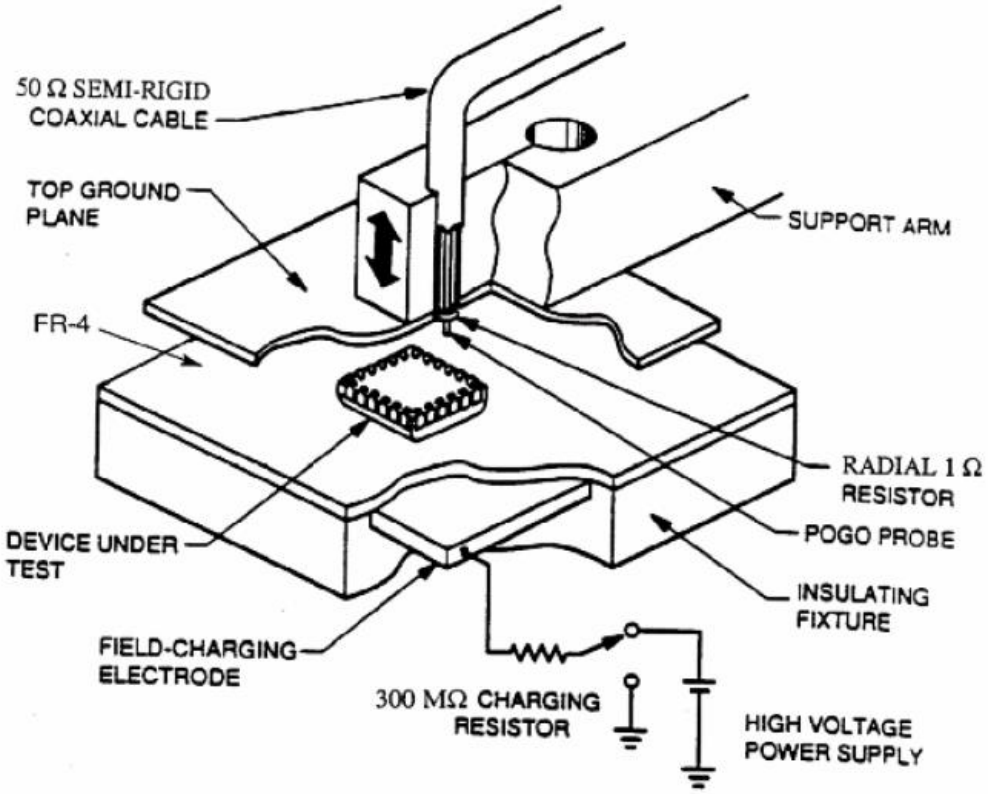

Figure 3: Sketch of ns-CDM charge device model test system by Bell Labs and incorporated in JEDEC CDM specification.

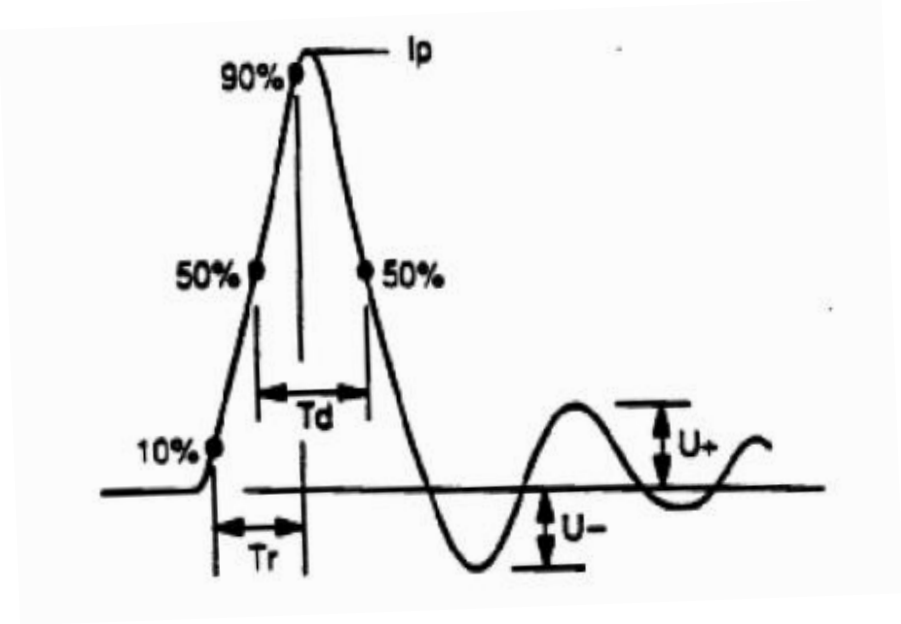

Figure 4: CDM waveform from ns-CDM standard document. Td is about 1 nanosecond.

Since the early 1990s, the socketed device model (SDM) has been a convenient way to exploit automated ESD testing equipment for CDM-like testing of components, using sockets and relays. The history of the first full decade of SDM testing is well-reviewed in a 2001 article [8], which followed shortly after the ESD Association technical report on SDM [9]. Waveforms and parasitics associated with SDM were found to be very different from ns-CDM, although both had the fast-pulse character of CDM and were useful in discerning product weaknesses to CDM. But the advances in process technology of the 1990s, along with much testing of components, made it clear that SDM and ns-CDM could not be unified into one standard. As of August 2017, the ESDA withdrew both the SDM standard practice and technical reports.

A brief history of CDM developments is as follows [10]:

- 1974: Model was first proposed by Speakman —"Human body model is not the only concern to semiconductor users".
- 1980: Bossard et al — "ESD damage from triboelectrically charged pins". Details of the potentially damaging model were given in this paper.
- 1985 and 1986: British Telecom workers made experimental investigations of the field-induced ESD model.
- 1985 and 1986: With the rapid introduction of automated handlers, CDM has become a major ESD failure mode.
- 1986: Japanese reported the first automated CDM testing system. (Fukuda et al, OKI Electronics)
- 1987: Siemens Group reported susceptibility of 256K DRAMs to the CDM testing versus real-world situations.
- 1987: Avery (RCA) reported design techniques for CDM protection.
- 1988: Maloney (Intel) reported more extensive design guidelines to avoid CDM failures.
- 1989: AT&T reported a field-induced charged device model simulator.
- 1995-Present: CDM failures became an important issue for IC devices with the shrinking of gate oxide thickness.

Much of this history was discussed in a review article about CDM [11].

In the initial stages of work on CDM and through the 1980s, the most common target voltage for CDM performance was 1500 volts. This was usually achievable with the equipment used and was achievable for the semiconductor devices. For relay-based methods, passing 1500 volts tended to compensate for the slow rise time and reduced peak currents of a relay-based system. However, as the testing hardware advanced, along with advances in semiconductor technology and our knowledge of what the components really experienced, opinions about the voltage target changed and lower voltage targets were accepted. The non-socketed CDM tester became better understood in terms of its actual rise time, peak currents, and waveform shapes. Users built up confidence in its ability to reproduce factory-level events. 500 volts had become acceptable to most of the industry as a non-socketed CDM voltage target for components that could be handled under "reasonable" static control conditions. A study of CDM stress in the factory and how it relates to the non-socketed CDM test voltage scale has revealed that 500-volt non-socketed CDM performance should usually meet those expectations comfortably [11]. As will be discussed later in this white paper, advances in integrated circuit technology, the demand for higher performance devices, larger package sizes, and advances in ESD control in factories call for further lowering the required level of CDM robustness.

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Chapter 2: CDM Challenges to IC Component ESD Design

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2.1 Introduction

Over the past two decades, charged device model ESD testing has increasingly become an industry requirement for the qualification of IC components. Unfortunately, over this same time interval, three trends have combined to greatly complicate the task of designing effective on-chip CDM ESD protection circuits.

1. The pin count and size range of IC components has grown significantly. This is a serious issue because the peak current produced during CDM testing at a given pre-charge voltage is a sensitive function of the die and especially package size. The net result is that the upper range of CDM currents seen on products is increasing rapidly. Large increases in ESD layout area on the die are required to protect fragile circuits at these higher currents. In some cases, the required ESD layout area becomes prohibitively large.
2. Advancements in IC process technologies with smaller and more fragile active devices as well as thinner and more resistive interconnects have degraded the ESD robustness of circuitry to be protected. This makes it more difficult to protect the component at a given CDM current level.
3. Mixed-signal ICs with high-speed digital, RF analog, and other performance-sensitive pins are becoming much more prevalent. Strict electrical performance limitations on these pins limit options for ESD protection. This often makes it impossible to meet typical CDM ESD qualification criteria.

Taken together, these trends have led to greatly increased challenges for the design of on-chip ESD protection. As a result, many products fail or are marginal to CDM qualification targets of 250 volts or 500 volts. This is a fundamental problem that will only get worse as these trends continue. This chapter is an attempt to summarize the CDM challenges to IC component ESD design presented by these continuing trends. It also reflects the two stages this document has gone through. In the first release in 2010, the challenges of designing to a CDM target of 500 volts were discussed, and a new target level for all pins of 250 volts was proposed while demonstrating that 250 volts complies with ESD control methods already in place in 2010. This paved the way for the high performance and low power designs which have been created in advanced CMOS FinFET technologies since then. The proposed target of 250 volts CDM has been adopted by an overwhelming majority of the industry today. The current release of this document in 2021, presented here, includes the novel challenge of very high-speed interfaces which are currently in development, and due to performance reasons, cannot comply with the requirements of a CDM target level of 250 volts.

2.2 The CDM Event from the ESD Designer's Perspective

As described in Appendix C, the CDM ESD test differs considerably from the HBM test, both in terms of the tester configuration and the current waveforms produced. These waveforms are compared in Figure 5 [1]. HBM is performed as a socketed device under test (DUT), with the stress pulse delivered between one or more stressed and grounded pins via an external pulse source. The resistor-capacitor (RC) network used in this source produces a relatively long pulse width of ~150 ns for HBM. For HBM, the peak ESD current at a given pre-charge voltage is more or less fixed, independent of the DUT. In contrast, during the non-socketed CDM test, the charge is distributed over the entire DUT and flows through multiple paths to a single grounded pin. Important consequences of this configuration are that the resulting pulse width is very short (~1 ns) and that the peak current produced can vary widely from DUT to DUT, depending on the die and package size. As can be seen in Figure 5, CDM current amplitudes typically vary in a large range from 1-6 amperes. Note that, at the 6 amperes upper limit, the 250 volt CDM peak current exceeds that of a 1000 volt HBM event by approximately 9X.

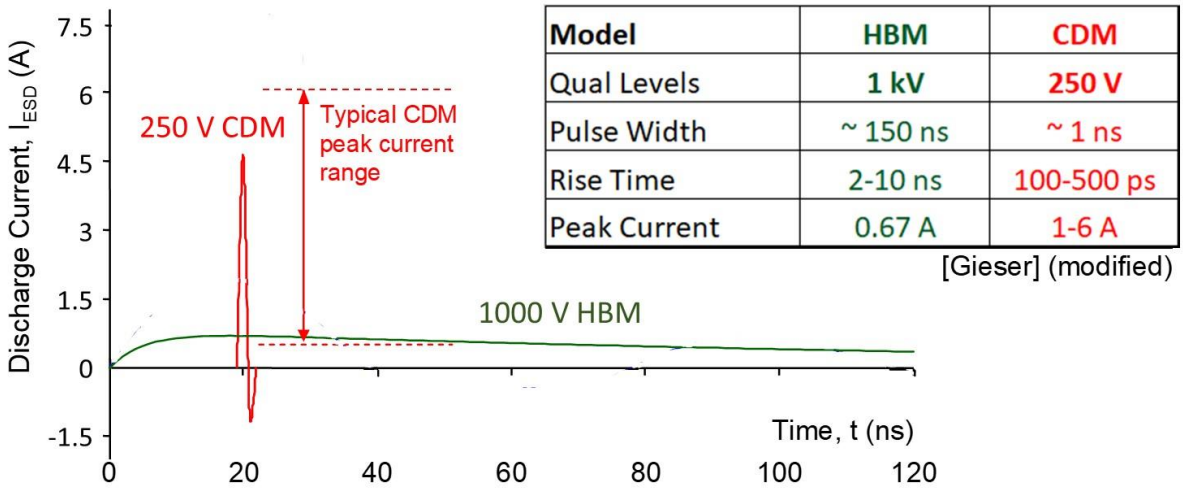


Figure 5: Comparison of current waveforms for CDM and HBM ESD events.

While component ESD stress levels are typically defined in terms of a stress voltage (i.e. 1000 volts HBM or 250 volts CDM), these voltage values are largely meaningless to the ESD designer. Designers consider the ESD event in terms of the resulting current waveform. Elements in ESD protection circuits and ESD conduction paths are sized based on a target peak stress current and duration. In general, if the target peak current increases, the ESD elements, and conduction paths must be increased in size accordingly. As will be shown below, the ESD layout area on the IC increases not linearly, but exponentially with increasing CDM peak current targets.

Another challenge that is unique to CDM is the fact that the true peak current is not known until each new packaged component is tested. When designing, for example, ESD protection for an I/O cell library which may be used in a wide range of products, the designer is forced to estimate peak CDM currents based on the estimated capacitance of the largest expected die and package. Accurate capacitance information is often not available, forcing the ESD designer to more or less guess a CDM peak current target for the I/O cell library. Marginal component CDM ESD

performance is often a result of inaccurate capacitance estimates in the ESD design phase of I/O cell library design. Furthermore, if a given product design changes to a larger IC package, it is expected that lower CDM performance could result. Further discussion on this and some proposals are discussed in Appendix B.

2.3 Design Techniques for CDM

In advanced complementary metal-oxide-semiconductor (CMOS) technologies, circuitry which connects directly to input/output (I/O) pads are often most at risk of damage during a CDM ESD event. In this section, two very common approaches to protecting I/O circuitry are briefly described. This will provide a framework for describing CDM ESD protection challenges in the following sections.

2.3.1 Dual Diode ESD Protection

A schematic of a dual diode I/O ESD protection strategy is shown in Figure 6 [2-6]. The I/O pad connects to receiver and driver circuitry which are powered by the Vddx and GND supply buses. Both primary and secondary ESD protection elements are placed to protect receiver transistors M1-M2 and driver transistors M3-M4, which are typically the I/O devices at greatest risk during ESD. Consider the case where the I/O pad is grounded during a negative CDM event. Most of the positive current will follow a primary path from the grounded I/O pad through the forward-biased D1 diode to the Vddx bus, then down the ESD power clamp to the GND bus, and then from the GND bus metal grid throughout the rest of the IC and package. Note that it is important to minimize the total voltage drop between the I/O pad and GND bus local to the stressed I/O pad during this ESD event. Diode D1 and associated interconnects must be adequately sized. It is also important to minimize parasitic Rvddx and Rgnd bus resistances since they add to the total voltage drop along this primary ESD current path. To better protect large banks of I/O cells in an IC, it is common for multiple power clamps to be distributed in parallel along the power buses.

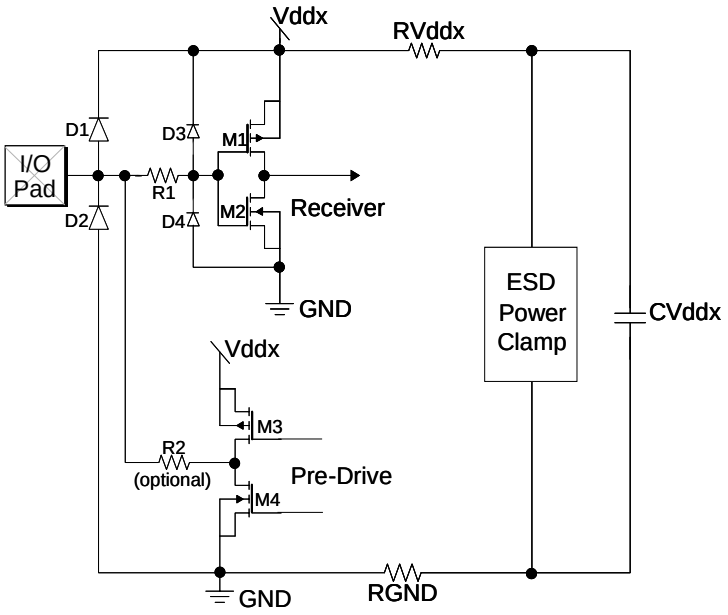


Figure 6: Dual diode I/O ESD protection strategy.

In the ESD strategy of Figure 6, separate secondary ESD protection elements are utilized for the receiver and driver circuitry. During the ESD event described above, a small fraction of the ESD current will flow to Vddx via a secondary path through resistor R1 and diode D3. The benefit of this secondary protection is that any IR drop across R1 will reduce the voltage stress seen across the fragile gates of receiver transistors M1-M2, as compared to the case where R1 is not present. R1 values from 100-5000 Ω are common for protecting receiver circuits. To better protect driver transistors M3-M4, there is another secondary path to Vddx via resistor R2 and the drain to N-well parasitic diode of PMOS transistor M3. Note that the use of R2 is shown as an option in Figure 6. This is because many applications such as high-speed serial (HSS) links or low noise amplifiers (LNA) do not typically permit the use of any series resistance between the driver and pad due to performance constraints. Typical R2 values for digital applications can range from 5-100 Ω. This resistance can have a significant impact on the effective CDM robustness of driver transistors M3-M4.

2.3.2 SCR-Based ESD Protection

A schematic of an SCR-based ESD protection strategy is shown in Figure 7 [7-11]. Here the primary ESD protection comprises a diode string triggered SCR clamp from the I/O pad to the GND bus. Therefore, when the I/O pad is grounded during a negative CDM event, most of the positive current will flow from the pad directly to the GND rail via the SCR clamp and then from the GND bus metal grid throughout the IC and package. This direct clamp to GND is an advantage of the SCR-based protection scheme over the prior diode-based approach, especially in cases where the GND bus resistance is significantly lower than Vddx bus resistance. In addition, SCRs often have reduced capacitive loading for the same ESD protection level. On the other hand, diode string triggered SCRs can have the disadvantage of higher leakage during normal operation depending upon the maximum operating voltage required.

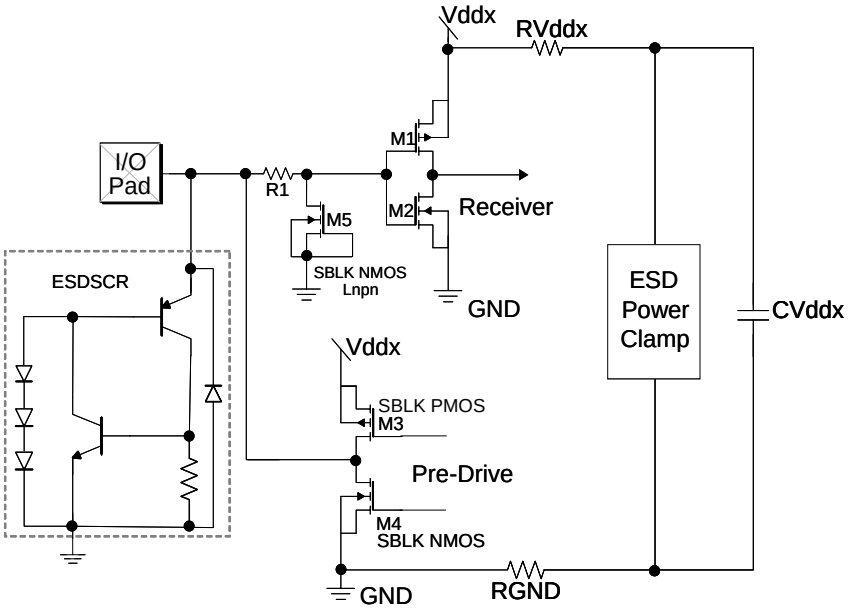


Figure 7: Diode-string-triggered SCR-based I/O ESD protection strategy.

Note that, in the ESD strategy of Figure 7, a different type of secondary protection is utilized to protect the receiver transistors M1-M2, as compared to that shown in Figure 6. Here a fraction of the ESD current will flow to GND via a secondary path through resistor R1 and clamp device M5. This clamp is a silicide blocked (SBLK) NMOS transistor which is intended to trigger and conduct as a lateral NPN bipolar during the ESD event. Blocking the silicide in the drain region adds local ballast resistance to the NPN, helping ensure uniform current flow across the device width during bipolar conduction, thereby increasing the failure current (I_{t2}). As before, any IR drop across R1 during ESD will reduce the voltage stress seen across the gates of receiver transistors M1-M2. Note, the secondary ESD NFET is shown for reference only, in this example, the secondary device could be replaced by dual diodes, forward-biased diode strings or another diode string triggered SCR.

The output drivers M3-M4 in Figures 6 and 7 can also be configured with silicide blocking in the transistor drain regions. Added ballast resistance increases the failure current (I_{t2}) of the drivers in the event they trigger and conduct as lateral bipolar transistors during ESD. Also, the added IR drop across this silicide block resistance increases the effective drain to source breakdown voltage the transistors can tolerate before suffering permanent physical damage. This provides more voltage margin to driver breakdown for the intended primary ESD path through the SCR clamp. Silicide block ballast resistance is commonly used to harden output driver transistors against ESD, typically increasing Vds breakdown voltages 1-3 volts, but at a cost in layout area and transistor performance, and process cost. Other design options, in place of these that have been discussed here, will also eventually lead to the same limitations.

2.4 Technology Scaling Effects on CDM ESD Robustness

Advancements in process technologies over the past 30 years have brought about impressive reductions in IC cost and gains in performance. Unfortunately, these advancements have come at a cost in terms of degraded ESD robustness. Technology scaling has produced smaller and more fragile active devices as well as thinner and more resistive interconnects. For these reasons, the ESD protection design becomes more challenging with each new technology node [12].

2.4.1 Trends in ESD Robustness for NMOS Transistors

In Figure 8 the robustness of NMOS transistors across multiple advanced CMOS technology nodes is compared. The maximum core Vdd supply voltage is shown as a function of the technology node scaling for both feature size transistor length and gate oxide thickness. Also shown is the simultaneous reduction of the gate oxide breakdown voltage (Vgs) and drain to source breakdown voltage (Vds) under 1.2 ns pulse stress conditions. This data was gathered with a very fast transmission line pulse (VF-TLP) characterization tool which best mimics the true CDM pulse event. All data was gathered on a baseline, minimum design rule, fully silicided NMOS transistors. The Vds breakdown data represents the minimum or worst-case value measured with varying DC Vgs bias applied during stress.

The data in Figure 8 clearly illustrates the reduction in NMOS transistor CDM robustness with each new technology node. While both the Vgs and Vds breakdown data trend downward with each new technology node, these NMOS devices are clearly more fragile under the drain to source stress. It turns out that PMOS transistors (not shown) exhibit similar trends but are slightly more robust than their NMOS counterparts. Compare, for example, the robustness of NMOS transistors at the 250 nm and 45 nm technology nodes. A 250 nm NMOS receiver device, such as transistor

M2 in Figure 6, could survive 14 volts Vgs stress during CDM ESD, while the 45 nm device would fail at only 5.2 volts. Similarly, a 250 nm NMOS driver device, such as transistor M4 in Figure 6, could survive up to 6.2 volts Vds stress during CDM ESD, while the 45 nm device would fail at only 3.2 volts. It is clear that transistors become more fragile with each new technology node. This Vds breakdown trend has continued as the channel lengths continue to scale.

It turns out that protecting output drivers with Vds breakdown values of less than 4 volts is a serious challenge for the CDM ESD designer. This is particularly true in applications that do not permit the use of secondary protection or silicide block ballast resistance. Consider, for example, an I/O circuit in a 90 nm technology, with ESD protection as described in Figure 6. During a negative CDM stress event the NMOS driver M4 will fail if the local Vds voltage across this device exceeds 3.8 volts (see Figure 8). Assuming that the peak current produced by the CDM event equals 7.6 amperes, then the ESD elements and interconnect resistances in the primary ESD path must dissipate this current while limiting the total voltage drop seen across the NMOS driver M4 to less than 3.8 volts. Sizing the ESD elements and interconnects to achieve this 0.5 Ω effective impedance is extremely difficult.

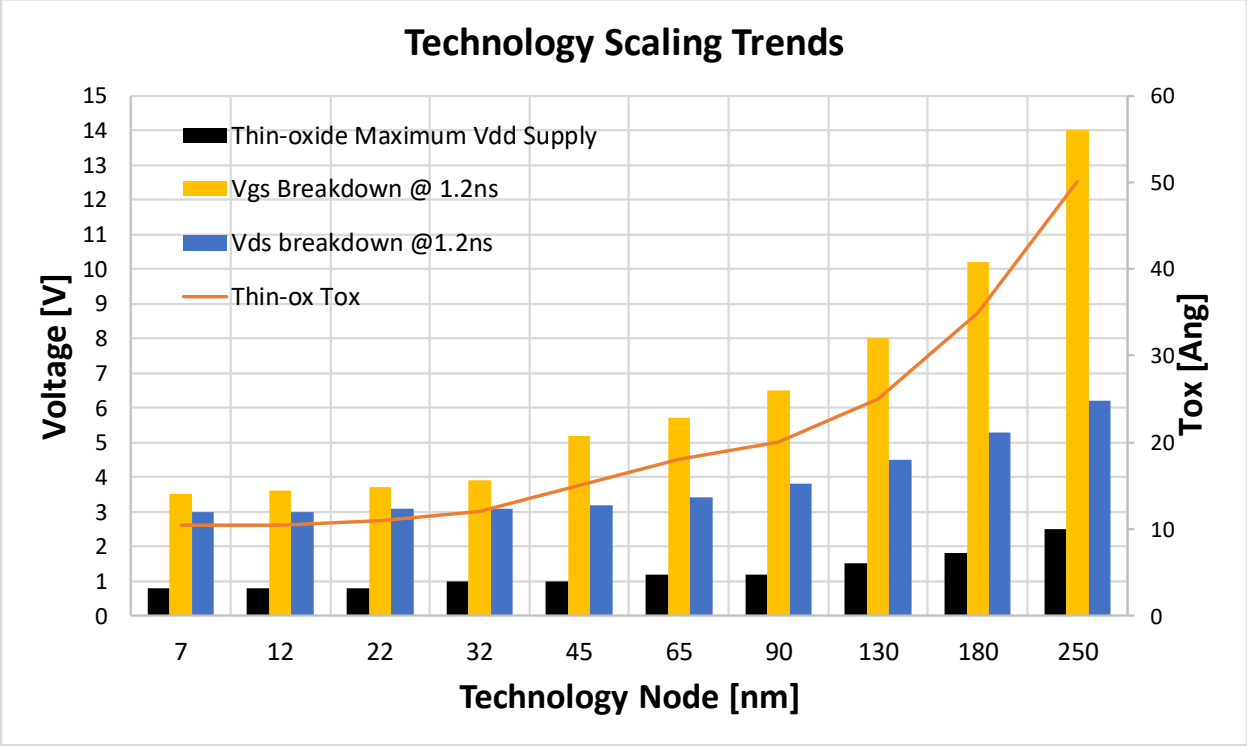


Figure 8: Trends of NMOS transistor breakdown voltages with technology scaling.

2.4.2 Trends in Interconnect ESD Robustness

Another critical technology parameter for CDM design is the maximum allowed current density in the interconnect layers. This trend is shown in Figure 9 typically for a copper metal interconnect. Note that the actual failure current density is dependent on the particular metal thickness, but this trend is more of an illustration of the constraint. In the CDM domain, the current failure density is actually 3-5 times higher than in the HBM domain. However, if the CDM discharge current level requirements become relatively larger (for example, from large high pin count packaged devices meeting a target level of 500 volts) this could turn into the limiting factor for design. For example,

at the 65 nm node, the current density limit of 0.5 A/um requires a 20 um wide bus to carry 10 amperes of CDM current. In addition to the layout area, wider metal interconnects to the ESD diodes increase the pad capacitance. This in turn may have a negative impact on the circuit speed as will be discussed in Section 2.5.3.

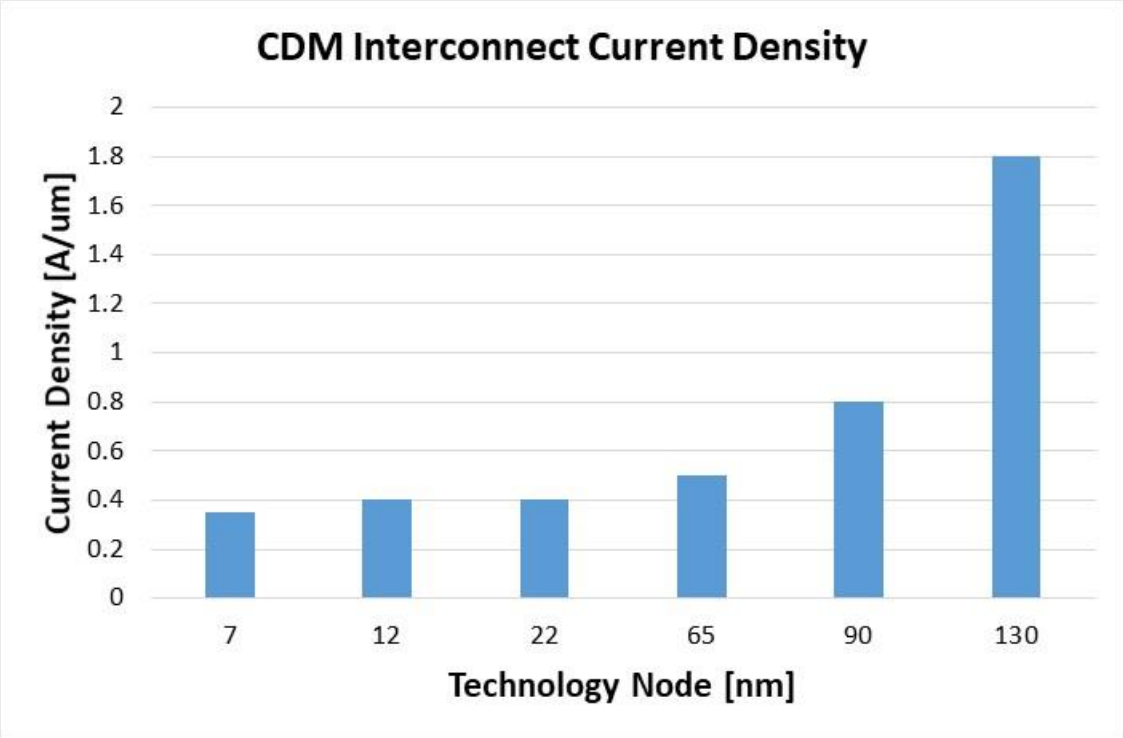


Figure 9: Typical trends for copper interconnect ESD robustness with technology scaling.

2.5 Examples of CDM Impact on Integrated Circuit ESD Design

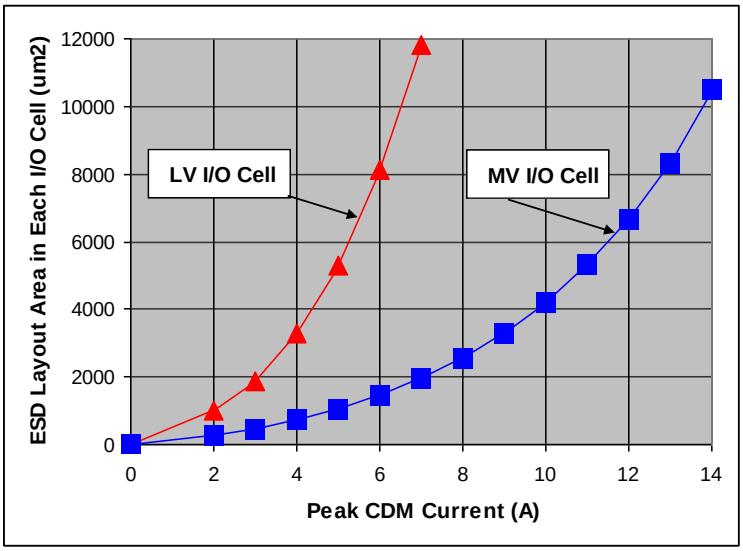
2.5.1 Impact on ESD Layout Area

The ESD layout area on the die required to protect an IC component from a 500-volt CDM event varies widely with product application and process technology. The target peak CDM current the ESD network must safely dissipate is a primary factor affecting layout area. As illustrated in Figure 5, peak CDM currents at 500 volts typically range from about 1 ampere, for the smallest die and package sizes, to 16 amperes or greater, for the largest. The process technology, which defines the efficiency of the ESD devices and interconnects along with the fragility of the circuitry to be protected, strongly influences the layout area. Finally, applications that do not permit the use of added secondary protection or silicide blocking to harden fragile input/output circuits will see significant increases in the layout area. In general terms, a very large IC component in the most advanced available process technology with driver/receiver circuits configured in the most fragile manner requires the greatest ESD layout area on the die.

The ESD layout area as a function of target peak CDM current is shown for two example 45 nm technology I/O library applications in Figure 10. The two I/O libraries differ in the type of transistor used in the driver and receiver circuitry. The low voltage (LV) I/O library, for use in

Vdd=1.1V supply domains, utilizes the core (18 Angstrom Tox) transistors available in the technology. The medium voltage (MV) I/O library, for use in Vdd=1.8 volts supply domains, utilizes the I/O (28 Angstrom Tox) transistors.

The dual-diode and rail clamp ESD protection approach described in Figure 6 was used in both the LV and MV I/O libraries. Small ESD power clamps were distributed in parallel in each I/O cell of an I/O bank within a supply domain. The ESD power clamps in both I/O libraries were built with the more robust I/O transistors. While secondary protection was utilized to harden the receiver circuitry in both I/O libraries, the application would not allow the option of placing either secondary protection or silicide blocking to harden the output driver devices. Therefore, the weak link for ESD in both the LV and MV I/O cells was assumed to be the NMOS output driver M4 in negative mode CDM events, and the PMOS output driver M3 in positive mode events. The measured Vds breakdown values for the NMOS and PMOS driver devices in both the LV and MV I/O libraries are shown in the table in Figure 10. In order to provide a comfortable margin, the ESD networks in both I/O libraries were sized to protect both driver devices to targets 20 % lower than their measured breakdown voltages. Therefore, as shown in the table, the target stress limits were set to 2.65 volts/3.60 volts for the NMOS/PMOS drivers in the LV I/O library and 3.50 volts/5.20 volts for the NMOS/PMOS drivers in the MV I/O library.



		LV (V)	MV (V)
NMOS	Vds (meas)	3.3	4.3
	Vds (target)	2.7	3.5
PMOS	Vds (meas)	4.3	5.9
	Vds (target)	3.5	4.7

Figure 10: Example estimate of the ESD layout area for I/O cell in two different I/O applications. ESD layout area is plotted versus peak CDM current. The layout area is calculated for two different NMOS and PMOS output driver protection targets.

As shown in Figure 10, the size of the ESD elements in both the LV and MV I/O cells is a sensitive function of the target peak CDM ESD current the ESD network must safely dissipate. The area value includes the area for the ESD diodes and power clamp in each I/O cell. Note that, for both curves, the ESD layout area increases exponentially with peak CDM current. In fact, for the LV I/O cell, the increasing slope of the curve suggests that CDM current targets above about 7 amperes are not realistic since, beyond this ESD current ceiling, huge increases in layout area are required to achieve a small incremental increase in CDM current. It is important to note that the exponential nature of the ESD layout area vs. CDM current target curve is common to all process technologies and all ESD protection schemes. However, the actual ESD current ceiling will vary considerably

from product to product, depending on process technology, circuit application, and ESD protection scheme.

It is obvious from the drastic differences between the two curves in Figure 10 that the Vds protection target for the output drivers M3-M4 has a major impact on the ESD layout area required at a given CDM current. While 7 amperes CDM protection can be achieved for the MV I/O cell with about 2000 um^2 of ESD layout area, the LV I/O cell requires almost 12,000 um^2 to meet the same protection level. This is a 6X increase. It should be pointed out that the layout area for full I/O cells (excluding ESD) in advanced CMOS technology products typically ranges from 2000 um^2 to 8000 um^2. Therefore, depending on the CDM current target and the I/O application, the ESD layout area may grow to dominate the overall I/O cell layout area. This is an issue of particular concern for IC components in large packages.

2.5.2 Impact of the ESD Design Window on CDM

It has been well established through various studies that the "ESD Design Window" is rapidly shrinking with the advancement of silicon scaling technologies [10]. As shown in Figure 11, the window is essentially defined as the space between the IC operating voltage (Vop) and the IC breakdown voltage (Vbd). Although the operating voltages have been slowly reducing (flattened out in the 0.9-1.2 volts range), the breakdown voltages have been degrading at a much faster rate giving rise to the reduction in the window. The limitation of the breakdown voltage could come from either oxide breakdown voltage under ESD conditions (for input buffers) and/or from the avalanche junction breakdown voltage (for output buffers). This is indicated as the "IC Reliability Constraints" in Figure 11. On the other hand, for scaled technologies the metal interconnects are getting thinner, leading to more resistive busses for ESD design applications. Thus, designing to a given ESD current level the voltages at the I/O pads build up to the critical breakdown values at even lower current levels. This metal restriction is shown as "Thermal Failure" in Figure 11. This design window reduction applies to any type of I/O protection strategy even though some advanced designs might give a slight advantage. Nevertheless, the overall reduction makes it difficult to design for any high HBM or CDM levels. This is further elaborated in Figure 12.

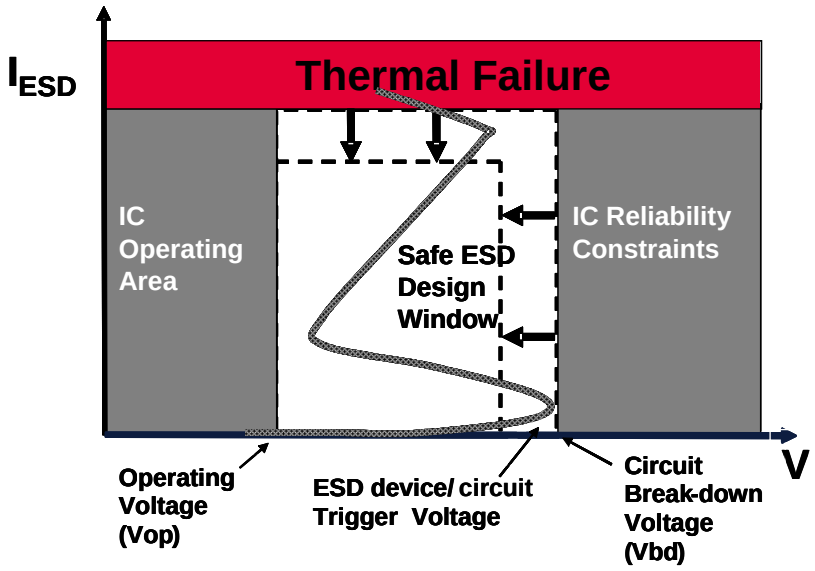


Figure 11: ESD Design Window Definition

Figure 12 shows how the ESD design window (Vbd minus Vop, defined in Figure 11) has scaled going from 350 nm down to 12 nm technology nodes. The design window has shrunk by approximately 2.9X scaling from 350 nm down to 12 nm while the ESD targets have not kept pace with this scaling. The ESD design window reduction requires either larger ESD devices to clamp the voltage to lower levels or it requires significant innovation in ESD devices as technologies scale. Increasing the ESD device sizes to compensate for the design window scaling is not practical for two main reasons: 1) the area allocations for ESD devices/circuits are scaling down at each technology node, and 2) the capacitive loading requirements are simultaneously also being reduced for each new technology generation.

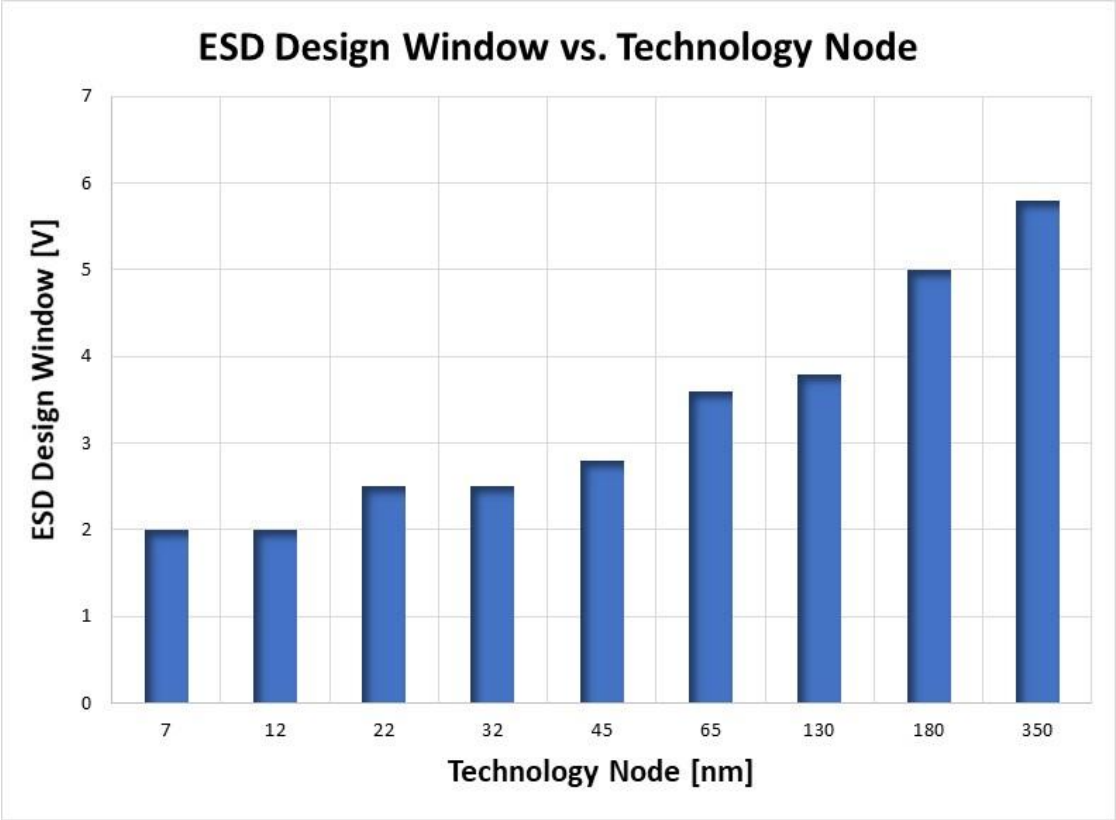


Figure 12: The ESD Design Window versus Technology Node

2.5.3 Impact on HSS, RF, and Analog Applications

In Figure 13 the acceptable ESD capacitive loading is shown for targeted HSS link data rates. The capacitive load of a high-speed data lane has a strong impact on the quality of the eye and the power per Bit. With increasing data rates the acceptable capacitive load declines more and more. However, the concept of the data rate of a SERDES link needs to be carefully assessed when parallel lanes are used. Actually, the critical parameter is the data rate per lane, which depends on the Nyquist frequency and the modulation standard. The widely used modulation approach for interface speed below 56 Gb/s is NRZ (non-return-to-zero) standard. At 56 Gb/s and above the PAM4 modulation standard was introduced. The latter compresses the eye height and is more sensitive to degradation of the eye due to capacitive load. An increase of the Nyquist frequency to 56 GHz and above creates even a higher sensitivity to a capacitive load of the ESD protection.

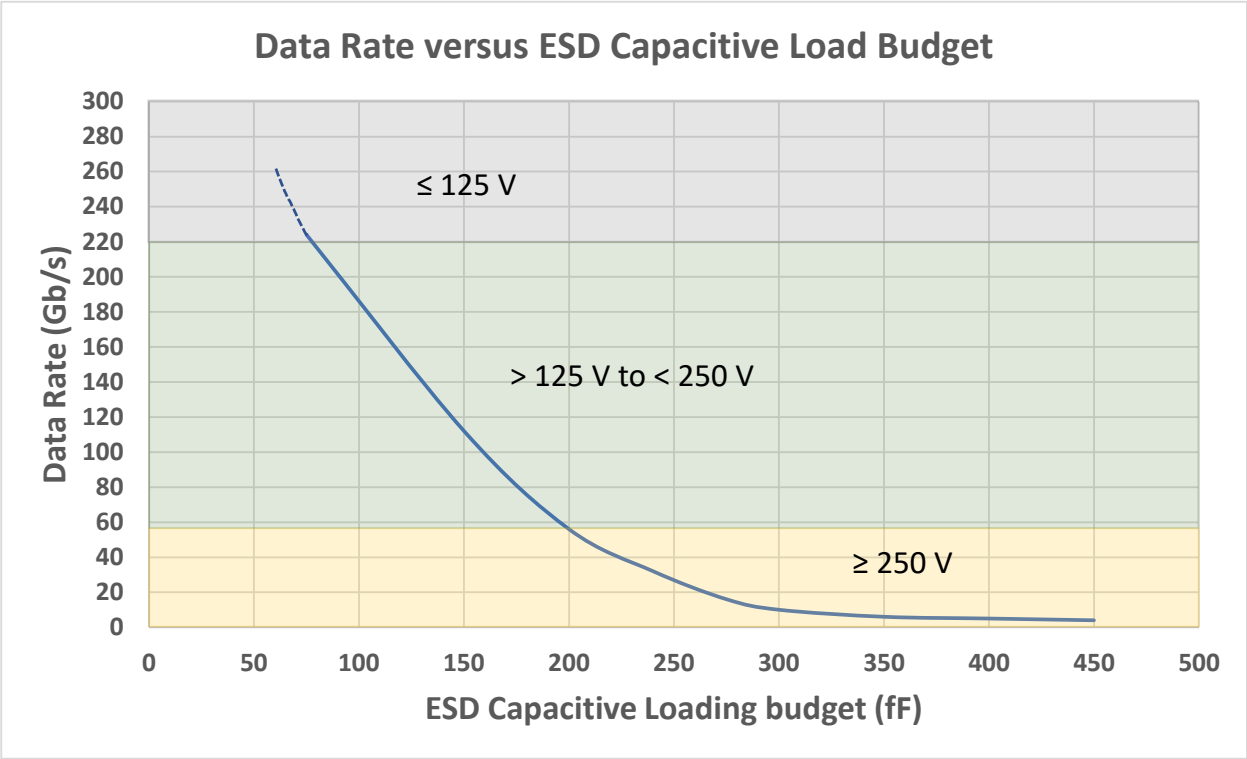


Figure 13: Data Rates of single lane SERDES vs. Allowed ESD Capacitive Loading Budget of high-speed IO circuits. NRZ SERDES interfaces are considered up to 56 Gb/s. At 56 Gb/s and above PAM4 is assumed.

RF high-speed designs are even more restrictive than standard high-speed SERDES designs. For RF pins with 5-10 GHz performance requirements, ESD design can be quite a burden. The low noise amplifier (LNA) input circuits are especially intolerant to ESD protection device capacitance. In these circuits, the ESD ground is often isolated from the LNA ground and separated by diodes as shown in Figure 14. With the usual requirement of less than 100 fF capacitance for the ESD diodes, it is difficult to achieve even 1000-volt HBM protection without damaging the gate oxide. This is mostly due to the on-resistance of the small protection diodes used to meet the circuit RF functional requirements. CDM performance can be even more challenging than HBM for these RF applications.

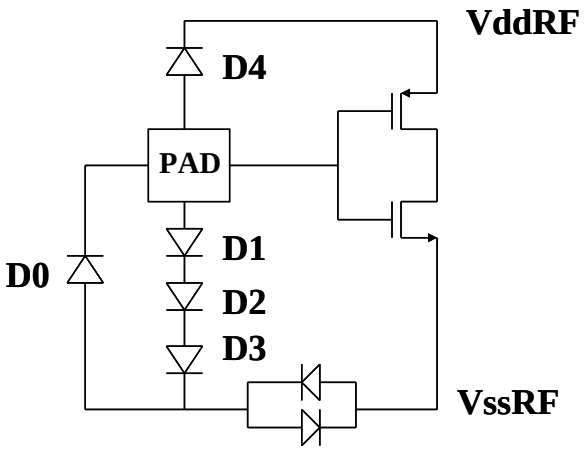


Figure 14: Typical Low Noise Amplifier (LNA) pin with diode protection.

The reasons for the low CDM performance are: 1) absence of secondary clamp, 2) smaller sized protection diodes that build up the voltage to critical levels even for small CDM currents, and 3) isolation of the ESD clamp ground from the RF buffer ground. Regarding restriction #2 the situation could become worse if the input pad is directly connected to the core gate oxide in order to achieve high-speed input performance. The clamp diodes must be smaller in size to meet the low total capacitance budget at the pin.

RF pin application chips with system on chip (SoC) function usually employ small ball grid array (BGA) packages of 8 mm X 8 mm or 10 mm X 10 mm. The peak currents are quite low, not more than 3-4 amperes at 500 volts. However, these sensitive RF designs with small clamps can often only be effective for CDM current levels of 2 amperes or less, thus severely limiting their CDM performance to 200-300 volts. For example, for an RF application chip with 10 mm X 10 mm package size the LNA input ESD design can only handle 2 amperes which corresponds to only a passing level of about 200 volts.

2.6 Package Effects and Package Trends

Advances in packaging technology are based on the requirements of the different market segments [13]. For computer applications, advances are based on performance and reliability. While for the consumer market it is more about the form factor, price, and robustness. For automotive and military applications, it could be temperature sensitivity and reliability. Each type of package is then designed and selected according to the application. This proliferation has gone from the standard dual-in-line (DIP) packages to multi-chip modules (MCM) and to flip-chips and stacked die or even stacked packages. In the past few years, wafer-scale packages (WSP) have also become more common.

Although not particularly considered in the past or even at present, during the package development some attention should also be given to the ESD effects as well. The aggressive technological advances into newer types of packages might very well determine the achievable ESD performance for overall adequate reliability.

The most serious impact that packages have is on CDM where its performance strongly depends on the package type and package lead design. If the qualitatively assessed CDM risk is now imposed the TQFP package might pose lower CDM performance while the micro-star BGA (u*BGA) can show relatively better CDM performance. This is simply related to the peak current that is discharged during the stress and directly depends on the effective package capacitance. Some of the most significant impacts of packages on CDM would come from a variety of packaging factors. What could influence the CDM peak current and hence the CDM performance is summarized for a BGA package below:

- The die size where larger die would mean more capacitance
- The mold compound material and its thickness
- The lead frame metal routing including the number of pins

Chips with larger die sizes that incorporate larger packages would naturally pose a larger threat to CDM design. For example, the measured peak current at 250 volts as a function of the package area is shown in Figure 15 (scaled from 500 volts) [14]. While the HBM current at 1000 volts is independent of the package size, the CDM current rapidly increases with package area. Note that trend, extended out to very large packages in the > 5000 mm^2 would near 6 amperes.

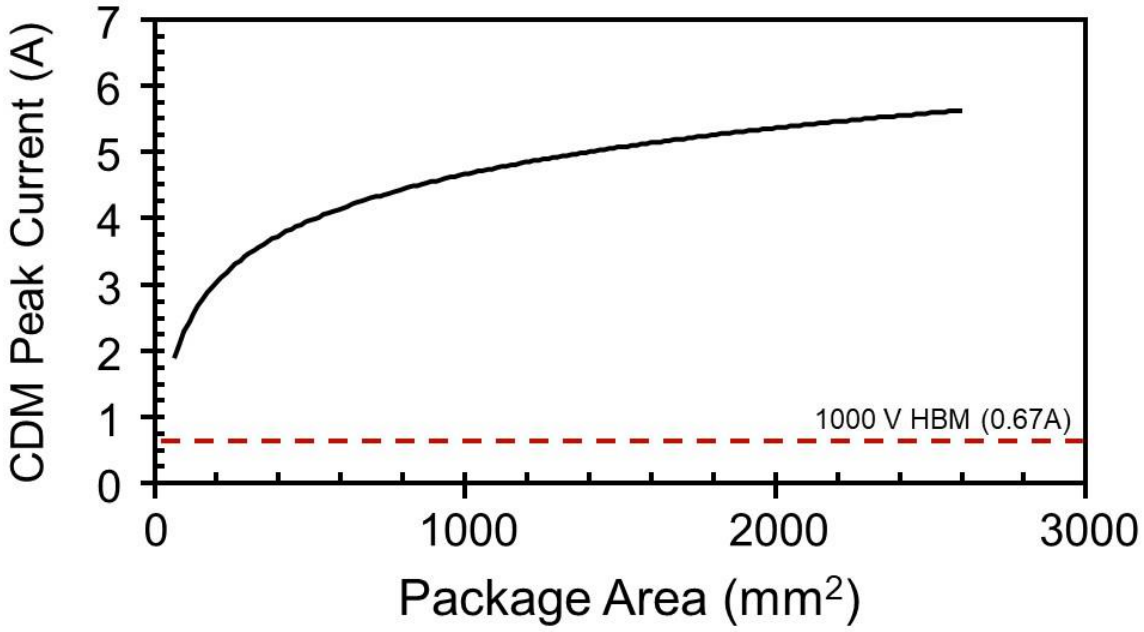


Figure 15: CDM Peak Current data for BGA packages at 250 V CDM.

The most critical design constraint for CDM comes from the trend towards higher pin count packages. This market is driven mostly by ICs for internet switching (with high bandwidth) and microprocessors where very high pin count packages are commonly used. This bandwidth can be achieved by incorporating a balance between high-speed I/O's and wide parallel busses. Designs for such markets use chip-to-chip interfaces with DDR4 (1600 MHz), RLDRAM (1600 Mbps), and SERDES (112/224 Gb/s). Although the trend for increased off-chip speed may reduce the number of I/O's required, it also leads to a higher number of power pins for thermal performance. The net result is an increase in the average pin count. This continued trend for high pin count is depicted in Figure 16 for BGA packages.

With the advancement of 2.5D and 3D technologies, package sizes continue to grow. By 2016 pin counts were over 5000 and in 2020 they are nearing 6000. At this pin count, the package area is well above 5000 mm^2. Indeed, both the die area and the package area contribute to increased CDM peak current at a given voltage stress level. Invariably designs requiring high-speed I/O's tend to be placed in IC packages with high pin count which consequently places a constraint on the CDM design capability.

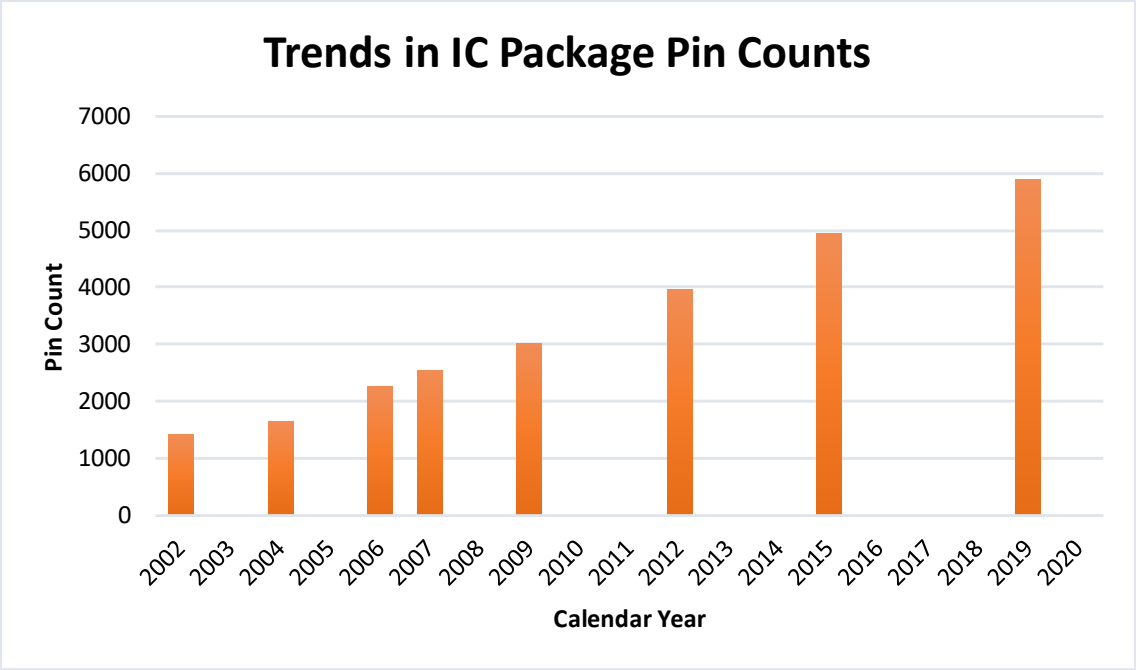


Figure 16: Trend for high pin count BGA Packages

Meeting a 500 volt CDM level, or even a 250 volt CDM level for very high-speed pins, for larger packages will in general not be possible. The more realistic design windows for CDM for package sizes exceeding 1000 mm^2 are shown in Figure 17. First, it is seen the CDM peak current increases as the package area increases (assuming the same thickness package) and that this behavior linearly moves to higher current levels at higher stress levels. For example, a 1000 mm^2 BGA would produce 4 amperes at a 200-volt stress level and more than 10 amperes at a 500-volt stress level. However, the practical design windows dictated by circuit performance would limit the achievable CDM level. For the 65 nm HSS I/O designs with speeds of 5-20 Gb/s, the peak current in the ESD design is restricted to between 2.5 to 6 amperes. This is shown by the blue box in Figure 17. At the 45 nm node, this would degrade to the 2 to 5 ampere range, further lowering the achievable CDM levels. Figure 17 clearly illustrates that for these HSS designs with large package areas the CDM performance is limited to between 200 and 300 volts.

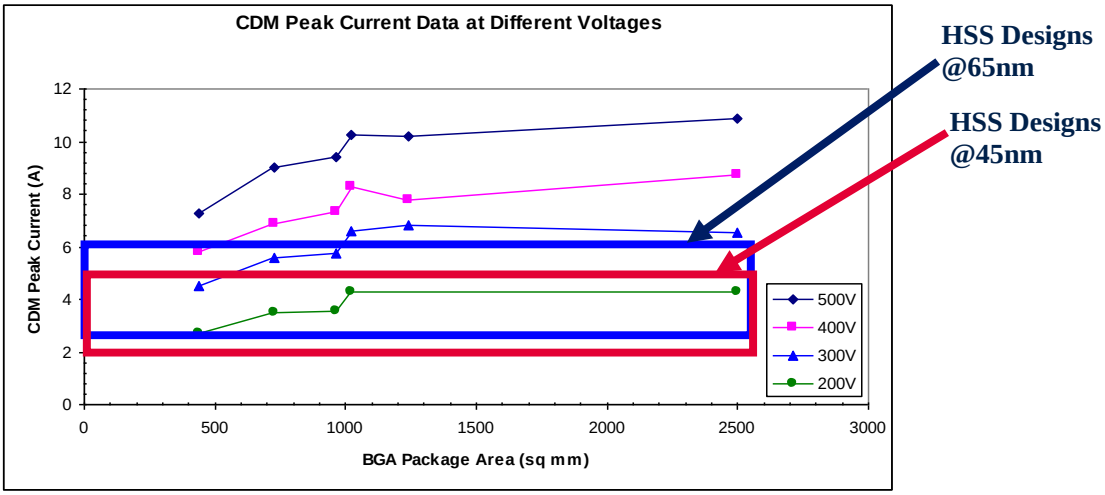


Figure 17: CDM Peak Current data for various packages at various CDM stress levels.

In this manner, we can see that as chip sizes are made larger and built-in complex packages with many more pins (>2000) the CDM stress current will continue to increase in magnitude. Combined with the package effects presented here, RF designs that can tolerate very little capacitance from the protection device will have difficulty meeting the ever-larger CDM currents. In the future, CDM package issues will become worse for stacked packages and multi-chip modules. Moreover, conversion to new organic materials for environmental safety could potentially exacerbate the situation. Therefore, package engineers and ESD engineers need to work in close collaboration to maintain package performance and ESD reliability!

2.7 ESD Designer's Perspective on Realistic CDM Targets

The overall expected performance for CDM while meeting all of the design constraints is already challenging and, in the future, will become even more of a challenge. In order to understand this, we need to examine the total picture of the IC packages ranging from small pin count (<100) to medium pin count (300-500) and high pin count (500 to >1000) ranges. This package map is illustrated in Figure 18. The top row shows the package type trends as they progressed from DIP to BGA to LGA. It is expected that the trend toward a higher percentage of packages being BGAs will continue for the foreseeable future. The second row shows the corresponding number of pins. Based on physical data the markers for the package areas corresponding to the package pin numbers are shown in the third row. After measuring actual peak currents at various stress levels for the different package areas (pin count) the estimated CDM performance chart for different I/O designs is shown. This data was generated by measuring the CDM discharge currents from various sized packages with design constraints defined in terms of maximum tolerable current levels in each case. For example, if a practical I/O design with its CDM protection design can handle 8 amperes of peak current, for pin counts up to 1000 the previously accepted CDM level of 500 volts can be met. But if the pin count goes beyond 1000 to nearly 2000, the CDM performance can only be about 400 volts. These numbers currently reflect 45 nm and 65 nm technologies. The next row for high-speed I/O designs shows that packages devices with >200 pins or a package area of >250 mm^2 cannot meet the same expected 500 volts. It should be noted here that beyond 2500 pin

packages the performance data is only an extrapolation based on the known relation between package area (capacitance) and the CDM peak current as a function of stress voltage.

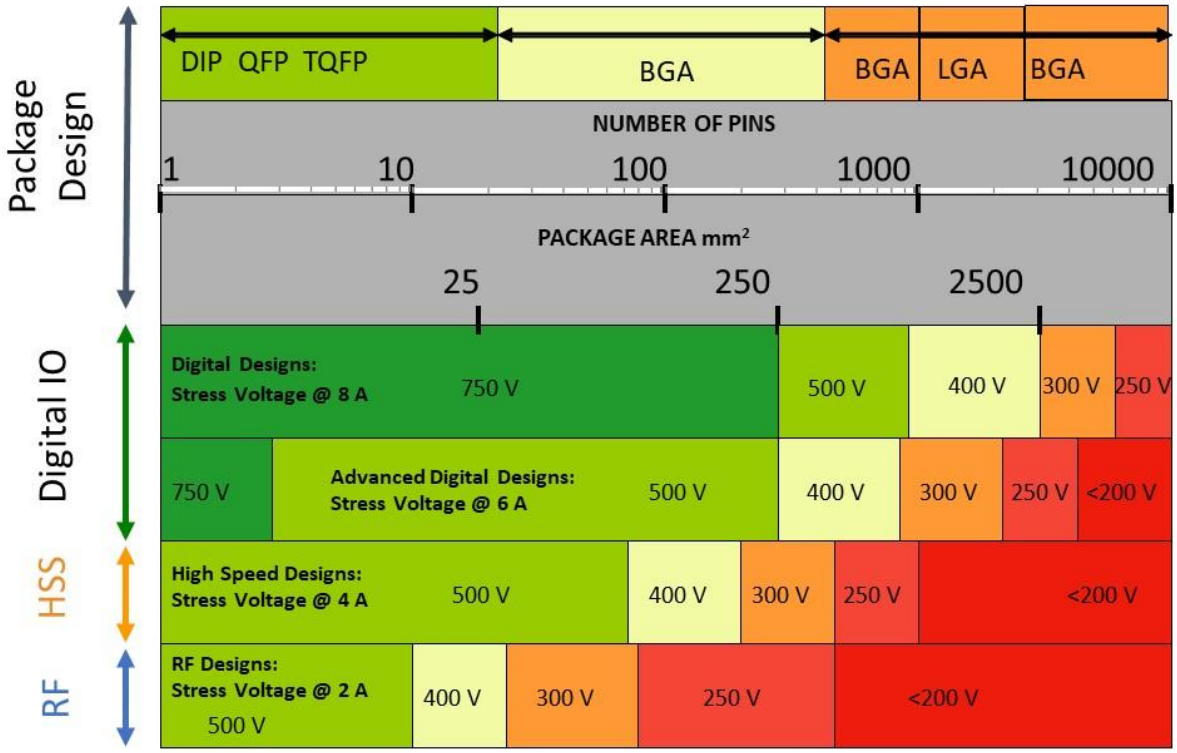


Figure 18: CDM package map for 65 nm and 45 nm designs. Products with >1000 pins or 1200 mm^2 area are limited to 400 V CDM passing voltage for all practical designs; this would reduce to 300 V for high-speed SERDES designs.

Following this trend, the CDM performance restriction faced by RF designs is indicated in the last row of Figure 18. Since most of the RF designs tend to be in smaller IC packages, they are not expected to face the severe degradation of performance as the high-speed serial link (HSSL) I/O's. However, even at smaller package areas, the RF pins are sensitive for CDM design as noted in Section 2.5.3 and thus are challenged to meet a 250-volt level for packages with even 300 pins.

2.8 Further Technology Scaling Effects and Additional Impact on Realistic CDM Targets

At 22 nm technologies and beyond, even a 250-volt level will place more severe restrictions on CDM protection design due to further scaling effects and the drive towards higher circuit speed performance at data rates exceeding 56 Gb/sec. A revised package CDM map for the 22 nm and beyond is shown in Figure 19.

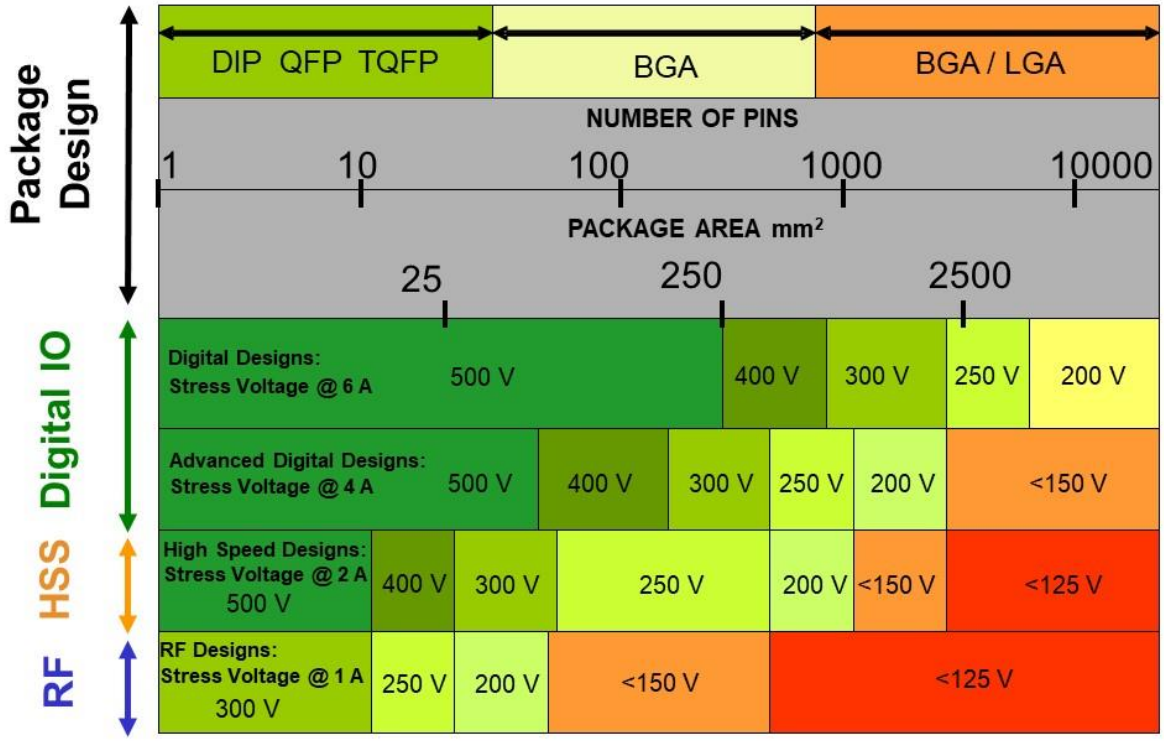


Figure 19: CDM package map, projected for 22 nm designs and beyond. Products with >1000 pins or 1200 mm^2 area would be limited to <150 V CDM passing voltage for all HSS and RF designs.

2.9 High Speed/RF Circuits, Scaling Impact on CDM Targets

As data rates of high-speed I/O interfaces continue to increase, this comes with the challenge of requiring reduced capacitances for ESD devices [15]. Reduced capacitances typically drive smaller ESD devices [15]. Technology scaling, in general, is driving larger area ESD devices when disruptive technologies like FinFETs come along as shown in Figure 20. In Figure 20, technology scaling from 130 nm down to 28 nm used standard planar CMOS, with the switch to FinFET based bulk CMOS technologies in 14 nm and 7 nm. The larger area in 14 nm and 7 nm also drives larger capacitance ESD devices as shown in Figure 21. Also shown in Figure 21, from 130 nm to 32 nm the capacitance increases a maximum 2X in 32 nm due to increased well doping to control FET short channel characteristics (device sized to meet 5.5 amperes using 1ns TLP failure current). However, as technologies moved to FinFET based on 14 nm and 7 nm this capacitance increase was 4-5X larger due to significantly less silicon volume in the same cross-sectional area compared to a 130 nm planar technology.

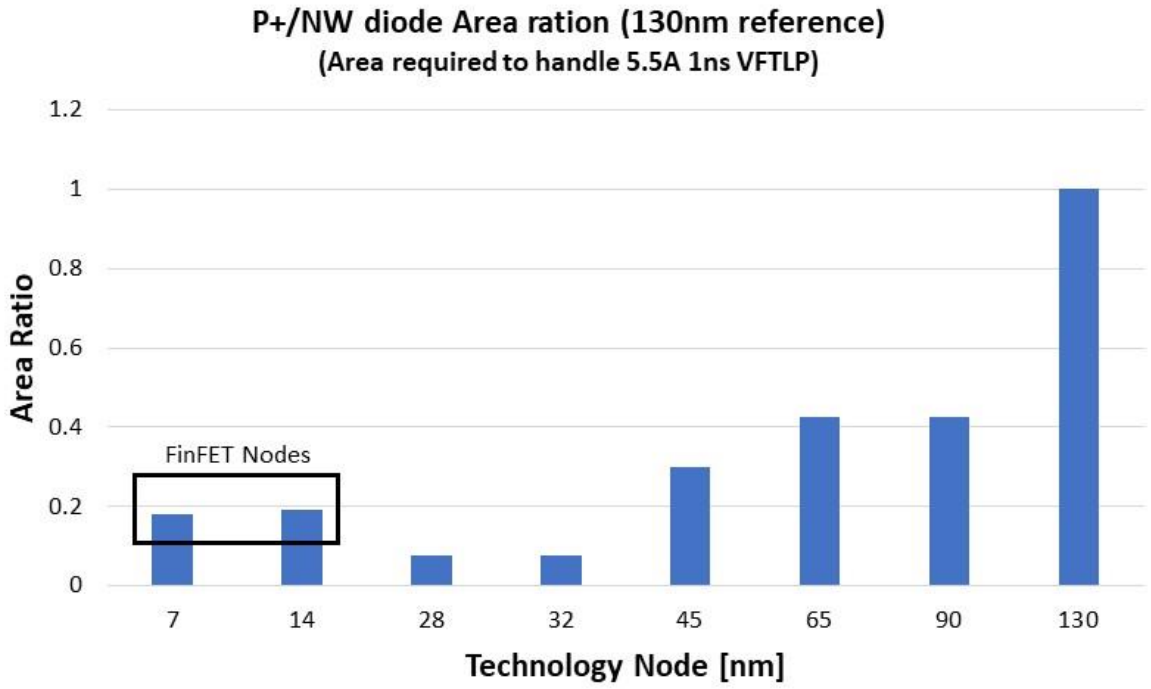


Figure 20: ESD diode area required to achieve a 1ns TLP 5.5 A failure current versus Technology Node (ratio values referenced to 130 nm)

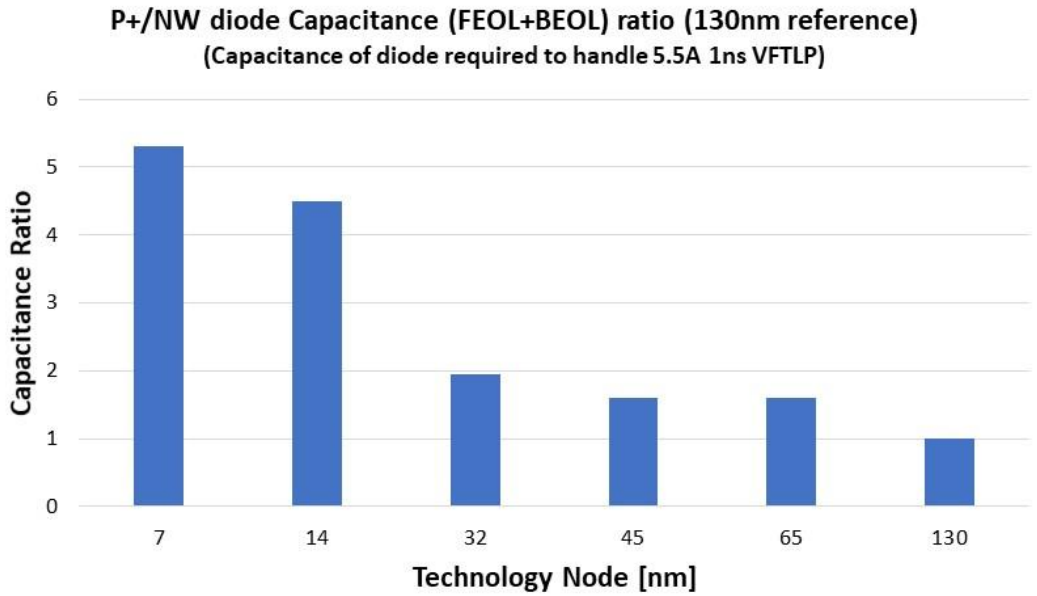


Figure 21: ESD diode capacitance vs. Technology Node (diode sized to achieve 1ns TLP 5.5A failure current) (ratio values referenced to 130 nm)

2.9.1 Data Rate/Frequency Scaling Challenges

As technologies continue to scale, so do the data rates/operation frequencies of various types of I/O interfaces. For example, if we refer to Figure 22 below, we can see the HSS link data rates have increased from ~10 Gb/s in 90 nm to ~112 Gb/s in 12 nm and to >200 Gb/s in 7 nm with continued data rate increases beyond 7 nm technology nodes expected. The data rates come from currently offered IP in the industry. From 90 nm down to 12 nm there has been greater than a 10X increase in data rates.

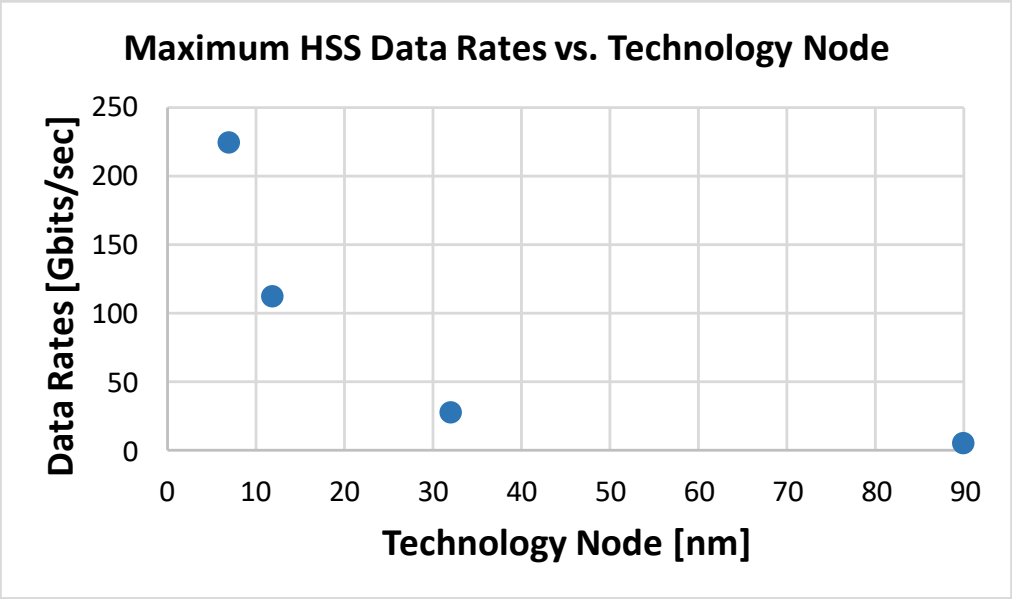
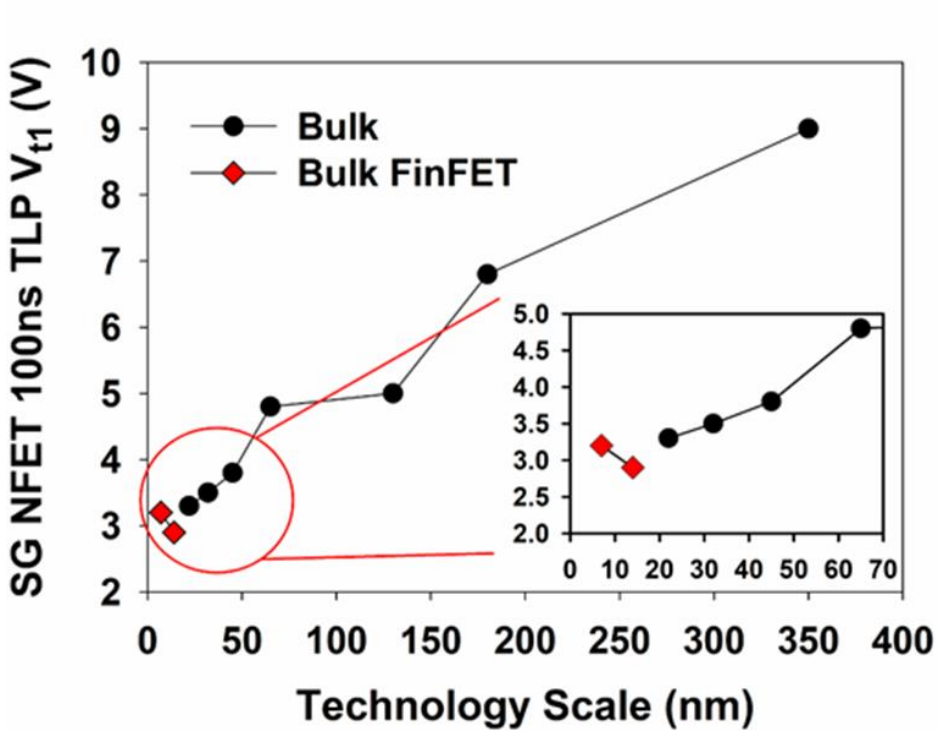


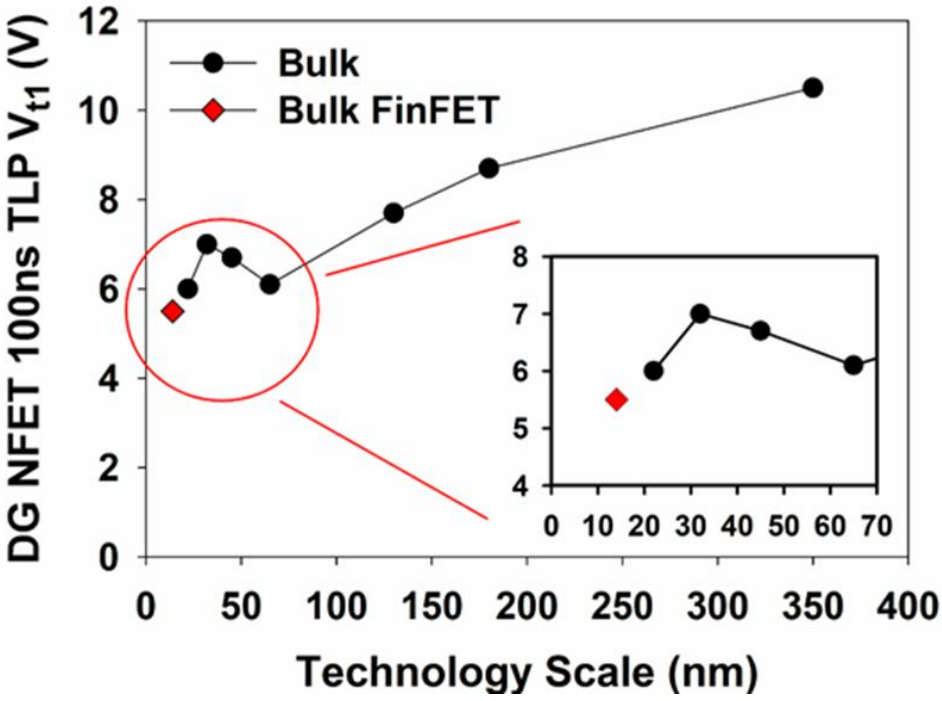
Figure 22: HSS data rate scaling versus technology node.

2.9.2 ESD Design Window Scaling as Technologies Scale

As bulk CMOS Technologies scale from 350 nm down to 7 nm thin-oxide (SG – single gate) NFET Vt1 reduces from ~9 volts down to ~2.8 volts reducing the design window by nearly 3X, this can be seen in Figure 23A. In the same technology generations, thick-oxide (DG – dual gate) NFET Vt1 reduces from ~10.5 volts down to ~5.5 volts, nearly a 2X reduction in the design window as shown in Figure 23B.



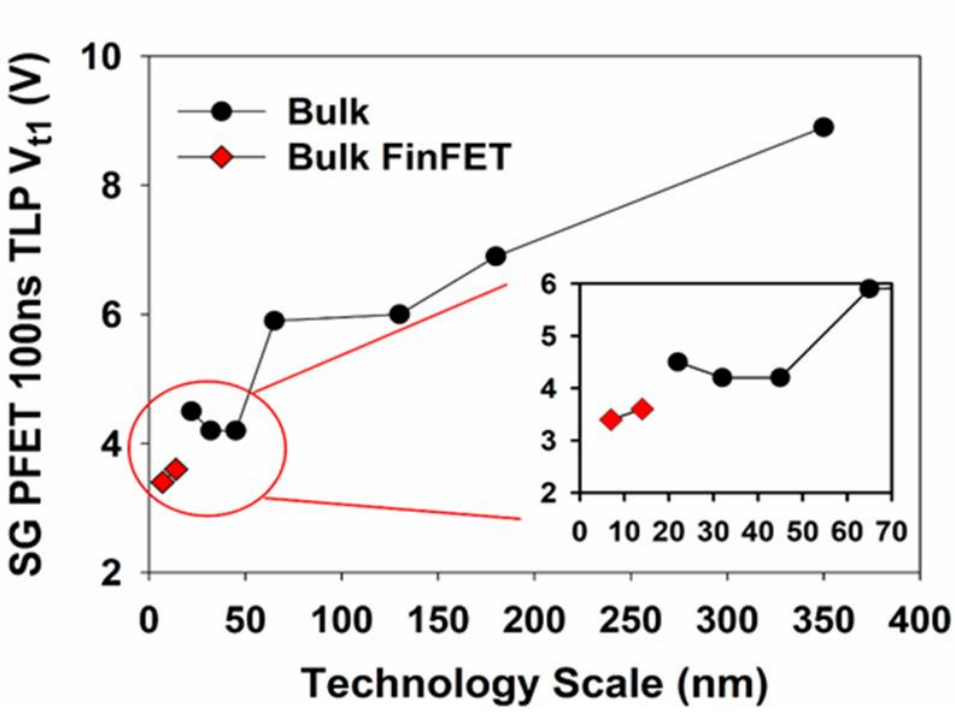
(A)



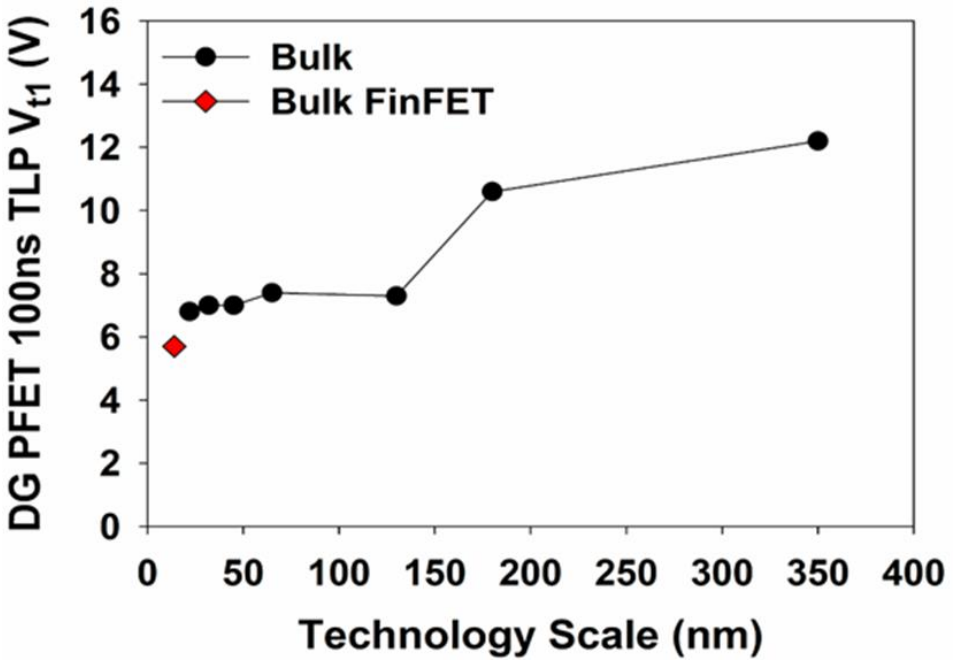
(B)

Figure 23: A) Thin-oxide (SG) NFET trigger voltage Vt1 vs. Technology Node B) Thick-oxide (DG) NFET trigger voltage Vt1 vs. Technology Node

For the thin oxide (SG) PFET the Vt1 reduction from 350 nm down to 7 nm is shown in Figure 24A where the Vt1 is shown to reduce from ~9 volts down to ~3.5 volts. In Figure 24B the Vt1 of the thick oxide (DG) PFET shows a reduction from ~12 volts down to ~5.8 volts.



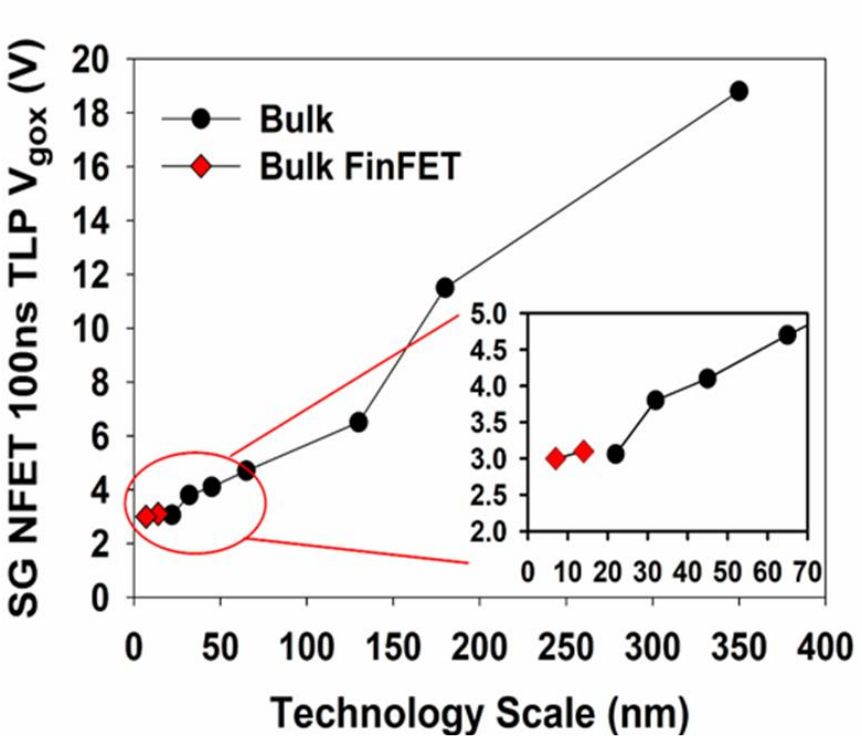
(A)



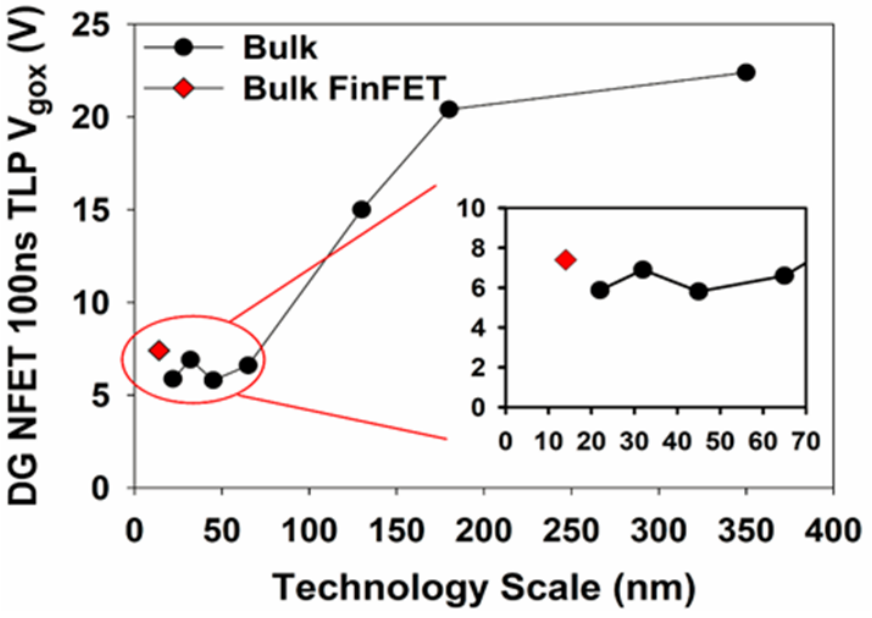
(B)

Figure 24: A) Thin-oxide (SG) PFET trigger voltage Vt1 vs. Technology Node B) Thick-oxide (DG) PFET trigger voltage vs. Technology Node

Figures 25A and 25B show the 100 ns TLP thin oxide and thick oxide NMOS breakdown voltages respectively under worst-case oxide breakdown gate biasing polarities. Figure 25A shows the thin-oxide (SG) NMOS 100 ns TLP breakdown voltages from 350 nm down to 7 nm is reduced from ~19 volts to ~2.8 volts. Figure 25B shows the same technology range but for the thick-oxide (DG) NMOS which reduces from ~22 volts down to ~6 volts.



(A)



(B)

Figure 25: A) Thin oxide (SG) NFET 100 ns TLP Oxide Failure Voltage (Vgox) vs. Technology Node B) Thick oxide (DG) NFET 100 ns TLP Oxide Failure Voltage (Vgox) vs. Technology Node

2.9.3 Estimation of What CDM Targets Designs Can Handle for High-Speed Interfaces in 7 nm and beyond

The worst-case scenario is a large package IC using thin-oxide I/Os where the high-speed performance doesn't allow for series resistors and secondary ESD protection. In a simple diode-based and RC-Clamp ESD architecture and assuming a bussing resistance of 0.1 Ω (very aggressive) we can come up with a rough estimation of the amount of current during a CDM event these I/O interfaces can withstand without reaching failure. Consider the CDM current path depicted in Figure 26.

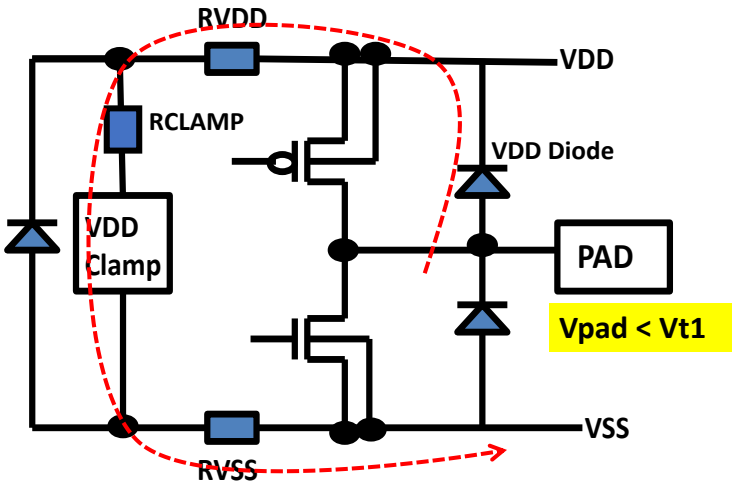


Figure 26: Rail clamp design where for a given CDM discharge current the voltage buildup at the pad (Vpad) must be lower than Vt1 to protect the output buffer device.

Assumptions (worst-case 7 nm design):
Vdiode_on = 1.0 volt
Rdiode_on = 0.2 Ω
RVdd_buss=0.1 Ω
RVss_buss=0.1 Ω
Vrcclamp_on = 0.5 volts
Rrcclamp_on= 0.1 Ω
Rseries_IO= 0 Ω
Vt1_thinox_7 nm= 3.2 volts (note: device fails at the trigger point of Vt1)
Large package giving CDM current of 2 amperes / 100 volts

- Vpad = Vdiode_on + (Rdiode_on * Icdm) + ((RVdd_buss + RVss_buss) * Icdm) + Vrcclamp_on + (Rrcclamp_on * Icdm) where Vpad in this example must be ≤ 3.2 volts
- 3.2 volts = 1.0 volt + (0.2 Ω * Icdm) + (0.2 Ω * Icdm) + 0.5 volts + (0.1 Ω * Icdm).
- Icdm = 3.4 amperes which leads to Vcdm = (3.4 amperes/2 amperes) * 100 volts = 170 volts (best case)

Based on a large package that gives 2 amperes per 100 volts of CDM voltage, using very aggressive on-resistances for RC_clamp, RVdd_buss, and RVss_buss which are all at 0.1 Ω (the best-case

scenario), the best we can achieve is a 170 volt CDM target level. Given that we should include some margin (~10 %), a realistic CDM target is 125-150 volts for high speed/RF interfaces in 7 nm and lower technology nodes.

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Chapter 3: CDM Related ESD Process Assessment

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Wolfgang Stadler, Intel Corporation

3.1 Motivation

The ESD robustness of semiconductor devices against discharges according to the human body model (HBM) and against discharges of isolated conductors is continuously trending to lower values [1]. There is a general concern by many companies that they cannot handle these sensitive devices. However, if ESD-protective measures in the assembly lines are set up according to international standards such as ANSI/ESD S20.20 [2], IEC 61340-5-1 [3], or JEDEC JESD625 [4], these devices can be handled without any adverse effects from HBM (see also [5]). The current editions of both standards are reasonably well aligned and provide rules for the safe handling of "electrical or electronic parts, assemblies and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volt human body model and 35 volts on isolated conductors" (taken from ANSI/ESD S20.20).

The Industry Council on ESD Target Levels recommends HBM target levels of 1000 volts for products [5]. Typically, this HBM target is met if a certain level of charged device model (CDM) robustness is designed into the product. Therefore, one does not have to expect ESD failures related to the human body and isolated conductors if an ESD program is implemented that follows one of the above referenced international standards.

However, these hazards are only two of the risks that can be found on an assembly line. It is also necessary to prevent the charging by triboelectricity or induction and subsequent "hard" grounding of electrostatic discharge sensitive (ESDS) items, resulting in a CDM-type ESD event. For integrated circuits, ANSI/ESD S20.20 and IEC 61340-5-1 require a CDM-robustness of 200 volts or greater to allow safe handling, leaving little margin to the recommended target of 250 volts as recommended in the 2012 version of White Paper 2 of Industry Council on ESD Target Levels [6].

The EOS/ESD Association's Technology Roadmap for Semiconductors provides a trend chart for CDM robustness [1]. There are more and more products for which the CDM robustness will fall below the 200-volt limit and, hence, will require additional ESD control measures.

What do international standards require to avoid CDM-like ESD hazards? Many of the basic ESD protection measures for HBM protection also protect against CDM-related problems, although they would not be called special CDM protection measures. Examples of these are wrist straps or dissipative table mats. If an operator is not grounded, he can induce a charge on a device or PCB without directly damaging it by a discharge when contacting the ESDS item. But when the device or PCB in the electrostatic field of the charged operator is placed on a metal surface, it could be damaged by a CDM-type discharge. On the other side, a grounded dissipative table mat avoids dangerous potential differences between various items in the production area, and, thus, reduces the risk of damage in the case of a hard discharge of the charged ESDS item. It is therefore also a CDM protection measure. Many examples like these can be found. The situation is summarized in Figure 27, which shows that basic CDM protection is already part of the basic ESD protection process that is in place in most EPAs worldwide.

Additional to the "inherent" CDM protection measures which primarily address HBM risks, international standards require the removal of non-essential insulators that can become highly charged and require a strategy on how to handle process required insulators as a CDM-specific ESD control measure. The limits set for electrostatic fields of the charged insulator at the location where the ESDS item is handled or the surface potential of the process required insulators are said to allow safe handling of ESDS devices with a CDM robustness of 200 volts or greater [2,3].

However, with a continuously increasing number of devices with at least some pins falling below this limit, following the requirements of both ESD control standards might not be enough to prevent ESD damage. Detailed process analysis must be conducted to assess the ESD risk in the process and determine the most efficient mitigation techniques. Such an ESD process risk assessment requires personnel with advanced knowledge and experience with electrostatic measurements and advanced measurement technologies. Assessment of any risk induced by a charged ESDS item or electrostatic field is briefly explained in this document in the following sections by some examples. Section 3.2 describes the ESD process assessment flow based on the basic ideas of charging and hard discharges. Several successful approaches to CDM-like process risk assessment and risk mitigation have been published and will be discussed in Section 3.2.2 after a brief introduction to the systematic approach of the basic ESD assessment flow. Section 3.3 discusses the approach of process capability and transition analysis. The case studies give the end-user good examples and ideas of a systematic approach. This includes how to analyze a CDM-like risk or the process capability of the respective production line and how a process can be analyzed to avoid CDM-like failures. Section 3.4 describes the approach for an ESD process assessment based on ANSI/ESD SP17.1 [7])

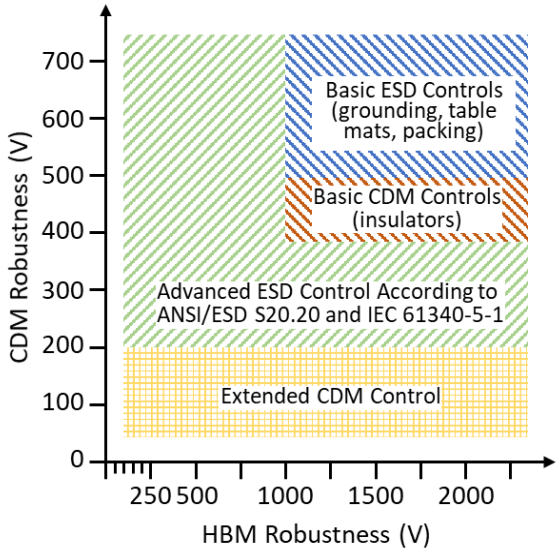

Figure 27: Relationship Between General ESD Control and CDM Specific Control
Note: Robustness levels are for rough guidance only

3.2 Basic Idea of CDM Protection and Process Related Risk Analysis

Many processes, particularly in assembly and test, cause charging of the ESDS item to take place, either by triboelectric charging of the ESDS item or by charging by induction of the ESDS item in

an electrostatic field of a near-by process required insulator. However, charging the ESDS item itself is not critical as it will not result in damage to the ESDS item. In many process steps, charging either by a triboelectric effect or induction cannot be avoided. “Hard” discharges of the ESDS item must be avoided in each process step. A hard discharge is a discharge through a low ohmic contact; it is the most severe discharge as compared to a discharge through a higher resistance contact (see definition in ANSI/ESD SP17.1 [7]).

There are several possible ways to analyze a CDM-like risk (see, for example [8-10]). The very basic idea of this approach is shown in Figure 28.

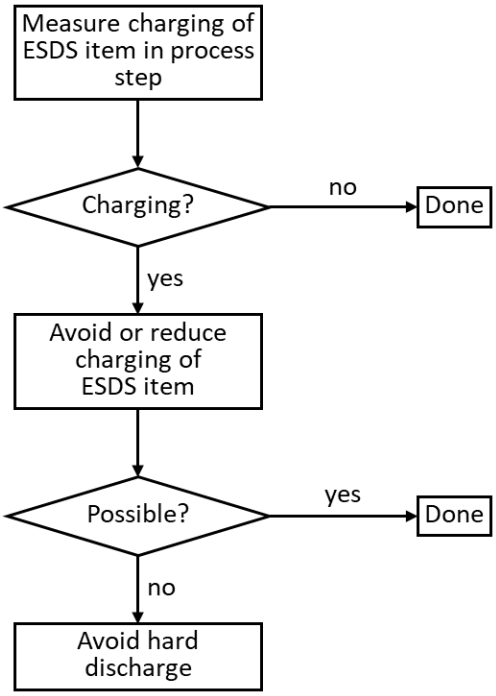

Figure 28: Basic ESD Assessment Flow for CDM-like Risks

3.2.1 Systematic Approach

While investigating device and PCB charging, it must also be considered whether these charging values are dangerous for the ESDS item. That means, it must be determined whether the charged ESDS item experiences a low ohmic contact to ground or contacts another conductive object at a different potential. Both scenarios are a hard discharge that can cause a dangerous CDM-type event. If that is not the case, the charging will normally not cause any damage to the object – electrostatic problems like the attraction of particles by charged objects will not be discussed here.

These considerations result in an analysis of every single process step by asking the following questions:

- Is there charging of the object being processed?
- Is there a chance for a hard discharge in this or the next process step?

If there is no charging, there is consequently no possibility for a hard discharge. If there is no hard discharge, there is normally no possibility of CDM damage.

3.2.2 Theoretical approach

The approach will be explained in some simple examples that can happen in a typical PCB assembly line [8]:

1) An uncharged PCB is transported on a conveyor belt from process step A to process step B in a closed tunnel. In order to be able to view inside the tunnel, the cover is made of a transparent material. To keep costs low the cover is made of insulative, highly chargeable Plexiglas. While the (initially neutral) PCB is running underneath the highly charged Plexiglas, the electrostatic field of the Plexiglas results in a charge separation on the conductors of the PCB. This is by itself not damaging the PCB! If the PCB exits out of the charged transport tunnel without having experienced a metallic contact (or an arc to a nearby piece of metal), the charges recombine, and a neutral undamaged PCB arrives at the next process step.

   NOTE: The use of a grounded, dissipative cover prevents the charging of the cover and therefore avoids the field-induced charge separation on the PCB. This makes the risk analysis much easier but is not absolutely necessary.

2) The same uncharged PCB now comes to a process step where it becomes charged. A possible example is when a charged barcode label is attached to the PCB, or when the PCB is held in place by a bar or stop at the end of a conveyor while the conveyor belt continues to run and charges up the PCB by rubbing (tribocharging). Such processes can charge the PCB to several hundred volts. If the metal parts of the PCB, for example, connectors or metal lines, are not contacted by or are not coming close to a grounded conductive object, there is no risk for a hard discharge or arc and the process step can be considered “safe”, independent of the charging. Additionally, it is necessary to determine what happens to the PCB in the follow-on process steps. If the PCB comes to a process step where it discharges slowly and in a controlled way, for example, by the temperature at reflow soldering or by the relative humidity while stored in a magazine, no further risk mitigation measures are necessary. If the charged PCB is going directly to a process where it contacts another conductor (for example, at testing), the charge must be drained off before the first contact happens, by using ionization for example.

3) The same uncharged PCB now comes to a process step, where it is charged during the process and contacted immediately afterward. It is possible that a hard discharge can happen immediately after the charging event. In this case, there is a clear risk for a CDM-like ESD event. A typical example of this is the in-circuit test (ICT). The PCB is pressed down by plastic pins, made very often of highly chargeable material. This charging is transferred to the PCB by induction. During the electrical measurement, the PCB is contacted with metallic pogo-pins and a hard discharge from the PCB into the tester can occur.

   NOTE: Very critical during such “closed” process steps is the fact that the problem can be overlooked very easily since the PCB is not charged before and after the process but can nevertheless be damaged during the process.

Table II shows possible ESD risks during different process steps in a typical assembly line for PCBs or control units. It also gives an overview of the risk during standard process steps and additionally shows how to perform a process-related risk analysis.

An example of how Table II can be used is explained here, using the process step "placement of ESDS item" onto the PCB (ESDS = ESD sensitive). Two different ESD risks can occur:

i. The PCB can get charged during the process step before and discharges into the ESDS item. This can be especially risky if a lot of other components are already placed onto the PCB as the capacitance of the PCB is increased.
ii. The ESDS item gets charged because an ungrounded or insulative pick-up tool (for example, a suction cup) is used for picking and placing and the charged ESDS item discharges into the PCB.

In both cases, the charging voltage should be measured using an electrostatic voltmeter.

- For case i), the PCB should be measured to determine whether the board, especially whether the metal lines on the boards are charged. If the charging voltage is too high it should be reduced, by using an ionizer for example.
- For case ii), it would be best to measure the charging of the device while it is hanging on the suction cup. If that is not possible during assembly, the charging of the bare suction cup in a "park" position can be measured and the charging of a device needs to be derived from this measurement. If that is also not possible, at least the resistance to ground of the suction cup should be measured.

If the charging voltage is too high, the use of a dissipative and grounded suction cup may improve the situation. Additionally, an ionizer might be necessary.

For the rest of the process steps described in Table II (and of course also for those not described there), the CDM related ESD risk analysis always must be performed in the same way:

- Check whether there is a high charging of the devices or the PCB
- Check whether there is a risk for a hard discharge of the charged device or PCB

It is best to do such a process-related risk analysis together with the respective process engineer since they should be able to explain how the process is really running and should also be able to run the process in a single step mode (if necessary). This allows completing all the necessary measurements in a "real-life" situation.

Table II: Possible ESD Risk in Typical PCB Assembly Process Steps

Process Step	Possible Risk	Test Method	Mitigation
Placement of non-ESDS item (for example, resistor, capacitor …)	The board can get charged during placement since a lot of non-ESDS items are sent in highly chargeable packing materials	Measure the charging of the board using an electrostatic voltmeter	Install an ionizer after placement of the non-ESDS item
Placement of ESDS item (discrete devices and ICs)	i) The board is charged due to the process steps before and discharges into the ESDS item	Measure the charging of the board using an electrostatic voltmeter	Install an ionizer before placement of the ESDS item (application-specific limit)
	ii) The ESDS item gets charged due to the use of ungrounded or insulative suction cups at pick and place and discharges into the board	a) Measure the charging of the IC while it is hanging on the suction cup Measure the charging of the suction cup b) Measure the resistance to ground of the suction cup	Use conductive/dissipative suction cups, that are grounded. If necessary, use an ionizer to reduce the charging
Reflow soldering	No risk, if there is no metallic contact to pins; charging is decreased due to higher temperature		
In-circuit test (ICT)	Downholder pins and/or (transparent) cover of the ICT are often made of highly chargeable materials; especially the downholder pins can be very close to the sensitive pins of the ESDS item and induce charges on the ESDS item; during the contact of the pogo pins from underneath a hard discharge can occur (CDM-like event)	Measure the charging of the board using an electrostatic voltmeter	Use dissipative materials for downholder pins and/or plastic cover and ground them. Use two-stage pogo-pins.
Final testing	Depending on the way the testing is performed, charging of the board can happen followed by a hard discharge into the tester	Measure the charging of the board using an electrostatic voltmeter	Avoid the charging by using ionizers or other appropriate measures (depending on the actual process)
Rework stations	Normal ESD risk by operators or by ungrounded tools (including soldering iron). Device storage boxes are often made of non-dissipative material.	Measure the charging of the board/operator using an electrostatic voltmeter	Use ESD protective materials and ground them (incl. soldering tip (limit < 1 MΩ))
Internal transport and packing (especially after final test)	Risk of charging using non-dissipative packing materials. Normal handling risk during packing.	Check packing materials (measure charging or resistance). Check handling procedure	

3.2.3 Field Examples

Recent experience has shown that real CDM failures, which are failures created by a hard discharge of the device with resulting failure modes similar to those found during qualification testing, happen mainly during semiconductor manufacturing, assembly, and testing. However, CDM and CDM-like failures happen outside semiconductor manufacturing processes as well. For example, CDM failures can happen in printed circuit board (PCB) assembly operations. Failures due to so-called charged board events can occur when a complete PCB (or part of it) is charged and subsequently hard discharged. CDM-like failures may result in different, more intense, failure modes. However, situations of CDM-like failures can be related to CDM events, and the techniques used to control either failure type within any manufacturing or handling process are the same.

Four examples of CDM and CDM-like failures will be discussed in the following sections.

3.2.3.1 CDM failure during automated semiconductor testing

Figure 29 shows the failure rate trend of a device in a BGA-293 package. The device had a CDM robustness of 250 volts and analysis indicated that the failing devices had a CDM-like failure signature. The device shows a high percentage of fallout in the ramp-up phase for this new product at the IC supplier's test site.

Upon analysis, the failure signature of these devices was the same as those found on failed devices during CDM qualification testing. The root cause of the failure was the high charging of the device during testing (up to 1000 volts), induced by an insulative nest that supports the mold compound on the backside of the device. The problem was discovered in an assessment of the handling process and the problem was solved by a minor but effective improvement in the test handling (dissipative support materials) which immediately restored a safe manufacturing environment. It was not necessary to redesign the device. It was manufactured and shipped without any further problems in manufacturing or the field.

Occasional problems during the ramp-up phase due to specific handling steps have been encountered for devices having a wide range of CDM robustness (even above 1000 volts).

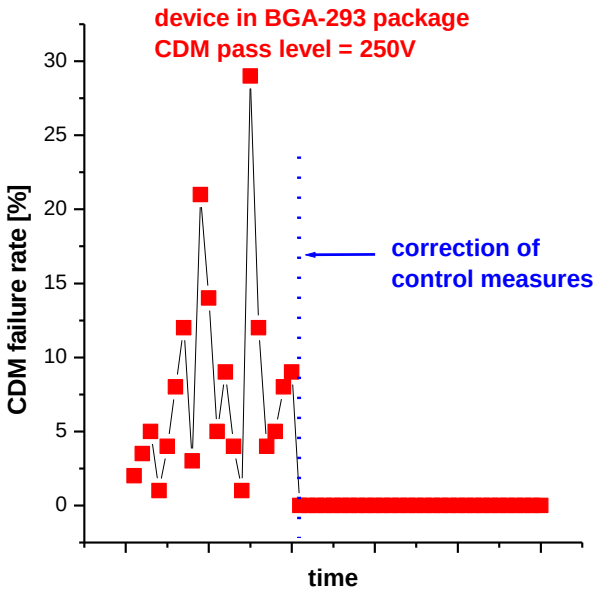

Figure 29: CDM-Type Failures Occasionally Occurring During Ramp-up of New Products.
Note: After correcting the CDM control measures, safe manufacturing was regained, and no further problems appeared.

3.2.3.2 CDM-like failure during manual semiconductor testing

In a semiconductor backend, failures of an ESDS device in a ceramic PGA package occurred. The "normal" ESD protective measures like operator grounding have been installed and verified on a regular basis. After a detailed analysis of all process steps [9], the testing process was determined to be the root cause for the fails. During the manual loading/unloading of the device for testing, the ZIF-socket had to be opened and closed very often. By doing this, plastic parts of the sockets rubbed against each other and charged the socket to more than 1000 volts. The electrostatic field generated by the charged socket was transferred to the device by induction, resulting in a charge separation inside the device. When the socket was closed completely by closing the lever, the charged pins of the device were pressed into the contact springs of the tester which resulted in a hard discharge.

NOTE: The problem could be solved by using an antistatic spray at the beginning of each shift, which dramatically reduced the charging.

3.2.3.3 CBE failure in an assembly line for automotive control units

A device with a CDM robustness of >500 volts, which was used in the control unit of an air conditioning system of a car, showed CDM-like fails during assembly of the PCB, after assembly into the car ("0 km"), and in the field (at the end-user). In all cases, the gate oxide of a transistor was damaged [11].

The normal ESD protective measures – like the grounding of operators or tables, internal transport boxes, etc. – have not been perfect, but this could not explain the observed systematic failure. A process-related risk analysis, performed using Table II, did not lead to findings during the first assembly steps like placement, soldering, or ICT. For the second test step, the metallic fixture,

which holds ten PCBs, had to be lifted in an isolated way for the measurement. By performing charging voltage measurements using an electrostatic voltmeter it could be shown that the fixture, and with it all 10 PCBs that have been metallically connected via the heat sinks to the fixture, were charged to several hundred volts. For the electrical testing, the PCB was contacted by a (metallic) pogo pin of the tester directly at the gate of the transistor resulting in a hard discharge of all ten PCBs. Depending on the charging voltage and the respective discharge current the failure could be detected immediately, at 0 km, or – worst case – only later in the field.

During the analysis of this process step, a corrective action could be defined together with the respective process engineer, which did not disturb the performance of the process. The fixture was grounded via a 10 MΩ resistance, which was sufficiently high to "isolate" during testing, but low enough to avoid the charging of the fixture during lifting.

A detailed analysis was required in this case because the PCB was electrically neutral before and after the process step of electrical testing.

3.2.3.4 CBE failure in a mobile phone production line

A mixed-signal device was used on a PCB for a mobile phone and showed a high failure rate during production. The "normal" ESD protective measures like operator grounding, grounding of work surfaces, and the use of ESD protective packing were analyzed and improved but these measures did not solve the problem. A process-related risk analysis was performed to find the root cause of the failures. It was enough to check the process steps from the placement of the IC to the first measurement where the damage was detected. After excluding the processes of placement, reflow soldering, and the testing itself, the failure must have happened between reflow soldering and testing. The only process steps in between were the placement of a barcode label onto the finished PCB and pressing the PCB out of the metallic fixture (used for mechanically fixing the PCBs for placement).

The analysis of possible charging and discharging events showed that the PCB was charged to several hundred volts during the automatic placement of the insulative barcode label. The charging was not the root cause for the damage (proved by electrical re-tests directly after charging and softly discharging). However, when the PCB was pressed out of the fixture with grounded metallic needles, the needles contacted printed leads on the PCB, which were directly connected to the damaged pins of the mixed-signal device (see Figure 30).

The contact resulted in a hard discharge which damaged the device. This was experimentally verified in the assembly line by charging (applying several charged barcode labels), discharging, and immediate electrical re-test.

NOTE: It would not have been possible to find the root cause of the failure without implementing the "normal" ESD protective measures before doing the process-related risk analysis.

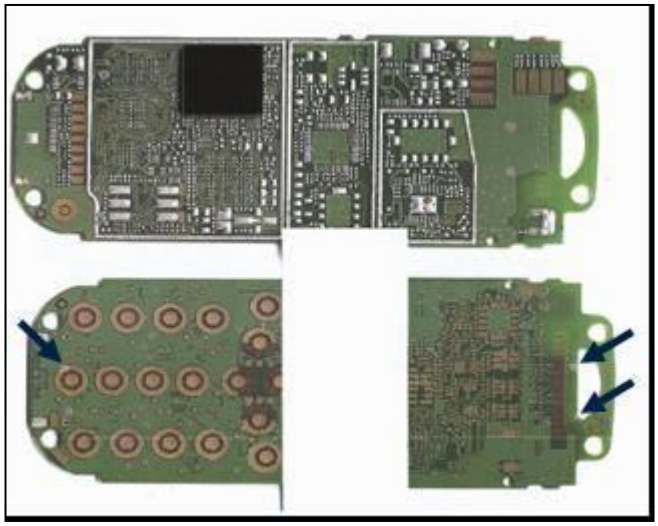

Figure 30: Arrows are Showing Where the Metallic Needles Contacted Printed Metal Lines on the PCB

3.3 Process Capability & Transition Analysis

While the risk analysis presented in Section 3.2 focuses on a single process, not considering where the charging possibly comes from, the process capability and transition analysis (PCTA) looks at the process in total and analyzes whether there is charging at all that theoretically could result in a discharge during process deviations. Additionally, it looks at CDM, HBM, and MM related problems as well as transitions between process steps. A detailed description can be found in [10]. It includes the following:

1) Defining the process critical path, identifying key process elements and their transition points
2) Making transition point measurements
3) Summarizing findings

3.3.1 Defining the Process Critical Path

The critical path may be defined as a series of tasks (for example, cleaning, screening, parts addition), each of which must be completed in order to finish a product. In the following example, the process critical path starts at Receiving and ends at Shipping.

Tasks fall into two categories:

- A process function (this related to all assembly and test operations)
- Movement, that is transport, from one task to another.

Process Transition Points occur when the product undergoes a change in the process (that means a board changes from a manual transport operation to placement on the screening conveyor). Transition points are possible sources for ESD events that require special attention during process analysis.

Figure 31 illustrates a basic process that was studied for PCTA and consists of human transport and automated equipment tasks. The process includes:

1) A board screening operation
2) Parts installation
3) Reflow

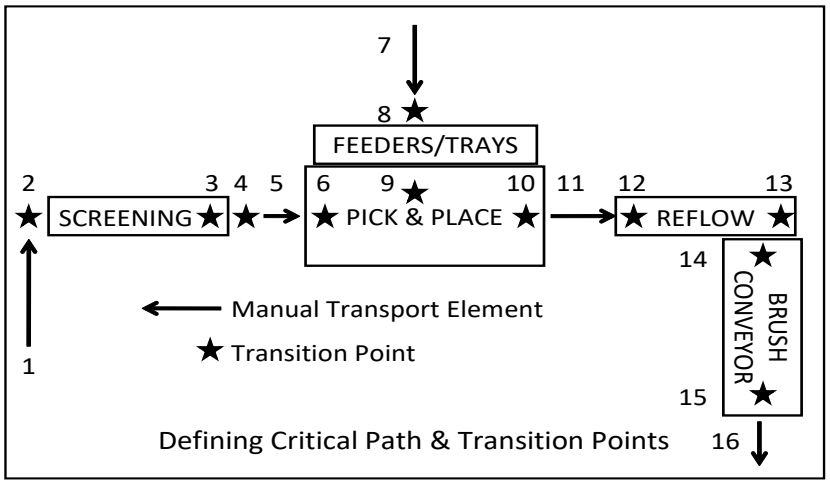

Figure 31: Characterizing the Critical Path and Identifying Transition Points

Detailed analysis of Figure 31's critical path reveals the following transition points.

1) Manual Transport of bare boards to Screener
2) Manual Load Screener
3) Screener Applies Solder Paste
4) Boards Manually unloaded & Inspected
5) Screened boards Manually Transported to Pick & Place/SMT equipment
6) Boards Manually Loaded into placement equipment
7) Devices Manually transported to Feeder
8) Devices Manually Loaded into Feeder
9) Devices Automatically transported from Feeder and installed on boards
10) Boards Manually unloaded from Pick & Place equipment and inspected
11) Boards Manually Transported to Reflow
12) Boards Manually loaded onto Reflow Conveyor
13) Boards Automatically Transported through Reflow
14) Boards Brush Conveyed from Reflow outlet
15) Boards Accumulate at end of Reflow Brush Conveyor
16) Boards Manually Removed

Once all process steps are described the next step in PCTA is the measurement of the critical Transition Points.

3.3.2 Transition Point Measurements

The objective of transition point measurements is to assess that portion of the process for conditions that would create HBM, CDM, or MM events. Then quantify the potential magnitude of those ESD events as they relate to the ESDS device sensitivity thresholds, even if the numbers are not comparable directly.

The measurement may not reveal that an ESD event is taking place at that transition point. Rather, it may show that an assembly is being charged at that specific point in the process, only to discharge some later time. It would also indicate how the assembly is being charged. Proper analysis will provide the probable type of ESD event the assembly will see when and if a discharge occurs.

To this end, measurements include:

1) The electrostatic voltage or charge condition of ESDS devices or subassemblies:
   a. Before a transitional element
   b. After the transitional element
   c. In some cases, during transitional element
2) The electrostatic voltage or charge conditions and resistance to ground of equipment, personnel, operational surfaces, and materials
   a. Making direct contact with ESDS devices and assemblies, or
   b. Producing electrostatic fields near or in the process flow, and at transition points
3) Identifying the charged device or object's discharge waveform

In [10] a detailed description of the new and traditional measurements to analyze all sorts of ESD risks is given. In this section, the focus is on the contribution

- of human charging to later CDM events
- of material handling devices and aids, e.g., device trays, totes, tape and reel, etc., for potential charge transfer to ESDS devices
- ESDS, subassemblies, and their connectors to potential CDM events
- field measurements in the critical path and inside automated equipment for FIM (field-induced model) assessment

3.3.3 Performing a Process Capability & Transitional Analysis

The Figure 31 process case study illustration consists of

- Five personnel transport and handling transition points
- Screening solder paste onto circuit boards
- Loading the feeder
- Placing parts on circuit boards in the Pick & Place equipment
- Reflow

The first task where the board can get charged is the screening operation, which consists of the following key transition points:

- The operator loads boards by hand into the screener
- The operator removes the boards after screening for inspection
- Parts are manually transported to Pick & Place (SMT)

A high impedance contact voltmeter was used to measure the voltage on the board conductors before and after the screening processes (Figure 32). The voltage before screening was less than 20 volts. After screening more than 440 volts were measured on the board's conductive elements.

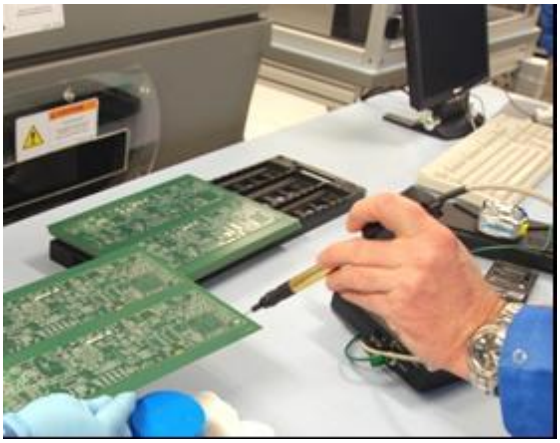

Figure 32: Measuring PC Conductor with High-Impedance Contact Voltmeter

Screening summary indicates:

- The screening process charges the board's conductive elements to >440 volts
- The charge poses a possible ESD CDM discharge source during subsequent handling or device placement if the charge is not removed
- In the illustration study, an ionizer was recommended to eliminate board voltage to reduce discharge risk later in the process

Pick & Place (SMT) Process:

At the SMT process several items require evaluation:

- Device trays, tape and reel supplied to placement equipment.
  - Are these parts charged by the materials or process creating a potential CDM event later on?
- Does the placement equipment charge the parts before placement on the board?
- Are there insulators in the process that may induce a charge on the device or PCB during placement?

Consequently, this portion of the process must be broken into two parts: Analysis of the Feeder transition points and analysis of the placement equipment

Feeder Transition Point Analysis:

The Feeder is loaded with devices that are manually transported to, and then mounted in, the Feeder for delivery to the SMT equipment. Once loaded, trays and individual devices were measured with the contact voltmeter to determine the existing voltage caused by transport that may not have dissipated after mounting in the Feeder.

Placement Transition Point Analysis:

The placement analysis of the Pick & Place process description includes:

- Screened boards placed by hand into the machine.
- The conveyor moves the board into position
- The machine picks up the IC and other devices and places them onto the board
- The conveyor moves the board to the machine exit

The placement concerns include the following potential ESD issues:

- Static generators near placement (FIM)
- Isolated charged placement nozzles and other conductive objects (MM)
- Parts charged from pick up process
- Note that we previously measured the Feeder process to see if parts are charged before pickup.
- Discharge from a charged device to conductive solder paste or socket (CDM)

Equivalent Field Voltage Measurement Considerations:

To assess the SMT equipment for electrostatic fields that may emanate from machine guards, plastic windows, pneumatic lines, and other auxiliary materials, a special carrier (Figure 33), resembling a circuit board, can be used.

The carrier is approximately 21.6 cm × 27.9 cm (8.5 inches × 11.0 inches) and serves as transport for a portable CPM (charge plate monitor) and battery-operated recording device. The carrier is transported through the machine by the conveyor system, the CPM measures the field and the recording device saves the data for later viewing.

The CPM plate is 15.6 pF and will see induced voltages differently than a device. A concern is relating the measured voltages to the device sensitivity and size (capacitance) of the device. In one approach we consider the 15.6 pF plate at the midpoint of ANSI/ESD STM 5.2 CDM standard calibration references of 4 and 30 pF. However, these values do not reflect device capacitance; they are simply a reference. Actual measurements of the internal SMT equipment voltages using this special CPM were less than 12 volts.

Figure 33: Instrument Carrier with Portable CPM and Recording Device

CDM Measurement Options:
Two options are apparent for measuring potential CDM problems in the SMT equipment.

One option is to program equipment to pick up a critical device and stop the placement of the device well above-board placement. Then measure the device conductors with a contact voltmeter and compare measured voltage to the ESDS device's CDM damage threshold.

The second option uses the above carrier with a portable CPM and recorder positioned at the point of device placement. Here the device is placed onto the CPM by the programmed placement equipment (Figure 34). Any device voltage is shared with the CPM and stored in the recorder's memory for later analysis.

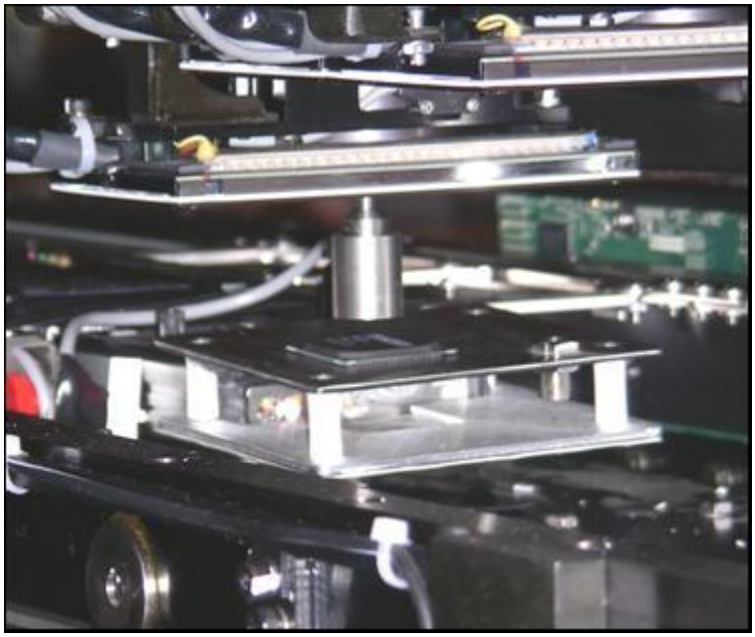

Figure 34: Device Charge Sharing Measurements with Portable CPM

The Feeder and SMT equipment analysis summary indicates:
- The feeder and the trays are properly grounded, and the parts are not charged
- Electrostatic fields are not a concern. <50 volts were measured on the CPM
- Tribocharging or voltage induction of devices due to IC handling is not a concern <50 volts measured on the CPM at device contact

In the illustrative case study, the bare circuit board was charged to >440 volts at the screener. The board was not discharged and was transported by a non-charge generating person to the SMT equipment still having >350 volts on the board. At SMT output, the board voltage was >290 volts when it was transported to Reflow.

Reflow Process:
The reflow process includes
- Boards manually loaded onto the metal conveyor
  - Note that boards in the illustration study remained charged >200 volts

- The system includes a metal wire conveyor grounded to the machine frame
- Primary concern: Are discharges occurring between charged boards and grounded metal conveyor?

- Conveyor system collects boards after reflow completed

Board Loading:

Measuring board voltage with a contact voltmeter prior to, and after placement onto a conductive surface will indicate:

- If an ESDS assembly discharges upon contact (CDM)
- If the assembly becomes charged by the conductor upon contact (MM)

Reflow Accumulation Conveyor:

In the illustration study, the board exited Reflow with <10 volts on its conductors, then transitioned to a rotating brush conveyor (Figure 35). The board was transported to the end of the conveyor. The brush conveying system operates on an adjustable friction basis. If a board is stopped, friction increases and the brush stops turning, assuming it is properly adjusted. In the illustration study, the brushes continued to turn, generating >525 volts on the boards awaiting manual transport to Cleaning and Testing.

Figure 35: Uncontrolled Brushes Generate > 500 V on PCBs

Reflow analysis summary indicates

- Discharges detected at the loading of the reflow conveyor
  - The board was charged to 200 volts before entering the reflow conveyor
  - Blow ionized air across the board before moving to reflow to resolve
- Conveyor at the exit of the reflow, charging boards to >500 volts.
  - Possible discharge to grounded operators or at the next process step
  - Change conveyor system or add ionization post reflow

Summarizing Process Capability & Transition Analysis Results:
A basic summary illustrating the PCTA study (Table III) indicates problem areas, voltage measurements, type of potential discharge events, and whether the process is within specification.

Table III: Process Analysis Summary of PCTA Illustration Study

Process Step	Input Voltage (V)	Output Voltage (V)	ESD Model	Within Spec?
Screener	40	268 – 441	CDM	NO
SMT Placement	216	95 – 200*	CDM/MM	NO
SMT Feeder	~0	<50	CDM	YES
Reflow	>200	>500	CDM	NO

*NOTE: Residual voltage from Screener Operations

3.3.4 Example of CDM-like Failure on the System Level

Large controllers for hard drive data centers have many features and options that allow customers to configure what they need. In order to allow for a customizable solution, the controller had to be flexible. This was accomplished by selectively plugging in PCB depending on the configuration ordered.

However, this did require the use of dummy PCBs when the features were not required to ensure that the airflow still allowed for the correct cooling of the remaining PCBs. These dummy PCB were made of an insulating plastic material without any regard to ESD requirements. These plastic PCBs were found to generate large electric fields. When using a field meter, the readings could be as high as 10,000 volts/inch. The process at the time was to plug the dummy PCBs first and then the active logic PCBs. This caused a voltage to be induced in the logic PCBs and the first pin that made contact would take the biggest discharge. This resulted in a failure rate of up to 5% at the functional test level.

Two fixes were put in place. The first fix was very simple. Change the order of plugging so that the logic would be plugged before the dummy PCBs. The long-term fix was to find a material that was static dissipative.

The result of the change in the process resulted in the elimination of CDM-type failures. The long-term fixed ensured that even if the process was worked around, the failure could not happen.

3.4 Advanced Process Risk Assessment Based on ANSI/ESD SP17.1

3.4.1 Systematic Approach

The main problem in the risk assessment flow as outlined in Figure 28 is to determine the limits of the measurements which are acceptable for safe handling of the ESDS items. In Figure 28, charging of the ESDS item is measured, for example by an electrostatic voltmeter, however, what is the limit for charging? A correlation must be established between the parameters measured in the process and the robustness of the ESDS item with respect to CDM-like discharge. Some basic ideas are discussed here, the detailed approach is described in ANSI/ESD SP17.1.

To assess the risk of an ESDS item being damaged in a process by a CDM-type event depends on the CDM ESD robustness of the ESDS item against the CDM-type discharge. For CDM-type events, the discharge current is the decisive parameter. Therefore, in a first step, the robustness of the ESDS item against the CDM-type discharge in terms of the discharge current must be determined.

The simplest case is integrated circuits which will be discussed here. For ICs, the CDM robustness is typically known from product qualification. Typically, qualification tests yield not only the CDM robustness as a "CDM withstand voltage", but also the corresponding "CDM withstand current". If discharge currents are not monitored during CDM qualification or not available, the CDM withstand current can be estimated from the correlation to CDM currents into the verification modules used for waveform verification of CDM qualification testers (see Tables 1 and 2 in ANSI/ESDA/JEDEC JS-002 [12]). The capacitance of the component in the CDM tester can be approximated from a comparison with the size of the modules. If the CDM robustness of a specific IC is unknown, the CDM robustness can either be approximated from a similar product or guessing as a last alternative. The lower the guessed CDM level is, the more ESD control measures that must be implemented in the process. Experience has shown that a 100-volt CDM robustness (corresponding to 1.0–2.0 amperes CDM current) is enough to handle components in most of the processes without ESD damage; however, it requires advanced charge and discharge control techniques in the process [7]. Each level of uncertainty (for example, not knowing the CDM withstand current, but only the CDM withstand voltage) might cause additional safety margin and, therefore, more ESD control measures.

Unfortunately, for the discharge of a charged board or system or a board/system in an electric field, there is no "product qualification" and no easy correlation to any component robustness qualification exists. The reason for this is that even if a component pin on a board is contacted directly, the charge stored on that board is typically much higher compared to the charge stored on a single component. If the discharge current of the board cannot be measured, the only reasonable approach is to avoid "all" possible discharges or limit the charging of the board/system to a very low and safe value. A detailed discussion is given in ANSI/ESD SP17.1 [7].

Knowing the robustness of the ESDS item against a CDM-type discharge allows some basic correlations to parameters that can be measured in the process. For charged ESDS items, the limits for the following measured parameters can be derived from the CDM-type withstand current. Examples and a more in-depth discussion can be found in ANSI/ESD SP17.1 [7].

- The time-dependent discharge current of the ESDS in the process. This parameter gives the best correlation to the CDM-type withstand current.
- The electrostatic voltage at ESDS item in the process. The electrostatic voltage of a single component measured in the process can often be correlated directly to the device CDM withstand voltage measured during device qualification as the capacitance of the component in the CDM qualification tester is typically higher than the capacitance of the device in the discharge scenario in the process. However, for electronic assemblies and boards, this approach does not work, as the capacitances of electronic assemblies or systems are typically much larger, and the discharge path on board is not exactly known.

- Resistance-to-ground R_g and surface resistance R_s of the item enabling the ESDS item to discharge. The surface resistance and the resistance-to-ground of the item contacting the ESDS item and enabling the ESDS item to discharge will determine/limit the CDM discharge current. As a rule of thumb, all items contacting the ESDS item should be in the dissipative range (10^4 Ω -10^{11} Ω).

In addition to the parameters mentioned above, for ESDS items charged by induction, correlations can be established between the CDM withstand current and the electrostatic field at the location of the ESDS item and the electrostatic potential measured at the surface of the process-required insulator [7].

From this discussion, the basic ESD assessment flow for CDM-like risks of Figure 28 can be refined, including the measurements of the parameters as discussed above (Figure 36 for charged ESDS items and Figure 37 for ESDS items in an electrostatic field of a process required insulator).

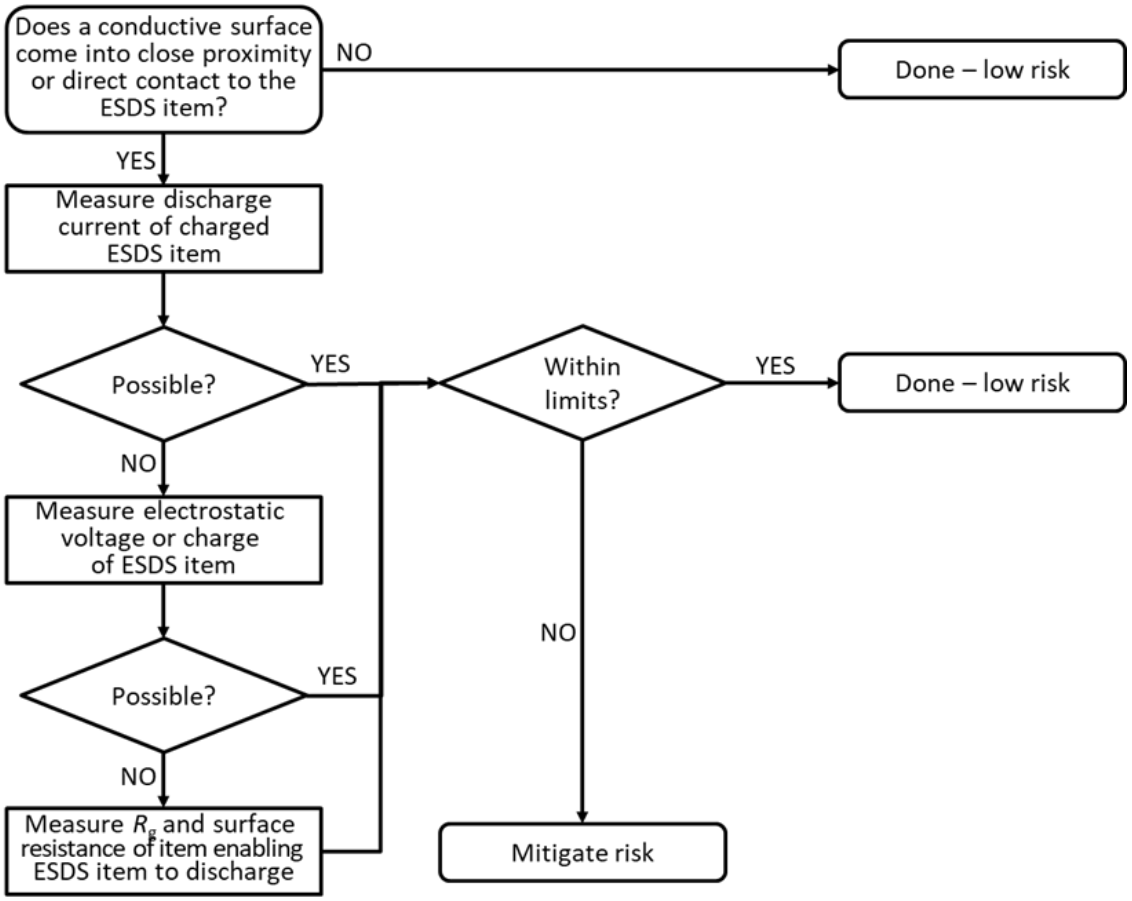

Figure 36: Flow to Assess the ESD Risk Induced by Charged ESDS Items according to ANSI/ESD SP17.1 [7]

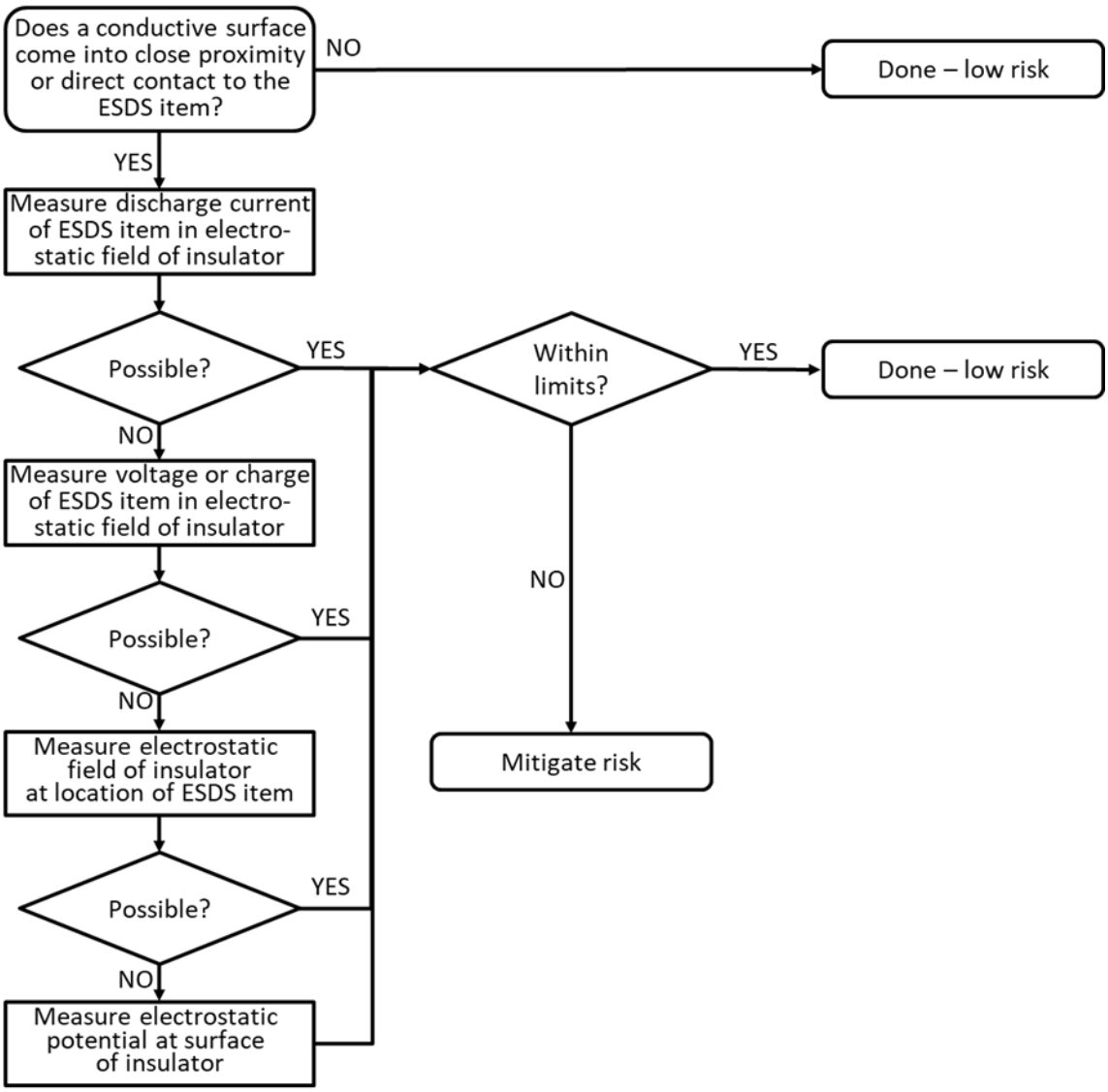

Figure 37: Flow to Assess the ESD Risk Induced by Process-Required Insulators according to ANSI/ESD SP17.1 [7]

The following sections give examples of how a process can be analyzed to avoid CDM like failures.

3.4.2 Practical Example of Process Risk Assessment Based on ANSI/ESD SP17.1

In this example, a printed circuit board (PCB) assembly is discussed. Integrated circuits (ICs) and discrete devices (for example, resistors, conductors, inductors) are picked from a tape & reel (carrier tape) and placed onto the PCB (and in the next step soldered), see Figure 38. Both ICs and discretes are considered as ESDS items.

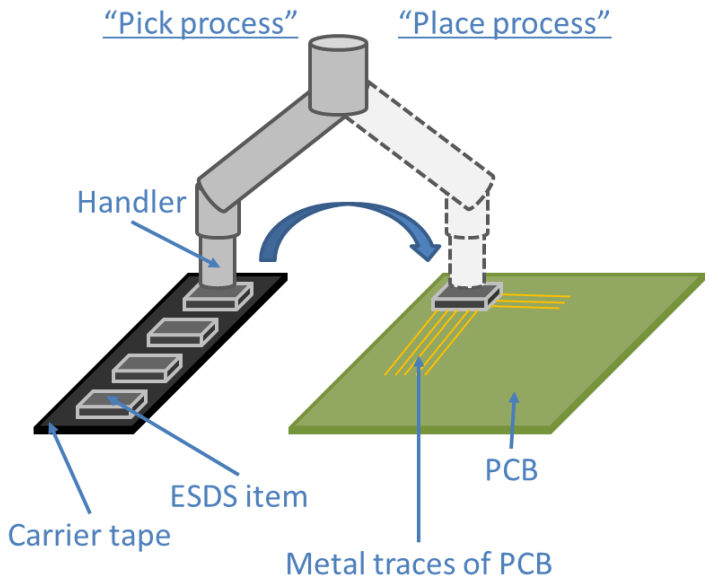

Figure 38: Pick & Place Process: ICs and Discretes are placed onto a PCB

In this pick & place process, three different risk scenarios – very typical for many pick & place processes – exist:

1. The ESDS item is charged in the cavity of the carrier tape and picked by an automated handler. This could result in a CDM-like discharge.
2. The ESDS item is charged and when it is placed onto the PCB, it discharges into the PCB. This will again result in a CDM-like discharge.
3. The PCB is charged and when the ESDS item is placed onto the PCB, discharges into the ESDS item. At first glance, this is a typical risk scenario of an ungrounded conductor, the PCB with ungrounded metal traces/areas, discharges into the ESDS item. Depending on how the ESDS item is fixed in the placement machine, the ESDS item may be floating during the placement process or may be grounded through the handler.
   - If the ESDS item is grounded through the handler, it is a risk scenario of an ungrounded conductor: the PCB with ungrounded metal traces/areas discharges into the ESDS item which is grounded.
     Note: This scenario was said to be modeled by the machine model.
   - If the ESDS item is floating during the contact with the PCB, that means the handler is not making electrical contact to the ESDS item, the discharge scenario is an “inversed CDM” (the ESDS item is charged instead of discharged in a “normal” CDM event.

Note: In this discussion, only the devices (ICs and discretes) are considered as ESDS items. In general, the PCB, and the PCB with assembled devices (PCBA), could also be considered as ESDS items. However, in this specific process, there is no risk seen for the PCB or the PCBA.

3.4.2.1 ESD robustness of devices in the process and measurement equipment

According to the datasheets of the devices in the process, the ESD robustness was as follows:

- The IC has an HBM robustness of 1000 volts and a CDM robustness of 250 volts.
- The discrete has an HBM robustness of 2000 volts and a CDM robustness of 500 volts.

For the measurements in the process, the following measurement equipment was available:

- Non-contact electrostatic voltmeter (ESVM)
- Resistance measurement apparatus (high-resistance meter)
- Multimeter (DC ohmmeter)

3.4.2.2 Parameter limits for process assessment of charged ESDS items picked from a tape & reel

The scenario of picking a (possibly charged) ESDS item with an automated tool, is discussed in Section 7.4 “Process Assessment Flow – Charged ESDS Items” of ANSI/ESD SP17.1 [7]. ANSI/ESD SP17.1 suggests the following parameters for a process assessment:

1. Discharge current (time-dependent). In this example, the process owner couldn't measure the discharge current due to a lack of appropriate equipment. The withstand currents from the product qualification are also not known.
2. The electrostatic voltage at ESDS item. If the discharge current cannot be measured or CDM withstand currents are not known, the electrostatic voltage of a single component measured in the process is the preferred parameter to be assessed. A non-contact electrostatic voltmeter (ESVM) was available.
3. Resistance-to-ground (R_g) and surface resistance of the item enabling the ESDS item to discharge is another parameter that can be used to assess the risk. Even if the electrostatic voltage of the ESD item can be measured, R_g can help to assess the risk further. A resistance measurement apparatus and a DC ohmmeter (multimeter) were available.

The detailed ESD risk assessment flow for the picking (sub-) process looks as follows:

1. *Assess whether the ESDS item comes into proximity or direct contact with a conductive surface during the process.* This is obviously the case in a picking process.
   - The automated handler is picking the ICs by contacting the mold compound. Consequently, there is no metal-to-metal contact when the IC is picked and there is no discharge path.
     → No risk in the picking process for the IC ✓
   - The discrete device is picked on the heat sink which is electrically connected to the circuit of the device. In contrast to the IC, picking the discrete device should be considered as a critical contact.
     → Possible risk of CDM discharge for the discrete ✗
     → Scenario must be assessed in more detail

2. *Measure the discharge current of the ESDS item using a current probe or a CDM test head.* Due to lack of equipment, the discharge current could not be measured.

3. *Measure the charge of the ESDS item by means of an electrometer, current probe, or Faraday Cup. Alternatively, the electrostatic voltage at the ESDS item may be measured by a non-*

contact electrostatic voltmeter, a contact-based high-impedance digital voltmeter, or an electrostatic field meter used as a non-contact electrostatic voltmeter.

- The charging voltage of the discrete was measured using a non-contact ESVM. Measurements on several devices show a significant variation, voltages between ~50 volts and 650 volts were measured. The tape itself was also charged, values of up to 200 volts could be seen. As a worst case, a charging voltage of 650 volts should be used. The device under consideration (discrete) was rated with an ESD robustness of 500 volts.
  → There is a potential risk for the discrete if it is picked with a metallic tool ✗
  → Scenario must be assessed in more detail

4. *Measure the resistance-to-ground (R_g) and the surface resistance of the item enabling the ESDS item to discharge using a resistance measurement apparatus.*
   - As there is a potential risk of a critical hard discharge that might damage the discrete, the resistance of the suction cup, either resistance-to-ground or surface resistance, can be used to further assess the risk. The measurements of the suction cup show a surface resistance of 1×10^8 Ω and, in the handler, $R_g = 5\times10^8$ Ω was measured for the suction cup. Even without knowing the CDM withstand current of the discrete, the resistance values seem to be high enough to eliminate any potential ESD risk. For a CDM withstand voltage of 500 volts, the discharge current of the very small discrete will not be higher than the discharge current of the small verification module of ANSI/ESDA/JEDEC JS-002 which is roughly 8.3 A. Using a simple Ohm's law estimation, the discharge through a suction cup with 1×10^8 Ω is I_{CDM} = 650 volts / 1×10^8 Ω = 6.5 µA, far below any critical discharge current.
     → No risk in the picking process for the discrete ✓

As a result of the assessment, in the picking process with a static dissipative suction cup, there is no ESD risk for both the IC and the discrete component even though voltages of 650 volts on the discrete were measured.

3.4.2.3 Parameter limits for process assessment of charged ESDS items placed onto the PCB

The following parameters can be used to assess the risk of the charged ESDS item:

1. Discharge current (time-dependent). As mentioned before, the most reliable method would be to compare the discharge current measured in production with the withstand current of the respective pin from product qualification. Unfortunately, in our example, it is not possible for the process owner to measure the discharge current and they also do not know the withstand currents from the product qualification.
2. The electrostatic voltage at the ESDS item. The next best approach is to compare the charging voltage of the IC in the placement tool with the CDM robustness of the device. From the datasheet, the process owner knows that the CDM robustness is 250 volts for the IC and 500 volts for the discrete component, respectively. The charging voltage of an ESDS item can, for example, be measured in production using a non-contact static voltmeter during pick and place. The datasheet value can then be used as a voltage limit for this device, having in mind that this a worst-case value for production.

   NOTE: To be able to make the measurement. the process must be paused; this gives the charging voltage time to decay. Hence, the measured voltage could be lower than the actual charging voltage of the device for the placement process. This should be kept in mind for the final assessment.

3. Resistance-to-ground (R_g) and surface resistance (R_s) of the item enabling the ESDS item to discharge. Normally, this would be another option to assess the CDM risk for the device, but here the resistance-to-ground of the item contacting the ESDS item is not a good parameter. The board is floating, so the resistance to ground would normally be very high. However, the board behaves like a capacitor for the discharge current, and the surface resistance of the material that makes contact with the ESDS item is less than 1 Ω since it is a metal line. This value was confirmed by a DC ohmmeter. Therefore, in this scenario, the discharge is caused by a critical metal-to-metal contact and a "hard" discharge must be assumed as worst-case.

A detailed ESD risk assessment flow could look like this:

1. *Assess whether the ESDS item comes into close proximity or direct contact with a conductive surface during the process.*
   - In this example, the ESDS item (IC and discrete) is placed onto the metal lines of the PCB; therefore, there is always a direct (metal) contact which might result in a hard discharge
     → Potential risk for IC and discrete ✗
     → Scenario must be assessed in more detail

2. *Measure the discharge current of the ESDS item using a current probe or a CDM test head.*
   - As mentioned above, in this example personnel in the PCB assembly line have no option to measure the discharge current of the ESDS item.

3. *Measure the charge of the ESDS item by means of an electrometer, current probe, or Faraday Cup. Alternatively, the electrostatic voltage at the ESDS item may be measured by a non-contact electrostatic voltmeter, contact-based high-impedance digital voltmeter, or electrostatic field meter used as a non-contact electrostatic voltmeter.*
   - The only parameter that is available in this example to assess the CDM risk for the ESDS item is the CDM voltage robustness in the datasheet. The only meter that is available for this measurement is a non-contact electrostatic voltmeter. With this, the charging voltage of the ESDS item can be measured. The charging voltage of the device is measured at a short distance (typically less than 5 mm) while the ESDS item is hanging on the suction cup of the pick-and-place tool.
   - For the discrete, the electrostatic voltage was always zero since the suction cup is dissipative and grounded and touching the (conductive) heat sink of the discrete.
     → No risk in the placement process for the discrete due to charging of the discrete ✓
   - In contrast, for the IC, the measured electrostatic voltage of the IC before placement was always higher than 300 volts.

4. *Compare the measured parameter (discharge current, charge, electrostatic voltage, Rg, and surface resistance) with the defined limits*
   - If the measured electrostatic voltage would have been significantly below the defined limits (in this example 250 volts), the assessment could be concluded with the result that there is low ESD risk by the charged ESDS item. However, a voltage of 300 volts was measured. Accounting for the possibility that the actual voltage on the ESDS item may have been even higher due to voltage decay as a result of pausing the process for the measurement, this voltage is higher than the defined limit (250 volts).
     → Potential risk for IC and discrete ✗

→The root cause of charging must be identified, and risk mitigation must be implemented

1. *Find root cause for charging,* for example, wrong packing, wrong or ungrounded suction cup. *The next step is then to define measures to mitigate the ESD risk.*
   - Possible risk mitigation measures are reducing the charging of the ESDS item or changes in the process to avoid critical contacts. There are two possibilities to reduce the charging of the IC; first, to install an ionizer but it must be checked whether the ionizer is fast enough to discharge the IC to a low enough voltage level within the process time. The second possibility is to change the material of the suction cup. Changing the suction cup to a different material with a lower point-to-point resistance reduces the charging to less than 100 volts. The resistance to ground was reduced to $R_g = 5\times10^5$ Ω. There are two potential reasons for the reduced charging, first, the suction cup itself is better grounded and dissipates charge faster to ground; secondly, there is less tribocharging between the product's mold compound and the changed material of the suction cup during the picking process.

3.4.2.4 Parameter limits for process assessment of charged conductors (PCB) discharging into ESDS items

In this example, it has to be assessed whether a charged PCB can discharge into the ESDS item while it is hanging on the suction cup. The first question is what is the relevant discharge scenario which must be considered in the process assessment.

- For the IC, the suction cup is contacting the insulative mold compound and, therefore, the IC is floating. This situation is reversed compared to the scenario discussed previously in Section 3.4.2.3 where the IC is charged and discharges into the PCB. The capacitance of the board is significantly larger than the capacitance of the IC and this situation can be assessed as an "inversed CDM". Limits, measurements, assessments, and risk mitigation are identical to the situation described above.

- The situation changes for the discrete. For the discrete, this situation can be seen as a "machine model" like discharge since the discrete is held by the grounded suction cup on one pin (heat sink) and the charged PCB is discharging into another pin. The entire charge is flowing through the discrete (where the conductor is formed by the metallic lines of the PCB) into the discrete. In contrast to the "inversed CDM", in this scenario, the entire charge of the board flows through the discrete and the grounded tool to ground. However, the resistance of the tool including the suction cup must be considered, too. As pointed out in Section 3.4.2.1, the surface resistance of the suction cup was measured as 1×10^8 Ω and, in the handler, $R_g = 5\times10^8$ Ω was measured. Therefore, although there is a ground path from the discrete through the suction cup to ground, the discharge current to ground is limited by the resistance of the suction cup and does not harm the discrete. Nevertheless, there is a critical metal-to-metal contact in this scenario; for the discharge current of the metal-to-metal contact the discrete is virtually floating. Hence, also for the discrete, the discharge scenario is best described by an "inversed CDM" with the same considerations as discussed in Section 3.4.2.3.

As for both the IC and the discrete, the discharge scenario is an "inversed CDM", the same limits apply to the charging of the PCB as for the maximum allowed charging of the ESDS items. The

charging of the PCB must be lower than the withstand voltage of the ESDS item with the lowest ESD CDM robustness, in the example, this is the CDM robustness of the IC which was 250 volts. The voltage on the PCB (that can be measured with the non-contact electrostatic voltmeter with high local resolution on the metallic lines of the PCB) must be reduced below this critical value, for example, by using ionization.

3.5 Conclusions

Different methods to analyze an assembly with respect to CDM risk are described. The described examples demonstrate how to use these methods in actual production lines.

The field problems presented demonstrate that if such a CDM risk analysis is not performed, even devices considered CDM robust might fail during assembly or testing since a PCB can get charged and discharges at a significantly higher current level than the stand-alone IC device at the same charging voltage level. At the same time, the practices discussed in this chapter and additionally in ANSI/ESD SP17.1 can be leveraged to manage CDM ESD risk in manufacturing for devices with CDM target levels of 125 volts and lower.

A process risk analysis performed according to ANSI/ESD SP17.1 can identify ESD risks in an assembly line. In an assembly line, CDM-related risks are typically predominant. The result of such an analysis can lead to the implementation of additional ESD protection measures in the process but can also result in improving existing measures that are not effective or not needed.

How often such a process risk analysis must be performed depends on the importance of the measures and their impact on the complete process.

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Chapter 4: Consolidated Industry Data on CDM levels vs. Field Returns

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This chapter discusses the impact of the CDM qualification level of a device on the potential risk of failure of this device in the field. The evaluation is based on the data gathered from many members of the council.

Although many members of the council contributed with data, the total quantity of devices that was included is less than for the HBM analysis, since CDM testing is not as common as HBM testing. Nevertheless, a total quantity of nearly 12 billion devices collected between 2003 and 2007 should give a good representation of the situation in the field. The device types range from discretes to ULSI system-on-chip parts. Field returns from testing and handling at the IC supplier, from the board manufacturers, and end-customers have been considered. There is a weak dependence of the return rate on the CDM qualification level. Typically, these returns are caused by problems in the ramp-up phase of the manufacturing process at all partners in the production chain of a new product. Minor changes in the ESD control of the manufacturing process solve these problems instantaneously without big investments. No dependency between EOS-related returns and CDM levels were detected.

Real CDM failures (gate oxide failures), like those generated during CDM qualification tests, are mainly occurring in the semiconductor backend and testing, but are not included in most of the data collected.

4.1 Field Return Rates versus CDM Voltage Level

The EOS/ESD field return data of various types of products have been collected. Product types range from discretes, memory, automotive ICs, µ-processors to highly integrated system-on-chip ICs for mobile communication. The analyzed fails include mainly returns from the manufacturing of the board and at the end-customer. About 1000 different designs are considered. The total number of shipped devices in this database amounts to 11.6 billion. The returns are analyzed versus the CDM withstand voltage of the design since this could give a correlation to the charging voltages measured in the field and since qualification test results are reported in voltage. Since the number of devices in the different voltage classes are not equal, the failure rate was statistically weighted (using the ChiINV function [1]) to get an indication about the possible expected upper failure rate limit with a confidence level of 60%. By doing this the different voltages classes can be compared much better. Figure 39 shows the statistically expected maximum failure rate as a function of the CDM withstand level.

In general, the analysis of the data was hindered by the fact, that

- Different CDM standards (JEDEC JESD22-C101 and ANSI/ESD STM5.3.1) were used.
- In many cases, the fail level was not determined, instead only tested up to 500 volts to confirm meeting a target. Thus, the actual withstand level might be much higher. This especially applies to parts passing 500 volts.

The inspection of Figure 39 shows a drop in the failure rate at a withstand voltage of 500 volts. This could lead to the assumption that a minimum CDM robustness of 500 volts is needed for safe handling. However, a more detailed analysis of the data reveals, that the statistics in Figure 39 are dominated by very high failure return rates (> 100 returned parts) of 15 designs out of 949. If these are excluded, there is a more or less equal distribution of FARs observed across the CDM robustness classes as shown in Figure 40. This applies to 934 designs and 9.5 billion shipped devices. The return rates are clearly below 1 DPM.

It is also evident that notable return rates can even be found with passing CDM levels of >1500 volts.

The few designs with higher failure return rates (> 100 returned parts) resulted from EOS-like events as shown in Section 4.2.2. A relation to a CDM-like discharge event could not be shown.

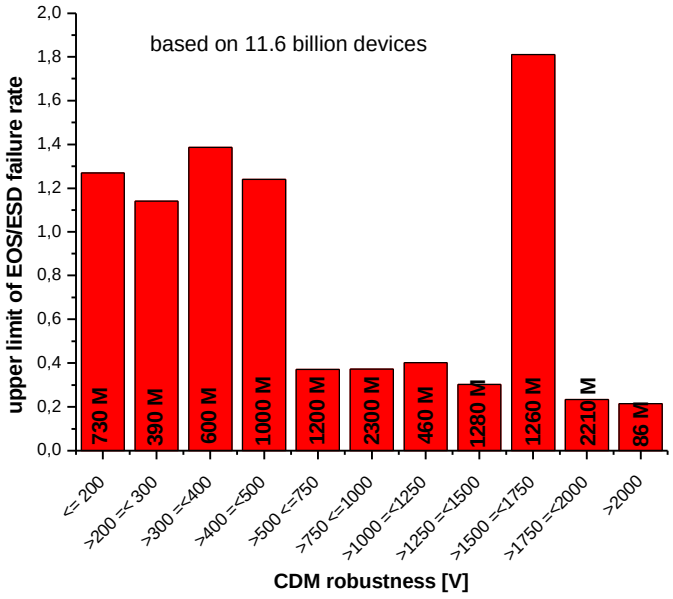

Figure 39: Upper limit of EOS/ESD failure return rate (in defects per million) versus CDM withstand voltage. An amount of 11.6 billion shipped devices has been considered. The number of devices shipped within a certain CDM classification regime is noted in each column.

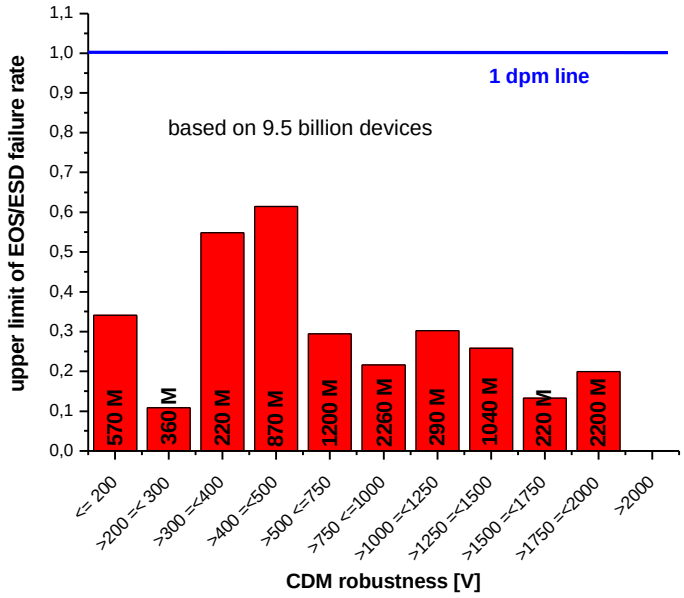

Figure 40: EOS/ESD failure return rate (in defects per million) versus CDM withstand voltage. The same database as Figure 39 but any designs with clearly elevated return rate (> 100 reported fails) have been removed.

4.2 Analysis of Typical Examples

4.2.1 Typical CDM-like Failure Picture

Figure 41 is taken from an FA report of a device with high-speed I/O pins having a low CDM value (< 125 volts). The failure found in the field (semiconductor fab) shows the same failure signature as devices damaged during CDM qualification testing.

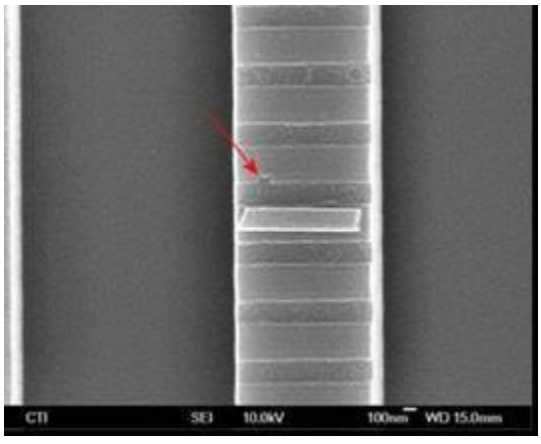

Figure 41: The SEM micrograph of the FAR depicts a pinhole in a gate oxide. This failure picture is classified as a typical CDM-type fail.

But failures with such a typical CDM qualification test failure signature are very difficult to find. Most of these occur during manufacturing or testing at the semiconductor manufacturer's site.

4.2.2 Typical EOS-type Failure Picture

The collected EOS/ESD failures include all types of EOS-related failures (including system-level ESD) and ESD-related failures (including CDM-type failures). Usually, HBM related failures are rarely observed [2]. Comparing the subset of designs accounting for 1.6 billion sold devices indicates that most of the EOS/ESD fails are due to electrical overstress (EOS).

Different from typical CDM failures, indicated by little pinholes in the gate oxide, most of the field returns show large areas of melted metal like in Figure 42. This example is taken from a device mounted in a TQFP 100 package which showed 409 fails out of 36 million sold devices. This device is one of the outliers of Figure 39 depicting a very high CDM robustness (1000 volts). A typical EOS-type failure of a melted metal bus was found. This implies a large amount of dissipated energy. The comparatively lower energy of a CDM event is not able to generate such an extended failure signature.

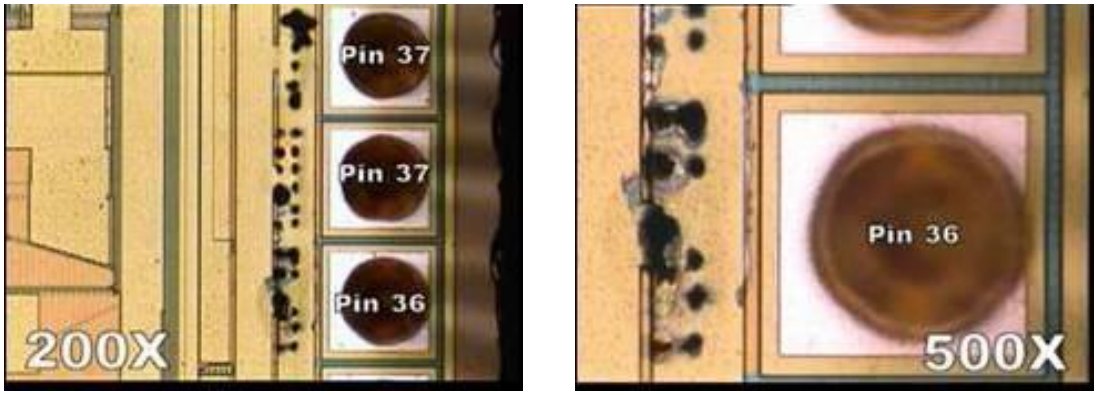

Figure 42: Optical inspection FAR depicts major damage in the metal bus which is an indication of a large amount of dissipated energy. This is rated as a typical EOS-type fail.

Another example of an EOS type failure was found with a large device in an LGA 1681 package as shown in Figure 43. The device had a reasonable CDM robustness of 300 volts determined by its 320 high-speed pins. All other pins had a CDM robustness of more than 500 volts. The failing devices coming back from customers did not show failures on the high-speed pins. Only power supply pins with a much higher CDM robustness were affected. As can be seen in Figure 43, the failure analysis showed a junction punch through which cannot be generated by a CDM-like event but only by an event with higher energy, i.e. an EOS-like event.

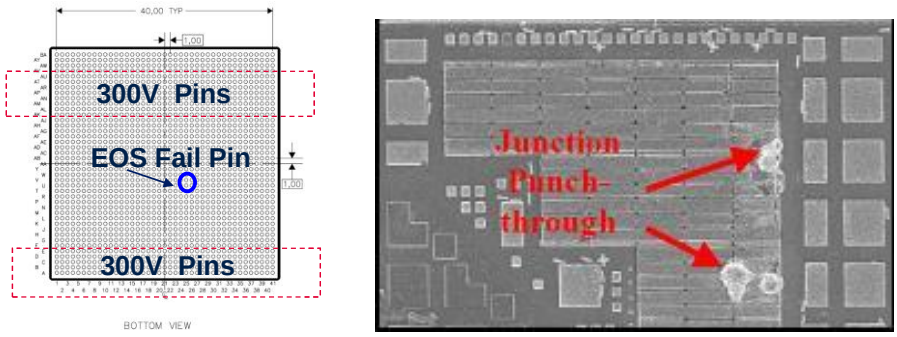

Figure 43: EOS-type damage that happened on the more CDM robust power pins of a device and not on the weaker high-speed pins.

4.3 Conclusions

The FAR data of more than 11 billion devices collected by the members of the Industry Council showed that EOS/ESD failures can appear in the field independent of the CDM robustness level from less than 100 volts to greater than 2000 volts.

During CDM qualification testing, the typical failure seen is a dielectric breakdown. Such a failure is mainly seen at the IC supplier during the ramp-up phase of a new product with low CDM robustness. This can easily be solved by improving the ESD control measures without doing a redesign of the product. Usually, only a minor effort combined with low investment is required.

Case studies showed that most of the field failures in the FAR data are due to EOS or Charged Board events. These EOS-like failures normally did not occur on the CDM weak pins but on more robust pins that are somewhat exposed. Also, these CBE-like failures are not directly comparable to CDM-like failures. They have their origin in the charging of the board which can be assessed in the same way as "real" CDM-like failures.

It should be noted that as CDM target levels drop below 200 volts, data is limited as to the overall impacts. Care should be taken to ensure that proper ESD controls are in place and that the proper process assessments have been made in the manufacturing flow as per ANSI/ESD SP17.1. This will ensure the manufacturing environment can manage the risks with component target levels moving towards 125 volts. Care should also be taken on the design side to ensure that if a target level of 250 volts cannot be met (for performance reasons) as discussed in Chapter 2 that the achievable target level is *maximized* to reduce manufacturing risks and also that the designed target level for the product is in line with the manufacturing capability.

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Chapter 5: Recommendations for Realistic CDM Target Levels for the Present and an Outlook for the Future

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5.1 Preface

In the preceding chapters, control of the manufacturing environment to prevent CDM events and design of ESD protection addressing CDM parameters have been discussed.

In contrast to HBM, there is no single CDM measurement parameter that relates to both CDM testing (Appendix C) and CDM ESD design (Chapter 2), or evaluation for CDM control measures (Chapter 3). HBM voltage levels allow both the extraction of a current level sustained by the ESD protection design and the corresponding voltage which can be correlated to measured voltages in the manufacturing environment, providing a useful guide for the quality of the ESD control measures. In contrast, the correlation between current and voltage levels in a CDM tester varies widely with the size of the package itself, the applied test standard, and the ambient conditions during the test.

As in the case of HBM, the application of ESD control measures in an EPA guarantees safe manufacturing of parts passing a base ESD level. For CDM, fails might occur even for parts with extremely high "CDM robustness." This can only be corrected by an audit of the process steps and the introduction of process-specific control measures. These details are covered in Chapter 3. For example, Table II in Chapter 3 lists possible risks in the PCB assembly. This is an illustration that CDM reliability does not just come from products with a specific CDM level but that manufacturing control measures are equally important. This CDM process control audit/process-specific control is typically not a relevant cost factor.

Consequently, a *compromise* has to be found balancing the growing limitations of the on-chip ESD circuits versus the effort in the ESD control field. The objective of this chapter is to propose a CDM target that accommodates both constraints without compromising quality. Moreover, we also present a *realistic roadmap* for CDM as the technologies further scale into the nanometer nodes beyond 10 nm. We will specifically examine the restrictions for ultra-high-speed designs in these sub-10 nm technologies. These are especially dictated by SERDES operating in the range of 224 Gb/s.

5.2 Relevance of Current Level

The CDM damage mechanism is typically due to an excessive on-chip voltage drop caused by the CDM peak discharge current. Thus, all on-chip design measures address the avoidance of this excessive voltage drop at critical locations such as across thin gate oxides. The sizing of the protection clamps is based on the value of the peak current level which has to be safely passed. In

the CDM domain, this peak current level can exceed the HBM peak current by an order of magnitude. In the case of I/O ESD cell development, it is not known beforehand which package they will be used in, yet the package is a major contributor to peak current. Thus, a well-defined current level is critical as a design goal.

5.3 Relevance of Voltage Level

The relevance of the CDM voltage levels comes from the gathered experience of ICs manufactured at production lines around the world, where only the CDM voltage level of the qualification test is known. The drawback had been the deviation between the various test standards as discussed in Appendix C. With the consolidation of the CDM test methods between the ESDA, JEDEC, AEC, and IEC this is much improved.

5.4 Correlation to Control Measures in Manufacturing Environment

The correlation of the CDM qualification voltage level of an IC to the capability of handling it in an EPA is of an empirical nature. The measured voltages in the line and the tester pre-charging voltage have no direct correlation. It is also unclear whether the strong dependency of the damaging current on the package, as given by the CDM tester, also appears in the real-world events within the manufacturing site.

Based on the experience of handling parts of a certain robustness class, analysis methods have been developed to rate the quality of an EPA concerning CDM events as described in Chapter 3.

5.5 Recommended CDM Target Level

With a detailed process-specific assessment of the manufacturing, handling or testing process is performed by an ESD control expert applying the available measurement methods (Chapter 3), a safe manufacturing environment can be achieved during ramp-up and volume production for parts with a CDM withstand voltage < 200 volts. The standard practice ANSI/ESD SP17.1 [5] provides insight into methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive (ESDS) items are handled. The process assessment covers risks by charged personnel, isolated conductors, and charged ESDS items and ESDS items in an electrostatic field. It can be used by experts in the field of ESD control to assess the manufacturing process and to ensure the safe handling of parts with CDM < 200 volts. This is an ideal case. But knowing that the capability of a detailed CDM assessment is limited today, we recommend reducing the assessment effort while still maintaining the basic CDM control measures as called out in ANSI/ESD S20.20 [1], IEC 61340-5-1 [2], or JEDEC JESD625 [3] for products with a CDM level of 200 volts and above. The recommendations are summarized in Table IV.

Table IV: Realistic Rating of CDM ESD Qualification Levels for All Package Types

CDM classification level (tested acc. to ANSI/ESDA/JEDEC JS-002)	ESD Control Requirements
$V_{CDM} \geq$ 200 V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators according to standards like ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625
$V_{CDM} <$ 200 V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators **+** • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads) **+** • **Charging/discharging measurements at critical process steps following ANSI/ESD SP17.1**

However, one must note that if a detailed process-specific assessment is not done during *ramp-up*, production failures can still occur under some circumstances for products *with any CDM level*. In this case, a specific audit is needed to find the root cause of the failure and to address it by process-specific ESD control measures.

Impact of the Recommended CDM Target Level

A **general CDM qualification target of 250 volts** (tested according to ANSI/ESDA/JEDEC JS-002) has been widely adopted in the industry since the publication of Industry Council White Paper 2 in 2009.

The downscaling and the progress in high-speed design now lead to new brick walls in ESD design. Ultra-high-speed interfaces operating at a Nyquist frequency of 56 GHz or data rate of 224 Gb/s PAM4 limits the available capacitance budget for on-chip protection diodes to less than 75 fF. While lower speed interfaces in downscaled technologies of 7 nm and beyond are NOT foreseen as limitations, the design of ultra-high-speed I/Os is the most challenging task with physical limits for the protection design. For this ultra-high-speed interface in advanced nodes, a practical CDM target level of 125 volts for design is recommended to ensure high-speed performance. In the high-speed regime from 56 Gb/s to 224 Gb/s, design effort should be put in to maximize the CDM robustness level between 125 volts and 250 volts CDM.

Commonly, pre-validated IP blocks are used for the implementation of high-speed interfaces, which are partly supplied by third-party vendors. A CDM target peak current needs to be defined for IP blocks to specify a meaningful ESD robustness target. The recommended target for ultra-high-speed IP blocks is a CDM peak current of 2.5 amperes to support a 125-volt goal for a wide range of package sizes. IP to be integrated into very large packages, e.g. beyond 4000 mm^2, may need to evaluate the need for a lower target peak current which would result in even a lower CDM

target level than 125 volts, or an evaluation for a higher target peak current may be needed in order to maintain the same 125 volt CDM target.

In general, the peak current requirement for IP blocks is not a hard target and can be reduced if the SoC size and package type are known as discussed in Appendix B. In this case, extraction of the actual peak current based on a 125-volt CDM robustness of the SoC can be done.

This recommended target level is not determined by any distinct threshold found in the field returns statistics, any physical models, or ESD control standards. It must be considered as a guiding value to allow alignment of practical ESD control measures in a manufacturing line and ESD on-chip protection design**.** As discussed in Appendix F, the robustness of these parts regarding other failure mechanisms like EOS, CBE, or system-level ESD is not degraded by this recommended target level.

5.6 Outlook and CDM Roadmap from Silicon Technology Scaling

As discussed in Chapter 2, IC designs continue to place severe restrictions on the achievable CDM levels as the demand for higher I/O speeds increases. This document has already shown that CDM withstand voltages must be relaxed to accommodate today's advanced process technologies and high-speed performance requirements. For technology nodes of equal or larger than 10 nm, a proposed goal of 250 volts CDM is not only safe; it is also practical and compatible with high-speed I/O circuit performance. This is especially true for large pin count ICs that contain these high-speed circuits. But as silicon technologies advance further into the single-digit nanometer regime at the 7 nm node and beyond, even lower withstand voltages will be required to account for scaling effects and the continued drive towards higher circuit speed performance at data rates reaching 224 Gb/s or more.

A roadmap based on this projection is shown in Figure 44. During the early years of CDM awareness, customers requested protection levels of 1000 or 750 volts. For instance, during the 1991 time period, AT&T specifications were 1000 volts for corner pins although some allowance was given to high-speed pins. At the time, these specifications were based on the commonly available ESD controls for CDM in the manufacturing area. However, by the late 90s, 500 volts became the default standard for the industry as customers and suppliers had become comfortable with this as a reasonable level. Therefore, there has been precedence that over time a revised level is necessary to avoid over-design and avoid harsh product requirements.

A CDM level of 250 volts had been introduced by White Paper 2 Revision 1 in 2009 as a safe and practical level to accommodate design demands while applying proven CDM ESD control methods. As the roadmap further projects, at the 7 nm node and beyond, 125 volts is proposed as a new practical CDM level for ultra-high-speed interfaces at 224 Gb/s and above only. While a CDM target level of 250 volts is no longer feasible for the design of high-speed interfaces between 56 Gb/s and 224 Gb/s, focus should be put on the implementation of an optimum CDM ESD protection to achieve the highest possible ESD robustness. This is especially needed in the coming years prior to when manufacturing ESD controls have been improved further to safely handle components with CDM levels well below 250 volts. At the same time, all other products, such as those with standard GPIO interfaces, would still be targeted at 250 volts leveraging basic control methods as described in ANSI/ESD S20.20 [1], IEC 61340-5-1 [2], and JEDEC JESD625 [3]. The

new ESD Technology Roadmap from the ESDA has published these prevailing trends [4]. Also, indicated in Figure 44, is the progress of CDM ESD controls within the manufacturing area. CDM ESD controls to less than 50 volts have already been demonstrated with proper advanced ESD control methods. Consequently, "*continuously improved CDM ESD controls*" in the manufacturing area must not only become a routine practice; it should be the primary approach to ESD sensitivity solutions. While the on-chip protection should always ensure some minimum protection, ESD control methods should take on a more prevalent role. Judging from the expertise and the factory control methods that are available today, this would not and should not be an issue. Continuous improvement in CDM ESD controls in the factory has taken on a multi-faceted approach to achieve these goals. This involves an increased awareness of CDM in the production and handling areas, improvements in, and greater attention to, auditing programs along with more readily available CDM data. When leading edge devices are introduced, the response time with failure-driven process control has to be improved. In the future, additional detection and monitoring technology may also become important. The purpose of this road map is to enhance this awareness and point out the dire necessity for continuous improvement of the CDM ESD control programs such as the recently released standard practice on process-specific ESD control measures in ANSI/ESD SP17.1 [5].

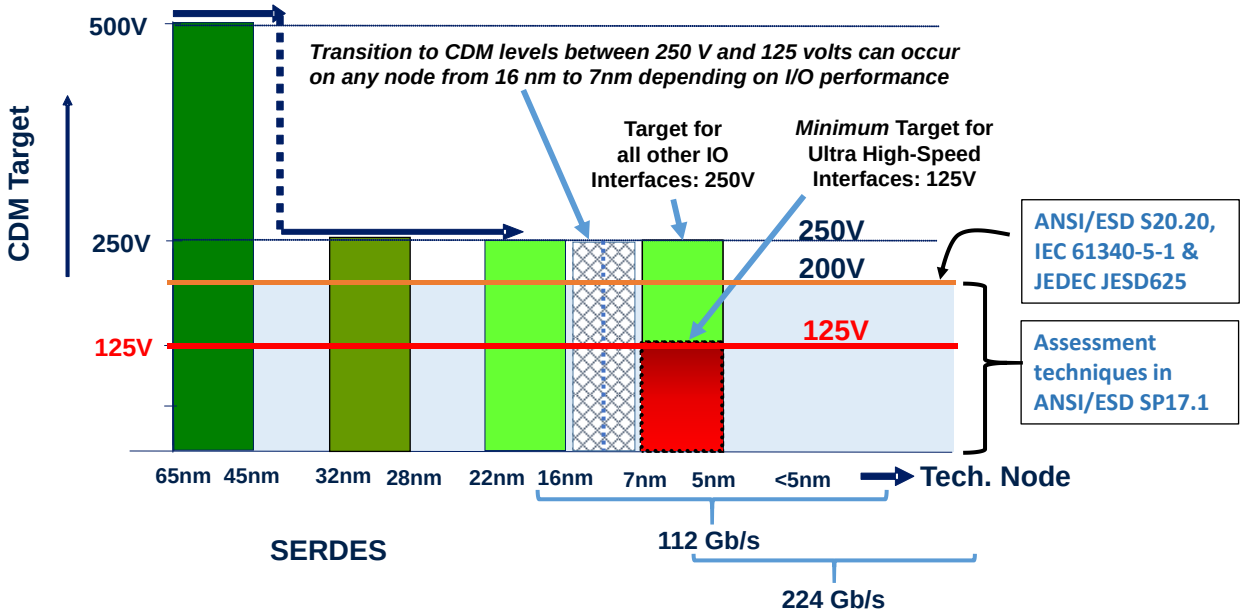

Figure 44: Evolution of CDM Target Levels vs. Time. The applicable measures of CDM control at the factory level are also shown in conjunction with the CDM level roadmap. While there is no change in the recommended CDM Target Levels for products manufactured in very advanced nodes of 7 nm and beyond with lower speed interfaces, the physical design limitation for ultra-high-speed interfaces leads to a reduced CDM Target Level.

5.7 Outlook and CDM Roadmap from Silicon Technology Scaling– Impact of 3D ICs

Today a growing number of 2.5D and 3D packages are seen in the field. In a 2.5D or 3D packaging process using die stacking, a high number of microbumps and through-silicon vias (TSVs) exists which are not connected to package balls, but they can experience ESD exposure during a few process steps in the manufacturing process. The number of such microbumps can range from

thousands to even tens of thousands. The constraints and first recommendations for 3D packaging are described in the joint whitepaper of the ESDA and GSA [6].

Careful control of a few critical process steps will guarantee safe handling for a CDM target level of 30 volts. This amounts to a CDM I_{PEAK} between 100 mA to 250 mA for smaller die size in the 100 mm^2 and below range and 500 mA to 800 mA for large die size in the range of 500-700 mm^2. While these are currently known and applied targets, they need to decrease when entering the regime of extensive heterogeneous integration based on hybrid bonding. This will lead to tens of thousands of die-to-die interfaces/mm^2 up to 1 million die-to-die interfaces/mm^2 [7]. To avoid an exponential increase in ESD-related chip area and power, the robustness target for CDM for die-to-die interfaces needs to drop to < 5 volts while improving the ESD control of the process and handling steps of the heterogeneous integration. The predicted roadmap is shown in Figure 45.

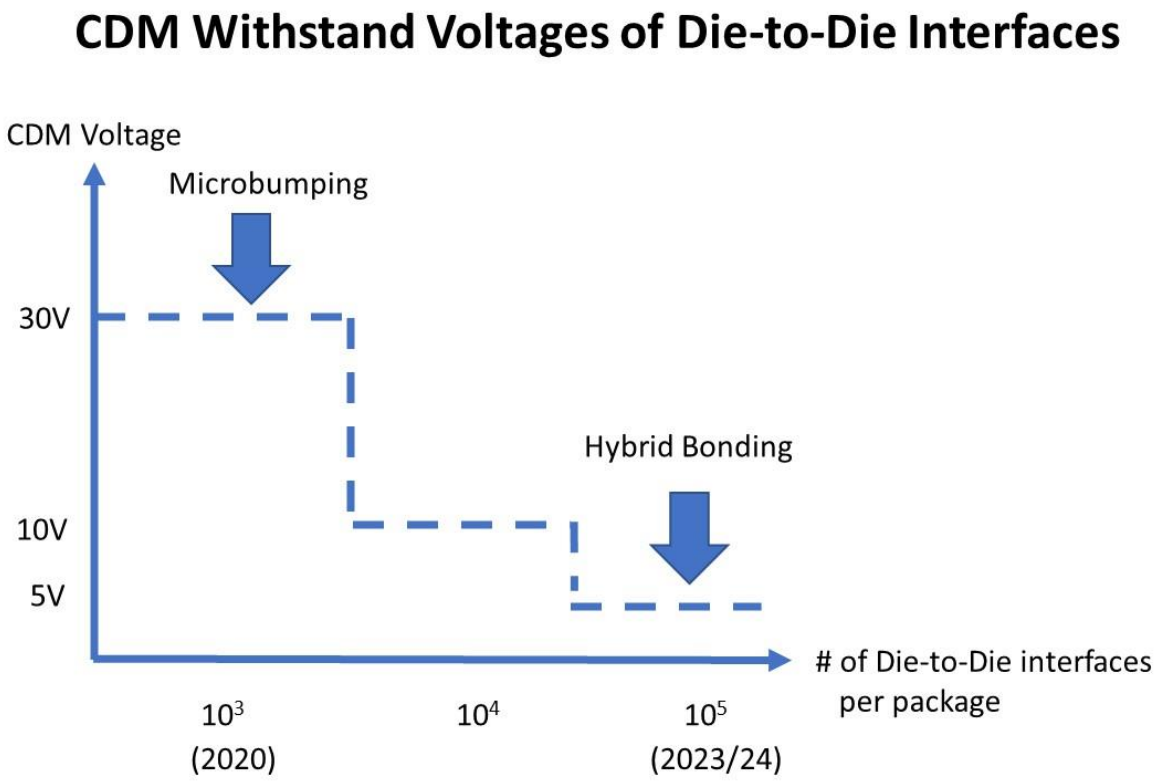

Figure 45: Evolution of CDM Target Levels for die-to-die interfaces vs. number of die-to-die interfaces per package With the technological advance of heterogeneous integration and the exponential growth of die-to-die interfaces over the next few years, the target needs to be stepwise reduced and the ESD control measures of the heterogeneous integration processes have to be refined accordingly.

Due to the extremely high number of die-to-die interfaces, the tight pitch of the bumps and hybrid bonds, and the missing ATE test capability for single dies, a full-scale CDM qualification test of microbumps is not feasible. It is recommended to verify the robustness of representative microbumps using a VF-TLP pulse setup or wafer-level CC-TLP. This can also be performed on test chips and be referenced for the final product.

5.8 Challenges and Future Direction of Low Voltage CDM Testing

CDM testing of products designed to the reduced levels recommended above requires caution. Air discharge test methods like ANSI/ESDA/JEDEC JS-002 exhibit pulse to pulse variability which is exacerbated at voltages below 200 volts. As shown in Appendix C.3, this variation can be so significant that it becomes very difficult to determine the true CDM robustness of a design. One unit may pass at the tested voltage level, while the next tested unit could fail simply because the stress current was significantly higher during the second round of testing. Such variation in generated peak current could lead designers to design with extra margin simply to pass the highly variable test – a situation which is not desirable and may not be feasible. Please see Appendix C.3 for more information regarding testing pitfalls at these low voltage levels.

To eliminate zap to zap variation at low CDM test voltages, a number of approaches are being perused. In one method, referred to as Contact First CDM [8], the air discharge is maintained, but the discharge is moved away from the pin under test using a specially designed test head to provide a better-controlled arc environment. Other testers eliminate air discharge entirely. Once in contact, a relay is used to initiate the discharge to the pin. The relay provides a very stable, repeatable mechanism for initiating the stress event. Low-impedance contact CDM (LICCDM) [9-11] and capacitively coupled transmission line pulsing (CC-TLP) [12-15] are two relay-based approaches that are being investigated across the industry. Please see Appendix C.4 for more information on these test methods.

Future CDM test standards must allow test methods with the ability to test more reliably at sub-200-volt levels [9]. As outlined in this document, such testing will become increasingly commonplace as technology scales and signaling rates increase. In the interim, understanding the pitfalls with the present techniques is critical to aid both designers and IC test houses.

5.9 Guidance for Design

As the goal of safe manufacturing is achieved by a combination of ESD control in the ESD protected area, an ESD conscious handling and testing procedure, the appropriate choice of the package, and the on-chip ESD protection, it is important to consider all aspects to safeguard low-level CDM interfaces. Knowing that today's EPAs are not yet equipped to fully support a minimum CDM robustness of 125 volts, the following best-known methods should be followed in design:

- Don't design high-speed interfaces to the minimum 125 volts CDM when it can be avoided, explore the best compromise between performance and CDM robustness, targeting a level as high as possible in the window between 125 volts and 250 volts by co-design methods.
- As ESD is a statistical effect, the number of pins designed with a low CDM target level (< 250 volts) should be kept to a minimum.
- Avoid the placement of high-speed balls with a lower CDM target level (< 250 volts) at the corner or - if possible - at the edge (if BGA) of the package.

5.10 Summary

The CDM roadmap is an evolving strategy that is dictated by I/O applications. In the past, 750-volt and 500-volt target values were common and served for several generations of technologies. In 2009, the first revision of this white paper documented with an abundance of evidence from products shipped at different CDM levels, that 250 volts is safe for all applications without regard to the I/O application speed. Moreover, factory control methods allow for CDM target levels ≥ 200 volts using basic ESD control methods with the grounding of metallic machine parts and control of insulators according to standards such as ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625. This newest revision of the white paper addresses the challenges for high-speed interfaces in 7 nm technologies and beyond, demonstrating that a CDM target level of 250 volts cannot be met due to several constraints. This necessitates the target be reduced to 125 volts while noting that additional process assessment (as per ANSI/ESD SP17.1) is mandatory for these cases. To support this lower target, a design target of 2.5 amperes of CDM peak current for these ultra-high-speed IP blocks > 224 Gb/s is recommended. Note that for the largest packages, this limit of 2.5 amperes may even bring the limit below 125 volts. For designs targeting the high-speed regime of 56 Gb/s to 224 Gb/s the CDM target of 250 volts will also not be achievable and a level between 125 volts and 250 volts has to be accepted. Nevertheless, in this high-speed regime, maximum design effort should be put into the optimization of the CDM ESD robustness to reach the highest possible CDM target level. This is especially important in the time when manufacturing ESD controls still need to be improved to safely handle components with lower CDM robustness.

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Appendix A: External Versus Internal High-Speed I/Os

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A.1 Introduction

IC component or PCB I/Os can be classified as internal or external based on the accessibility during various phases. This estimates what type of I/Os have a higher probability to be exposed to ESD stress during processing, installation, and use. This ESD stress can have varying waveforms including similar peak current, energy, and rise time characteristics as found during HBM and CDM testing.

Most of the previously published information about grouping component I/O pins to internal and external from an ESD sensitivity point of view comes from Industry Council White Paper III. The grouping is typically done from a final product design point of view where all I/Os which are accessible by the end-user are classified as external. In addition, there can be ESD-sensitive I/Os that are not directly accessible in the final product but are contacted during system manufacturing, testing, and handling phases. These I/Os are also accessible during component frontend and backend manufacturing processes where ESD control precautions are required. Therefore, ESD damage risks depend on product manufacturing steps, design of the system, and the environment where the final product will be installed and used.

I/Os classified as external or internal should have a known ESD robustness for three main reasons; a) the data can be used to build up ESD protection during manufacturing and handling phases, b) the IC or system designer can use sensitivity data to optimize external protection by using on-board circuits or by shielding the interface, c) the interface is designed to survive system-level tests.

One challenge with internal versus external selection and risk assessment is that the CDM withstand voltage rating can be challenging to link to real-word ESD scenarios as the qualification voltage alone doesn't directly define charged device type ESD risks or susceptibility of ICs. Typically, CDM damage correlates well with the CDM peak current and the rise time of the current waveform. With energy-sensitive I/Os, the charge transferred in the first main pulse of the CDM current waveform defines the failure threshold. In addition, the same high-speed I/O interface in different size IC packages can have varying peak current, rise time, and charge transfer with the same withstand voltage. However, a lower generic CDM withstand voltage decreases the peak current and total charge transfer failure absolute maximum rating thresholds. Therefore, high-speed I/Os with a lower CDM rating can be more vulnerable to a charged device type of ESD event, including similar discharges as found during CDM testing.

A.2 Exposed High-Speed I/Os

I/Os exposed in the final product can have varying on-board ESD protection and filters along the signal net, thus, the I/O can be well protected against an ESD stress from the external environment. Alternatively, exposed interfaces can have limited or non-existent on-chip and on-board protection,

depending on the design of product mechanics and PCB layout. Therefore, all exposed high-speed I/Os require good ESD protection precautions in handling, manufacturing, assembly, testing, and system installation phases.

I/Os exposed in the final product can be well protected after cable connection. In a typical case, high-speed interfaces are connected to shielded optical link modules and direct ESD stress events are unlikely during normal operating conditions. Also, high-speed data interfaces require cables with a solid impedance match and these cables have an electric shield that is connected to the electrical ground; thus, the external interface is protected against direct ESD when the cable is attached. Unconnected exposed interfaces should be shielded or protected with protective shielding capacitors during handling and installation until connected.

Cables can have static charges when they are connected to the system. When a data cable is plugged into the product, the ground shield should make the first contact, and in case of a cable discharge event, the shield should conduct most of the ESD current. Cable discharges can also have a fast rise time and high initial peak current pulse resembling a CDM current waveform. In addition, there can be residual ESD stress from charged signal wires inside the cable. On-chip and on-board protection need to protect against these stress pulses.

In summary, shielded data cables and optical data connections reduce ESD risks with exposed high-speed interfaces, but these interfaces can still be vulnerable during component or equipment manufacturing, installation, and handling steps. Data cables should also use connectors with a ground shield which will make the first contact between the cable and connector. Detailed component and product voltage, charge, and discharge current control measures are required when CDM withstand voltage ratings are below 200 volts. For example, it is recommended to ground all cable connectors before joining the cable connector with a high-speed interface. Protection methods are discussed in more detail in Chapter 3.

A.3 Product Internal High-speed I/Os

Product internal high-speed interfaces are typically used to connect sub-assemblies or PCBs together. Therefore, the interface can be on the PCB and board-to-board connectors or data cables can route signals between separate assemblies inside a system enclosure. Also, there are typically high-speed signal traces between ICs and between an IC and the on-board connector. These traces are routed inside the PCB to maintain signal integrity requirements and are visible only via component pads on the PCB. Therefore, these signals are electrically shielded when all components have been assembled on the PCB, except if there are test pads or test connectors along the signal net. These can be contacted during signal testing and tuning phases.

A charged IC, electromechanical connector, or PCB can initiate CDM-like events during component assembly. Here, a destructive ESD event requires that the first contact and ESD current travels through the sensitive I/O signal path. In addition, there must be a voltage difference and a low capacitive coupling between the ESD source and PCB just before the contact. Charged connector assemblies can discharge on the PCB and stress I/Os with less than 20 ps rise time current pulses. These fast pulses can bypass CDM protection devices. Therefore, it is essential to limit electrostatic charge buildup on all assembled components during system manufacturing and assembly.

As a summary, the risk of CDM-like events is limited with product internal I/Os but can exist especially during PCB and system assembly if ESD control precautions are not fully implemented. Detailed component and product voltage, charge, and discharge current control measures are required when CDM withstand voltage ratings are below 125 volts and failure peak currents below 2.5 amperes.

A.4 ESD Risk Classification with High-speed I/Os

Several design and environmental aspects are affecting the decision of high-speed I/O grouping to external or internal. The I/O pin grouping and level of ESD risks can be estimated based on the following examples. Figure A1 has example interfaces marked with letters (a – j).

- External pin when the interface is visible or accessible in the final product:

  Decreased risk when:
  - ― There are onboard protection components between the sensitive I/O and the exposed interface (a, b).
  - ― I/O signal net travels inside a PCB and the exposed interface has a shielded connector (f).
  - ― The exposed interface is connected to an optical module and the module is shielded (f).

  Higher risks when:
  - \+ There are limited or no onboard protection components between the I/O and the exposed interface. The interface can be contacted by the end-user (b, c).
  - \+ The I/O signal net is tested or contacted with pogo pins during frontend, backend, or PCB assembly phase (a, b, c, d, f).
  - \+ Connectors, ICs, or PCBs can have static charges during PCB assembly or final system assembly (a, b, c, f).
  - \+ There are many high-speed I/Os on each PCB or sub-assembly (a, b, f).

- The internal interface which is not accessible in the final product:

  Decreased risk when:
  - ― I/O signal net travels inside a PCB between the IC and product internal interface (e, g, h, i, j).
  - ― There are onboard protection components between the I/O and the interface (j).
  - ― ICs and connector components are physically small in size with low source ESD capacitance (i, j, e)

  Higher risk when:
  - \+ The I/O signal net is tested or contacted with pogo pins during frontend, backend, or PCB assembly phase (d, g, h, i).
  - \+ Connectors, ICs, or PCBs can have static charges during PCB assembly or final system assembly (e, i, g).
  - \+ Charged cables or other conductors are connected to sensitive signal nets (i, g).

+ There are many high-speed I/Os on each IC or PCB (i).

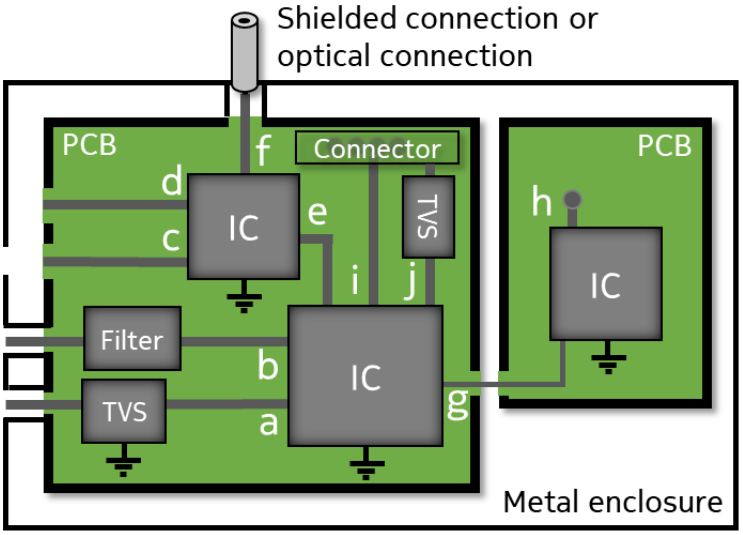

Figure A1: External and internal interfaces with varying levels of shielding and protection.

Appendix B: CDM Qualification of Interface IP Based on Peak Current

Peter C. de Jong, Synopsys

This appendix addresses how the specific nature of CDM demands a dedicated methodology to assess the CDM robustness of interface IP (e.g. USB, DDR, HDMI, MIPI, Ethernet, SATA, etc.) and describes a proposal for an appropriate CDM qualification method for these IP. In contrast to HBM, for CDM the discharge current is not only determined by the tester but depends on DUT properties as well. Consequently, at a given CDM classification voltage, the resulting peak current seen by the IP will generally not be the same on the IP test chip and the final product. In order to enable a valid assessment of the CDM robustness that holds equally for both test chip and product, the CDM discharge peak current is proposed as a measure of the CDM robustness, instead of the voltage.

B.1 Introduction

With the intention to link the product robustness to real-life discharge threats in the factory, all standards for ESD have a classification system that is based on voltage levels. However, for CDM, the discharge (peak) current associated with a given CDM voltage level is not fixed but depends on characteristics of the DUT, like die size, pin count, pin position, package size and others. The peak current is the primary ESD design parameter and when the maximum peak current is exceeded, a failure occurs, regardless of the actual CDM voltage. Consequently, if an interface IP passes the CDM qualification for a certain voltage target on a test chip, there is no guarantee that this IP will pass the same voltage level when integrated into the product. For instance, if the product has a larger package size as compared to the IP qualification test chip, the CDM current at the same qualification voltage level on the product can be higher and the IP might fail.

For this reason, it is not possible for 3rd party IP providers to guarantee a CDM *voltage* specification for IP that is to be integrated into a yet unknown product; only a CDM *peak current* level should be used when the IP is qualified on the test chip.

Qualification of IP based on a peak current is a three-step process:

1. Choose the desired target peak current for qualification testing of the IP. This is explained in Section B.2
2. Establish the relationship between CDM voltage and peak current for the test chip to be used for IP qualification and choose the CDM voltage (V_{QUAL}) which produces the desired qualification current, as explained in Section B.3
3. Perform CDM qualification testing on three test chips at the voltage level V_{QUAL}, determined in Step 2, see Section B.4.

B.2 Choose Target Peak Current

Generally, the desired target peak current is determined by the IP provider and should be aligned with the customer's product requirements: The IP target peak current should comply with the CDM voltage class requirement of the product. Figure B1 illustrates how the CDM current depends on the device size. The CDM discharge peak current is measured for several ball grid array (BGA)

package types for 500 volts CDM stress as a function of the package size [1]. Depending on the BGA package area, the peak current for a 500 volts CDM discharge can vary from less than 4 amperes to over 10 amperes.

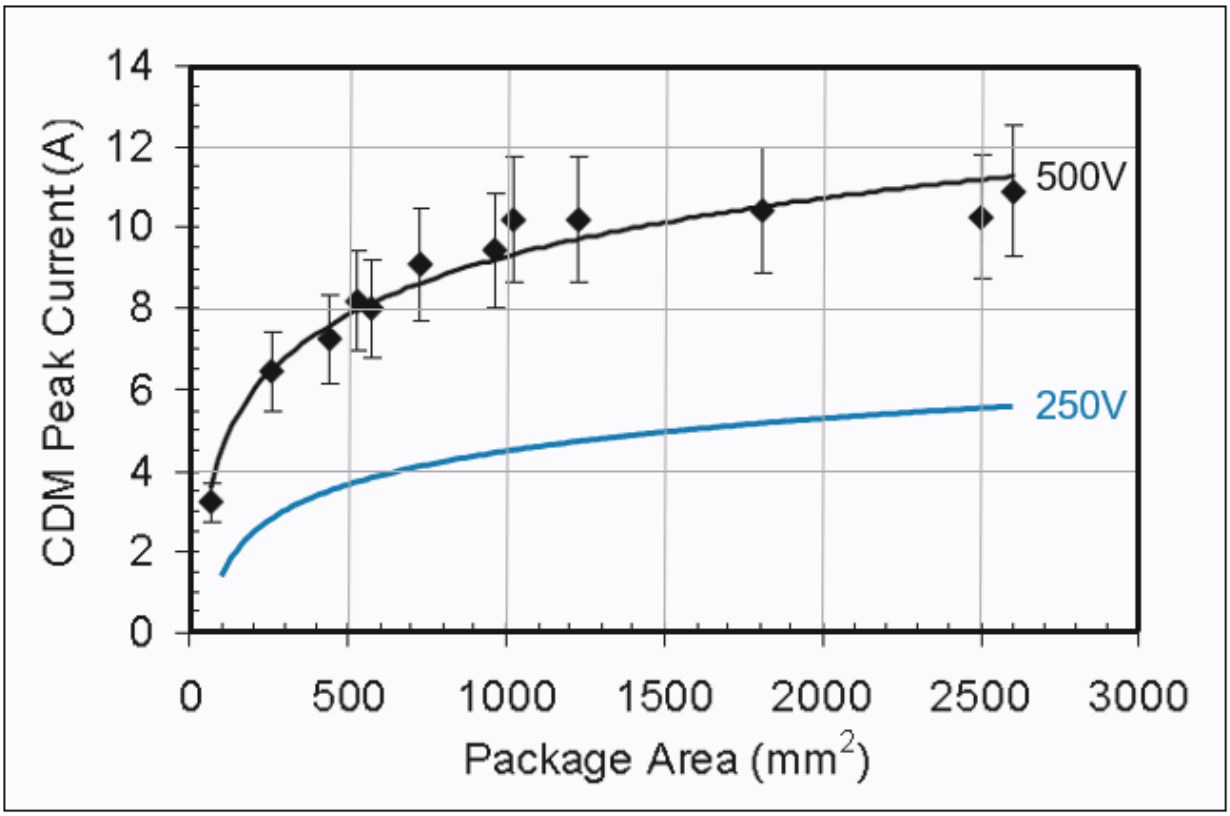

Figure B1: CDM peak current dependency of package area for BGA types at 500 V (measured) and 250 V (derived)

Since the peak current for a given package (capacitance) is linear with the CDM voltage, the curves for other CDM levels can easily be derived, see for instance the 250 volts curve in Figure B1. The scaled 250 volts curve reveals that for practically all package sizes the peak current will stay below 6 amperes, while for package size up to ~1500 mm^2 the peak current does not exceed 5 amperes. Similarly, a 125 volts target will be met with 2.5 amperes peak current criterion for most package sizes. Table B-I summarizes the maximum peak currents, appropriate to meet the most common CDM voltage classes for larger package sizes.

Table B-I. CDM peak current target levels for IP qualification, corresponding to the most used CDM Classification Levels according to JS-002 for larger package sizes

Classification Level JS-002	Test Condition [V]	Peak Current Target [A]
C0b	125 to < 250	2.5
C1	250 to < 500	5
C2a	500 to < 750	10

Presently, 250 volts is considered a realistic and safe CDM target level for handling today's products using basic ESD control methods. This means that a peak current target of 5 amperes can be recommended as an appropriate design and qualification target for IP meant to be used in large (up to ~1500 mm^2) package products. Lowering of the peak current target is possible if the product package is relatively small, e.g. < 1000 mm^2. In that case, it is recommended to derive the expected peak current from an existing product in a comparable package or, if not attainable, estimate the peak current, using an I_{PEAK} vs. package size relationship, like shown in Figure B1. As discussed in Chapter 5, for ultra-high-speed interfaces a peak current target of 5 amperes is not realistic and a target of 2.5 amperes is recommended.

B.3 Qualification Voltage Setting from Test Chip CDM Voltage and Peak Current Relationship

In order to choose the voltage level (V_{QUAL}) for the desired target qualification peak current, the next two steps should be followed:

1. Determine the correlation between CDM voltage and peak current for the test chip
2. Choose the CDM voltage corresponding with the target qualification peak current

Step 1: Determine the correlation between CDM voltage (V_{CDM}) and peak current (I_{PEAK}):

- Stress all device pins (IOs and power/ground pins) at different CDM voltage levels
- Monitor the discharge peak current waveform and determine I_{PEAK} for each pin

It is not critical which voltage levels are chosen for testing or even whether the device passes or fails at certain CDM voltage levels. A good practice is however to have read-points below and above the target CDM voltage. Further, avoid the inherently large variability of the peak current at very low voltage levels (< 150 volts). If it is necessary to develop a relationship at these lower voltages, multiple data points may need to be taken and averaged.

Step 2: Choose the CDM voltage (V_{QUAL}) corresponding with the desired qualification peak current (I_{TARGET}):

- Calculate per CDM voltage level the average I_{PEAK} of all stressed pins
- Find the linear curve for CDM voltage vs. average peak current
- Use the I_{TARGET} and the discharge current plot, see the example with I_{TARGET} = 6 amperes in Figure B2, to determine the qualification CDM voltage (V_{QUAL})

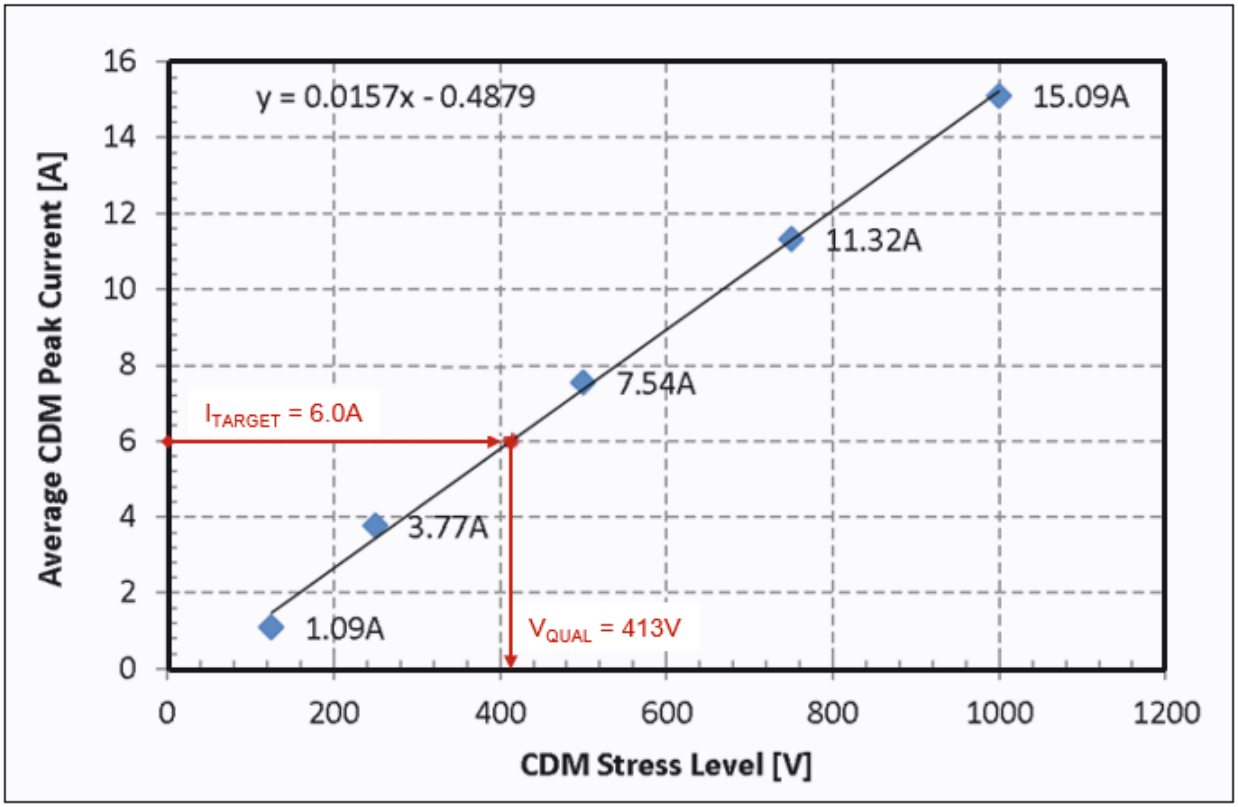

Figure B2: Example of an I_{PEAK} vs. V_{CDM} plot, used to determine the voltage level V_{QUAL} for a peak current target I_{TARGET}

The result of the procedure at this point is that the CDM qualification voltage (V_{QUAL}) of the DUT (in this case the IP test chip) that corresponds to the target qualification peak current (I_{TARGET}) is determined.

B.4 Perform CDM Qualification Testing

Finally, the actual qualification should be performed at the target peak current (I_{TARGET}). For the appropriate qualification stress level, the CDM tester voltage should be set to the V_{QUAL} level as determined in the previous step. To comply with the CDM standard, three devices are used for the CDM qualification test. The pass/fail test data is essential and determines the qualification result.

- Apply pre-stress parametric and functional tests
- Use V_{QUAL} as voltage setting for the CDM tester
- Stress all pins at V_{QUAL} CDM level using three devices
- Apply post-stress parametric and functional pass/fail tests

Note that a prerequisite for the IP qualification method is that the test chip size is sufficiently large so that the target peak current is reached at a CDM voltage below the practical limit of 1000 volts.

B.5 Summary

Since for CDM, the discharge current at a given voltage level is a function of DUT properties, a standard CDM qualification of IP to a voltage class is practically useless. This appendix proposes a qualification method that is based on a CDM peak current as a qualification parameter. Together with the basic properties of the final product, like the dimensions of the package, this enables the end-user to determine whether the IP, when integrated into the product, is expected to pass the product's classification level. A target peak current of 5 amperes can be considered valid for a product specification of 250 volts for a wide range of package sizes. For ultra-high-speed I/Os the recommended target is 2.5 amperes peak current.

References

[1] A. Jahanzeb, Y-Y. Lin, S. Marum, J. Schichl, C. Duvvury, "CDM Peak Current Variations and Impact upon CDM Performance Thresholds", Proc. EOS/ESD Symposium 2007, pp. 283-288.

Appendix C: CDM Qualification and Test Methods

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This appendix summarizes existing CDM ESD test methods and standards and differences between them and demonstrates the impact of the differences on product test results. It explains the weaknesses of the existing test equipment and methods that lead to inconsistencies and non-repeatability issues in product test results. This appendix demonstrates that these deficiencies are in part attributable to missing specifications in the standard test methods, such as the size of the charge plate or the ground plane, which results in a strong dependency of test results on the tester manufacturer, type, and setup parameters. It will show that reproducibility and non-repeatability issues are also due to fundamental properties of the currently widely used air discharge test method. This variability increases at sub-200-volt test levels, prompting the development of relay-based test methods. These emerging test methods are briefly described here. This appendix will also demonstrate that the current CDM voltage classification levels apply more stress to larger and thinner devices than to smaller and thicker devices for the same classification level.

C.1 CDM Qualification Standards

There are currently four widely used CDM qualification standards in use, as listed in Table C-I. Fundamentally, however, there are only two base standards, ANSI/ESDA/JEDEC JS-002, hereafter for this appendix referred to as "JS-002", issued jointly by the Electrostatic Discharge Association (ESDA) and JEDEC [1], and the JEITA CDM standard issued by the Japanese Electronics and Information Technology Industries Association (JEITA) [4]. The AEC CDM standard [3], issued by the Automotive Electronics Council (AEC) references JS-002 for all equipment, calibration, and test procedures, but adds several additional requirements such as enhanced CDM level requirements for corner pins and the use of three stresses per pin, rather than a single stress per pin. The IEC CDM standard [2], issued by the International Electrotechnical Commission, is an adoption of JS-002-2014 with an added informative annex, which includes a core of the JEITA CDM standard.

Table C-I: CDM Qualification Standards

Standard	Issuing Body	In this appendix
ANSI/ESDA/JEDEC JS-002-2018 [1]	Joint ESDA & JEDEC	JS-002
EIAJ ED-4701/300-2 Test Method 305 [4]	JEITA	JEITA CDM
AEC - Q100-011 Rev-D [3]	AEC	AEC CDM
IEC 60749-28:2017 [2]	IEC	IEC CDM

Both JS-002 and JEITA CDM are non-socketed test methods in which the DUT is placed on top of a thin FR4 insulator on top of a field plate, as shown in Figure C1. The two test methods differ in terms of how the devices are charged and in the discharge path.

All ESD events are governed by two fundamental properties, a capacitor that becomes charged and a current discharge path. CDM ESD events are different from HBM events, which are simulated by the HBM test standard JS-001 [5]. In HBM the charged capacitor is the human body's capacitance and the discharge path is dominated by body resistance. Both are largely independent of the DUT, both in for a "real world" event and in the test method where the body capacitance is represented by a 100-pF capacitor and body resistance is represented by a 1500 Ω resistor. The capacitance relevant for CDM is the capacitance of the DUT to its surroundings, typically a nearby ground plane. During CDM ESD events, arc resistance is a significant part of the discharge path, but the chip and package impedances also significantly influence the discharge current path.

A CDM standard test method must address the following issues:

1. Produce a capacitance that scales with the IC's size and reproduces the IC device's capacitance to its surrounding during a real-life event.
2. Provide a method to rapidly transfer charge to or from this capacitance through each individual pin of the IC device while:
    a. Creating a reproducible discharge event.
    b. Maintaining a low impedance path for the discharge current.
    c. Ensure that a discharge event has occurred.
    d. Accurately measure the discharge current.

In both JS-002 and JEITA CDM, the DUT is placed in a "Dead Bug" or "pins up" position, on top of a thin insulator on top of a metal plate, as shown in Figure C1. This creates a capacitance between the DUT and its surroundings that depends on the size of the DUT.

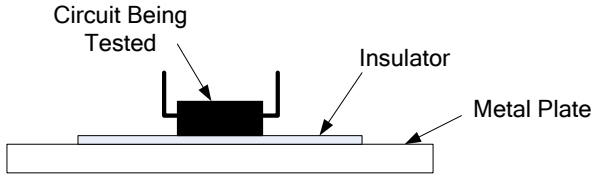

Figure C1: Capacitor formed by placing the IC on top of the metal plate.

In both test methods for each pin, the DUT is placed at a high potential and then the pin under test is rapidly grounded, creating a simulated CDM event. The two test methods differ in how the DUT is placed at a high potential and how the device is grounded. JS-002 uses field induction to place the device at a high potential and the DUT is grounded with an arc to a robotically controlled pogo pin. JEITA CDM uses a direct charging approach to elevate the device potential and grounds the DUT through a relay. (JEITA also has a field-induced option, but this is not the preferred method.)

C.1.1 Charging Method

Two different charging methods are illustrated in Figure C2. In the direct charging method, contact is made with a robotic probe to one pin (typically a substrate-connected pin) of the IC device. The

electrical potential of the IC device is elevated to a high voltage level by connecting a high voltage supply to this pin through a high-value resistor, usually many megaohms.

For the field-induced CDM charging method, a metallic ground plane is placed over the IC. The metal plate under the device is called the field plate. The electrical potential of the field plate is controlled with a high voltage power supply through a high-value resistor. If the capacitance between the field plate and the IC device is much higher than the capacitance between the IC and the ground plane, the electrical potential of the IC device will closely follow the electrical potential of the field plate. The net result of raising the voltage level on the field plate is to raise the electrical potential of the IC device relative to the ground plane above it. Unlike the direct charging method, the field-induced method does not transfer charge to the device under test during this "charging step".

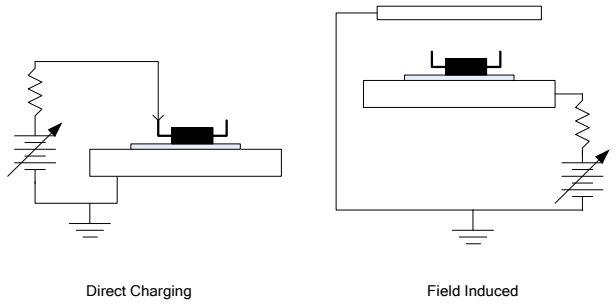

Figure C2: Direct charging and field-induced charging method.

C.1.2 Discharge Event

Discharge of a directly charged IC device can occur in one of two ways, as illustrated in Figure C3. A grounding electrode may make contact with the pin under test, by creating an air discharge, or the pin may be discharged through a relay. In some cases, the same electrode is used to charge and discharge the IC device as is illustrated in Figure C3.

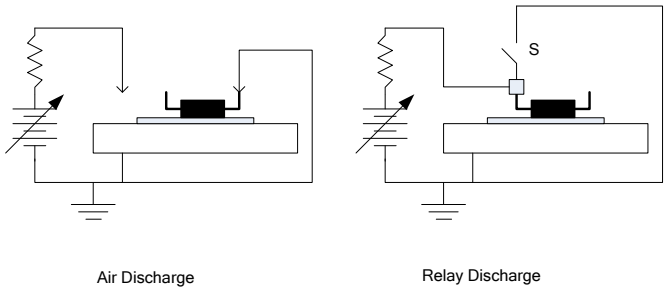

Figure C3: Discharging of a directly charged IC.

In the field-induced method, the stress event is more properly defined as a grounding of the device under test, rather than a discharge, since the IC device actually becomes charged when it is grounded. This method is illustrated in Figure C4. In the center of the ground plane is a spring-loaded pin, commonly called a pogo pin. The pin is in the center of a 1Ω resistor. As the pogo pin approaches the IC device's pin under test, high electric fields occur between the two electrodes.

When a critical electric field strength is reached, the air will breakdown and an arc will form between the grounded pogo pin and the IC device's pin. A charge transfer will now abruptly occur to ground through the pogo pin. The discharge event results in a net charge on the IC device as the grounding of the pin actually charges up the IC device.

As the discharge current flows through the pogo pin and 1Ω resistor, the discharge current can be measured as a voltage drop across the resistor and can be recorded either by an oscilloscope or a pulse detection circuit.

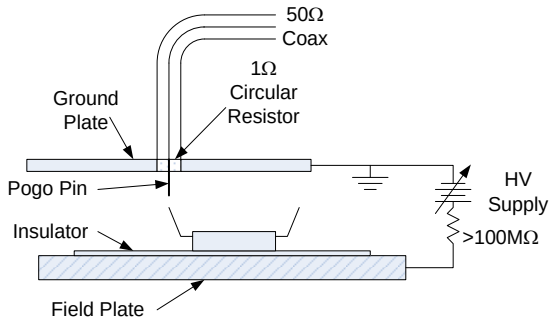

Figure C4: Field-induced CDM.

The two test methods give similar results and provide meaningful metrics for evaluating a DUT's robustness from CDM type stress in a manufacturing environment. The voltage levels from the two test methods should not, however, be considered equivalent. The differences in charging methods mean that the severity of stress as a function of device size differs between the two methods. The use of a relay in the JEITA CDM standard creates a more reproducible discharge, at the expense of creating a discharge path with higher inductance, and therefore stress pulses with lower frequency characteristics. There are also significant differences between the calibration procedures in the two test methods.

C.2 Comparison of Existing CDM Industry Standards

C.2.1 Comparison of Key CDM Standard Features

Appendix C.1 of this White Paper gives an excellent summary of the existing industry CDM test standards. It states that the JS-002-2018 standard and the JEITA EIAJ ED-4701/300-2 Test Method 305 standard are the two base CDM test standards (with their distinct tester differences) in force today. Therefore, for purposes of tester hardware, oscilloscope bandwidth, calibration modules, and tester waveform parameters, which are considered in the next section, the remainder of Section C.2 will mainly compare these two base (JS-002 and JEITA) standards. The primary difference between AEC and JS-002 is the requirement to complete 3 discharges rather than 1. The comparison of all 3 standards is shown in Table C-II.

Table C-II: Comparison of key CDM features of different standards.

Organization	**ESDA / JEDEC / IEC**	**AEC**	**JEITA**
Standard	ANSI/ESDA/JEDEC JS-002-2018	AEC - Q100-011 Rev-D	EIAJ ED-4701/302A 305D
Charging Method	Field-induced	Field-induced	Direct
Calibration Modules	Metal Coins	Metal Coins	Metal Coins
Calibration Module Thickness	1.27 ± 0.05 mm	1.27 ± 0.05 mm	1.3 ± 0.1 mm
Calibration Module Diameter	8.89 ± 0.127 mm (small) 25.4 ± 0.127 mm (large)	8.89 ± 0.127 mm (small) 25.4 ± 0.127 mm (large)	9.0 ± 0.1 mm (small) 25.0 ± 0.2 mm (large)
Calibration Module Capacitance	6.8 pF ± 5% mm (small) 55 pF ± 5% mm (large)	6.8 pF ± 5% mm (small) 55 pF ± 5% mm (large)	6.8pF, 55pF (Reference) (Do not need physical dimensions due to adjustment of the calibration current waveform)
Insulator Thickness (mm)	0.381 ± 0.038	0.381 ± 0.038	0.40 ± 0.04
Insulator Dielectric Constant	4.7 ± 5%	4.7 ± 5%	4.0 ± 5% (@ 1GHz)
Ground plane size	63.5 x 63.5 ± 6.35 mm	63.5 x 63.5 ± 6.35 mm	No specified shape and size (No shape and physical dimensions due to adjustment of the calibration current waveform)
Discharge	Air	Air	Relay
Current measured during CDM stress	Yes	Yes	Not required
Number of Discharges + & -	1	3	1
Number of Parts	3	3	3
Calibration Voltage Levels	125, 250, 500, 750, 1000	125, 250, 500, 750, 1000	125, 250, 500, 750, 1000

C.2.2 Comparison of Waveform Parameters

Table C-III: Comparison of CDM current waveform properties for different standards (JS-002 & JEITA) at 500 V: peak currents, rise times, and full width at half maximum (FWHM).

Standard (Scope bandwidth)	**Small Module**				**Large Module**			
	C [pF]	**I_{PEAK} [A]**	**T_{RISE} [ps]**	**FWHM [ns]**	**C [pF]**	**I_{PEAK} [A]**	**T_{RISE} [ps]**	**FWHM [ns]**
JS-002 (1 GHz)*	6.8	5.1 ± 15%	< 350	325-725	55	10.7 ± 15%	< 450	500-1000
JS-002 (6+ GHz)*	6.8	7.2 ± 15%	< 250	250-600	55	12.1 ± 15%	< 350	450-900
JEITA (≥ 2 GHz)**	~6.8***	4 ± 10%	≤ 300	≤ 0.6	~55***	5.5 ± 10%	≤ 400	≤ 800

* JS-002 is the tester platform now used in the IEC and AEC Q100 / Q101 CDM test standards.

** JEITA peak current values for the standard verification method. There is an alternative method specified in the standard that has different peak current values.

*** JEITA specified the diameter of the coin used for the verification, not the actual capacitance. The size is comparable to the values defined in the JS-002 specification.

Table C-II and Table C-III demonstrate that there are differences between these standards that make CDM test results difficult to compare. It is generally true though that the most critical CDM waveform parameter that leads to IC device failures is the peak current, I_{PEAK}. A comparison of I_{PEAK} values measured when stressing metallic coins is shown in Figure C5 comparing JS-002 [1] to JEITA [4]. There are at least two factors that affect the difference between the two standards in terms of peak current versus coin area. The tester geometries are considerably different between the two test methods. Additionally, in the JEITA standard, the preferred method is direct charging, rather than field-induced charging. In direct charging the device under test always reaches the applied voltage. In the field-induced method, the device potential depends on the relative sizes of the device to field plate and device to ground plane capacitances. If for some devices the device to ground plane capacitance is not significantly lower than the device to field plate capacitance, the device potential will be considerably below the voltage applied to the field plate. Rise time can also be important depending on the turn-on time of protection circuitry and the full width at half height can relate to the total energy deposited into the device being tested.

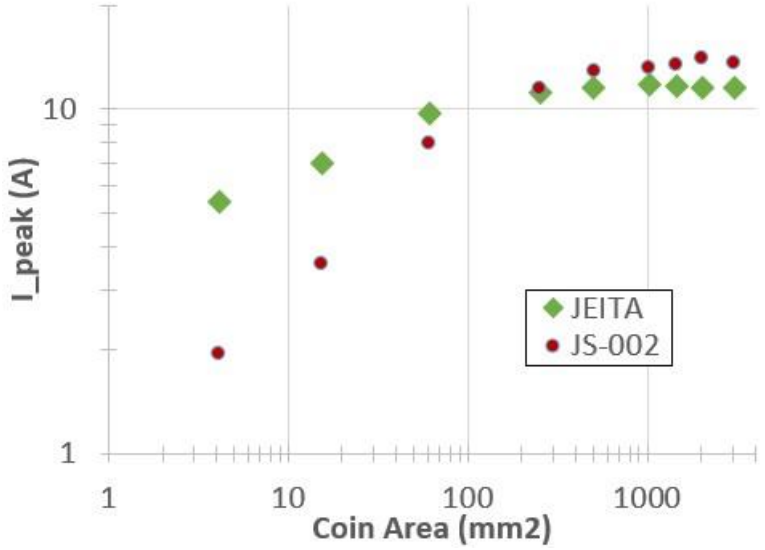

Figure C5: Comparison of calibration module expected CDM peak currents for JS-002 (6 GHz BW oscilloscope) and JEITA (with 2 GHz BW oscilloscope) standards.

C.2.3 Insulator on Field Plane – Thickness and Dielectric Constant

One of the main differences that directly affects the peak current is the insulator thickness on the field charging plate. The JS-002 standard uses a 0.381 mm insulator (harmonizing from the now obsolete JEDEC JESD22-C101 standard) while the JEITA standard calls for a 0.4 mm insulator. Also, the dielectric constants used on the field plane dielectric differ between the JS-002 (nominally 4.7) and JEITA (4.0 +/- 0.5) standards. Significant changes to the package area and thickness will cause more of a change in the capacitance in the JS-002 than in the JEITA standard and this is reflected in Figure C5.

C.2.4 Accuracy of Verification Modules

JS-002, in the harmonization of the ESDA and JEDEC test standards/calibration modules to a single tester/calibration module construction, harmonizes the calibration modules to the JEDEC large and small calibration module specifications.

In Table C-III the specifications for the small and large modules are slightly different for the JS-002 compared to the JEITA standard. JEITA made a change to their standard in 2004 to make the physical dimensions closer to JEDEC which does help in the comparison of waveform parameters.

C.2.5 Oscilloscope Bandwidth

Another area where the measurement accuracy of I_{PEAK} can cause unwanted variations is in the specification of oscilloscope bandwidth in the standards. When the CDM standards were first written, the cost of a high bandwidth oscilloscope that measured in the gigahertz frequency range was extremely expensive. As a consequence, the bandwidth required for the oscilloscope used for the verification was relatively low. Today, the costs for higher bandwidth oscilloscopes have decreased dramatically, and some changes to the JS-002 bandwidth requirements reflect this. Table C-III shows the test equipment requirements for the different CDM standards. JEITA requires an oscilloscope with a bandwidth of 2 GHz or more. JS-002 requires high speed (>= 6 GHz) for equipment qualification and for when tester hardware changes are made and allows the use of 1

GHz bandwidth scopes for routine (daily / periodic) checking (provided the 1 GHz oscilloscope waveforms are first correlated to the high bandwidth scope to determine relative differences between the two waveforms). Measurements at 1 GHz are quite marginal (and have been shown to filter the response significantly) for the speed of CDM events and there can be considerable differences in waveforms when captured with greater than 3.5 GHz bandwidth oscilloscopes [9]. This variation in measurement bandwidth confirms that discharge current waveforms have much more variability than the standards waveform specification values imply. These differences in oscilloscope bandwidth were a primary reason JS-002 included waveform parameters for 1 GHz and 6+ GHz bandwidth.

C.2.6 Size of Ground Plane

The JS-002 (and now AEC Q100-011D by reference) method specifies fixed ground plane dimensions of 63.5 +/- 6.35 mm for this setup parameter. The JEITA standard test platform does not incorporate a "ground plane" per se but a fixed metal bar. This can lead to differences in the tester "effective capacitance" when considering ground plane to field plate and DUT to ground plane capacitances. The differences in the ground plane geometry are one of the factors creating the differences between the standards in Figure C5 and as shown in [10] [12].

When the CDM standard was first developed in the late 1980s and early 1990s, the largest IC device package capacitance was less than 30 pF. Hence, the specified requirements were more or less adequate as the dependence of peak current on device size is a linear function for small capacitive values ranging from 0 to 40 pF. Today, very large IC packages with capacitances in the nanofarads range are becoming more commonplace. The introduction of these large packages has resulted in hardware configuration problems where the JS-002 ground plane cannot completely cover the package. Hence, the failure of the ground plane to fully cover large devices is one factor in the saturation of the peak current at capacitance values greater than 40 pF [12]. As a consequence, the test results for these large devices can vary significantly between JS-002 and JEITA.

C.2.7 Air versus Contact Discharge

The difference in the discharge current waveform between air discharge and discharge in a relay can be significant. Relay switch discharges are expected to be more consistent, but the added inductance of the relay may increase pulse rise time, reduce peak current at a given CDM voltage, and increase ringing. Any attempt to convert the single relay into a relay matrix network will introduce unwanted tester RLC parasitics and change the fundamental properties of the CDM discharge current waveform.

Section C.4 describes new contact-based CDM test methods considering these relay issues in the development of their tester platforms.

C.2.8 Conclusions: CDM Standards Comparison

This comparison of the existing CDM test standards highlights significant differences in the tester setup parameter specification and actual current waveform measurement methods. These differences are significant enough that a product CDM fail voltage level would be unique to that test method. Applying a simple scaling ratio to calculate the failure level between the standards would not produce consistent and correct results. JS-002 is a significant advance to harmonize to a single CDM test standard throughout the industry, with most other standards bodies having harmonized to JS-002.

C.3 Sources and Impact of Zap to Zap and Tester to Tester Variation

The stress current generated by CDM testers can differ greatly from zap to zap and tester to tester, even when following the same test standard. Consequently, product pass and fail voltages can vary widely between different CDM simulators, even when the same standard is applied. This section examines the sources of the stress current variation.

C.3.1 Tester to Tester Variation

CDM ESD standards primarily define the waveform requirements and offer fewer restrictions on the hardware setup itself. This decision has been consciously made by the standards committees to ensure the manufacturability of the CDM testers and at the same time ensure the integrity of the waveforms. But this implicit specification causes additional variations in the discharge current waveforms since the tester manufacturers have been given a high degree of freedom to design and specify the setup parameters for the CDM testers. They can implement different combinations of field charging plate size, pogo pin length, and inductive and capacitive parasitics to produce waveforms that comply with a certain standard. However, the stress imposed on a real product under test can vary significantly for the different tester setups.

C.3.1.1 Variation in High-Frequency Characteristics

When the original CDM specifications were written a 1 GHz oscilloscope was the highest bandwidth oscilloscope that could reasonably be required in a testing laboratory due to economic issues. This 1 GHz oscilloscope was capable of demonstrating the day-to-day functionality of the CDM tester at least for the lower frequency properties of the fast-transient current pulse. However, new research shows that discharge current waveforms using a 1 GHz oscilloscope are unable to capture the important CDM discharge waveform properties [10]. Consequently, signals can appear very similar when measured with the 1 GHz oscilloscope, while they can look very different when measured with a 6 GHz oscilloscope. These hidden differences can lead to different product test results between different testers or tester setups, even if the waveform captured from these testers with a lower bandwidth oscilloscope appears to be very similar. An example of a “clean” waveform signal as measured with the limited 1 GHz bandwidth oscilloscope is shown in Figure C6. A waveform from the same tester, measured with a 6 GHz oscilloscope is shown in Figure C7. Significant distortion in the waveform is apparent in the higher bandwidth measurement.

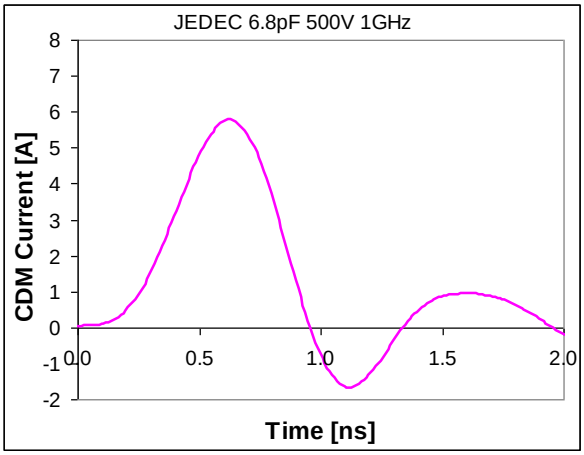

Figure C6: CDM discharge waveform, captured with a 1 GHz (5 GS/sec) Tektronix oscilloscope: legacy JEDEC JESD22-C101 standard, Oryx Orion CDM tester, 6.8 pF verification module, 500 V.

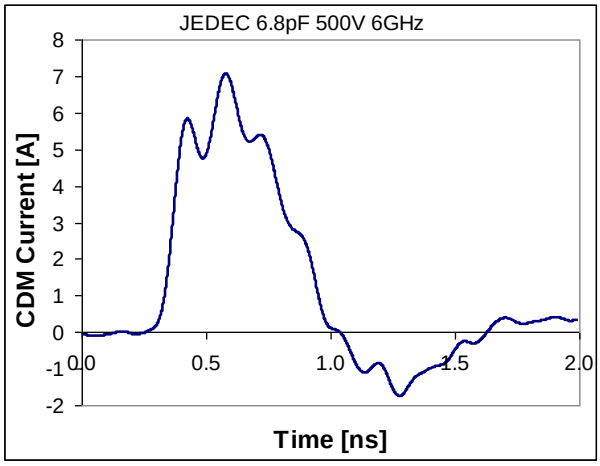

Figure C7: CDM discharge waveform, captured with a 6 GHz (10 GS/sec) Tektronix oscilloscope: legacy JEDEC JESD22-C101 standard, Oryx Orion CDM tester, 6.8 pF verification module, 500 V.

The new JS-002 standard now encourages the use of 6 GHz BW scopes and requires it for the initial tester qualification conducted by the manufacturer as well as during periodic calibration and when major changes or repair are performed on the tester. This helps to ensure there are no high-frequency anomalies that might not be visible at 1 GHz. As shown in Table C-III, the peak current and pulse shape properties are specified differently at 1 GHz and 6 GHz. However, subtle factors like multiple small peaks (as seen in Figure C7), the width of the pulse at regions other than the mid-point of the waveform (e.g. at the 80% and 20% point), and a minimum rise time are not specified. Recent works have also shown that waveform differences can occur in spectrums unmeasurable by 6 GHz oscilloscopes. These high-frequency components of the waveforms can be significant causes of tester-tester variation in test results [17, 18].

The new JS-002 standard also prohibits the use of ferrite beads or other passive devices in the test head. In years past such elements had been inserted by manufacturers to achieve the waveform specifications at 1 GHz bandwidth, but these resulted in highly variable upper bandwidth response.

C.3.1.2 Peak Current Range

All standards allow for a significant variation of the measured peak current during a discharge on the verification module from the nominal peak current. JEITA allows up to ± 10% [4], while JS-002 allows up to ± 15% at higher voltages and up to ± 25% at the lowest test voltage [1].

As a consequence of the wide tolerance in I_{PEAK}, testers can be set up at the lower end or higher end of the allowed current window and the same tester can stress a device with a significantly higher peak current, depending on the setup. An example for the range of allowed peak currents from the JS-002 standard is depicted in Figure C8 at 250 volts, and in Figure C9 at 125 volts. When one considers that the allowed variation of the verification module capacitance is ± 5% (See Table C-II), the allowed variation in peak current from tester to tester further expands as indicated by the red dashed lines.

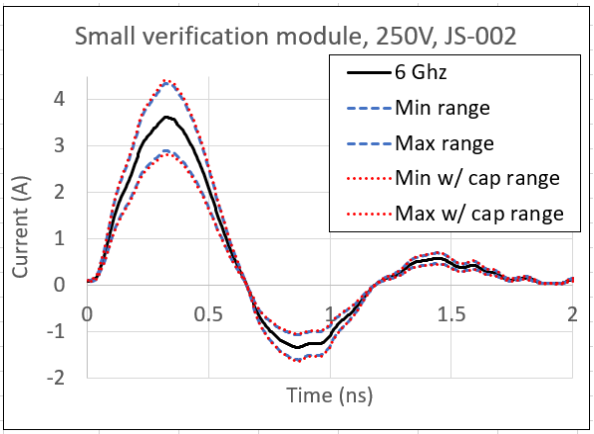

Figure C8: CDM discharge waveform for the small verification module using JS-002 at 250 V with a 6 GHz oscilloscope. The blue waveforms represent the maximum and minimum allowed peak current (± 20%). The red adjusts these to account for the allowed capacitance variation.

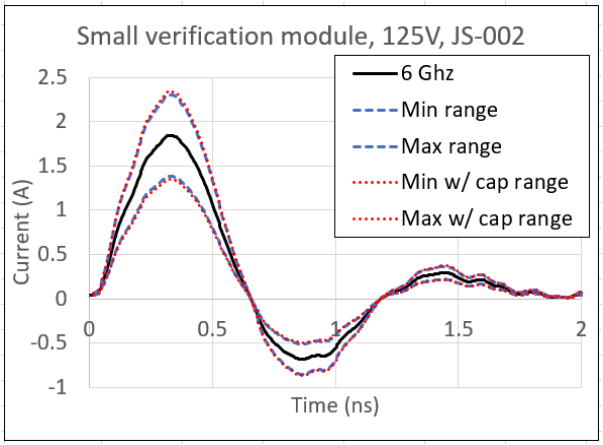

Figure C9: CDM discharge waveform for the small verification module using JS-002 at 125 V with a 6 GHz oscilloscope. The blue waveforms represent the maximum and minimum allowed peak current (± 25%). The red adjusts these to account for the allowed capacitance variation.

C.3.2 Zap to Zap Variation

C.3.2.1 The Downsides of Mimicking Real-World Discharges

The non-socketed CDM tests as specified in the various CDM standards (Table C-I) require or allow either a “non-contact mode” or “air” discharge mode of operation, where the discharge occurs across a small air gap after the air dielectric breaks down between the test pin and the approaching discharge pin. The non-contact method more closely represents real-world discharge conditions of the device, compared to the "contact mode" discharge where switching a mercury relay initiates the discharge.

The major drawback of the non-contact mode discharge method is that the properties of the discharge arc are influenced by both test equipment and environmental factors. The material, surface area, and geometries of the CDM pogo pin and device pins, the approach velocity of the pogo pin, and climatic conditions such as temperature and humidity all combine to influence the discharge current waveform properties. In addition to that, the formation of the spark is a statistical process; the resistance can vary significantly from discharge-to-discharge.

Furthermore, when testing IC devices with very small pin-to-pin spacing at higher voltages, discharging to a specific pin can be problematic as making a contact with the small device pins is difficult and arcing to neighboring pins is likely. Reducing the size of the pogo pin’s dimensions does not help as the electric fields around the electrode tip’s head increase dramatically as the head is made smaller. The higher electric fields cause a premature dielectric breakdown at variable distances between the pogo pin and the pin under test. This variation can introduce an unpredictable arc resistance which can cause additional oscillations in the peak current values.

C.3.2.2 Zap to Zap Variation at a Given Voltage

The available commercial CDM stress simulators are designed to reproduce the CDM event as realistically as possible. The large deviations in the discharge currents resulting from non-contact mode discharges are currently accepted in the industry.

There can be significant variations in the CDM peak discharge current when a product is stressed several times on the exact same pin. In Figure C10 and Figure C11 Jahanzeb [10] and Brodbeck [11] show significant peak current variations ranging by ± 20% in the first paper and + 25% and - 60% for the second paper. This data clearly illustrates the extreme statistical variation in the arc discharge within the stress of a single pin.

If the ground pogo-pin discharges on different positions on the IC device's lead finger (Figure C12) then the rise time, peak current, and pulse frequencies are also affected [11].

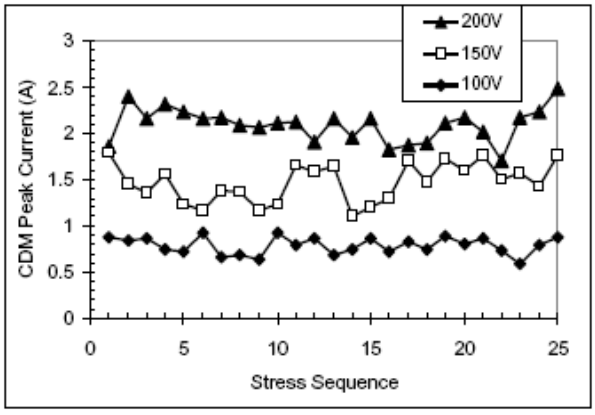

Figure C10 (Jahanzeb et al. [10]): Peak CDM discharge current for a sequence of 25 pulses on the same pin. The variation of the discharge current is depicted for three different CDM voltages. The device package size is 10 mm x 10 mm.

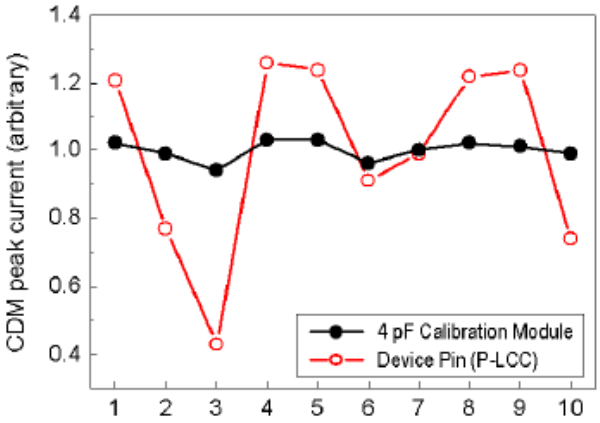

Figure C11 (Brodbeck et al. [11]): Normalized CDM discharge peak currents for a component (P-LCC) and a verification module (4 pF legacy ESDA standard [8]) for ten consecutive discharges (RCDM, 1.5 kV, 60% RH).

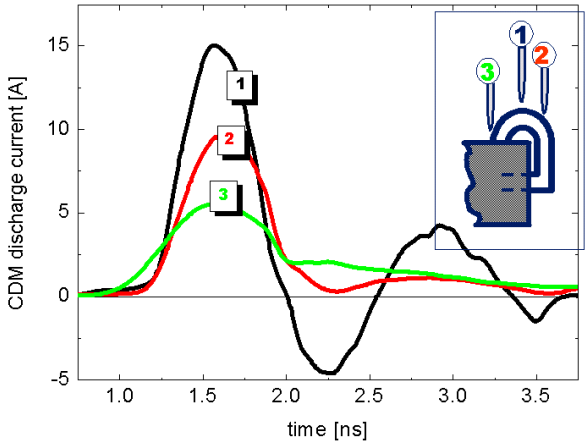

Figure C12 (Brodbeck et al. [11]): CDM discharge current waveforms for three different positions between the discharge pin of the test system and the pin of the device (RCDM, legacy ESDA test standard [8], 60% RH).

C.3.2.3 Variation at Sub-200 Volt CDM Levels

It has been shown that the variation caused by the spark will increase as the precharge voltage decreases. In [14] Jack showed that the variation as a percentage of the mean increases significantly for precharge voltages below 200 volts (Figure C13). As indicated elsewhere in this document, it will become increasingly necessary to design for CDM protection limits below 200 volts as I/O signaling rates increase and technology feature sizes decrease. Such significant zap-zap variation will become extremely impactful at these low voltage levels. As shown in Figure C14, this variation is so large that the stress current can be non-monotonic with precharge voltage. Despite 25 volt increments to Vpre from 125 volts to 175 volts, I_{PEAK} actually decreases in some cases (red arrows in Figure C14). Increasing Vpre from 175 volts to 200 volts causes more than a 60% I_{PEAK} increase. These data indicate that even a 50-volt step size is too small to avoid non-monotonic behavior; this makes it difficult to determine the true Ifail of the pin.

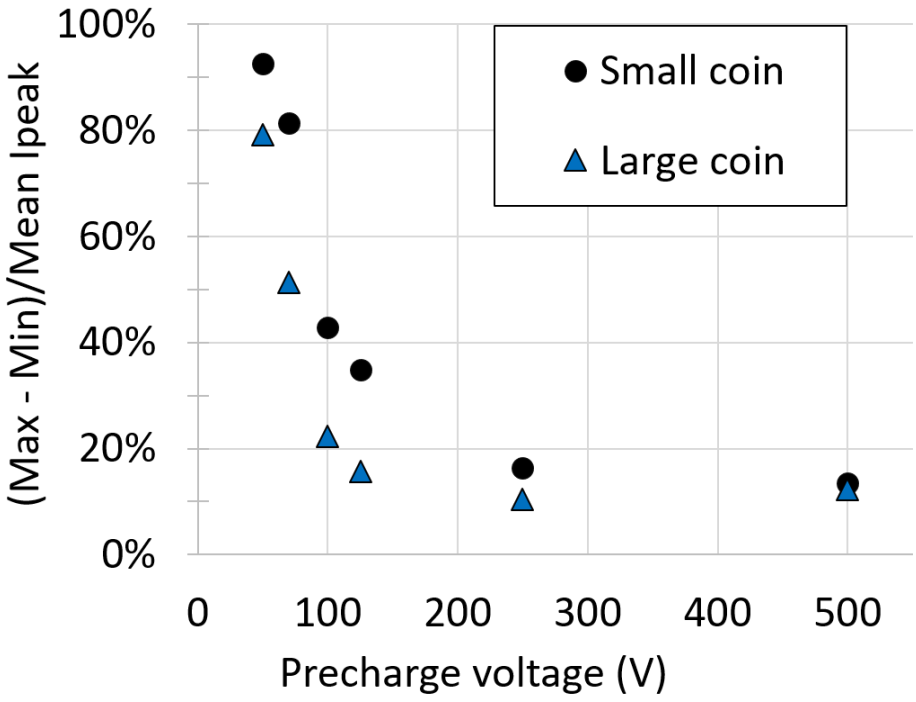

Figure C13 [14]: I_{PEAK} maximum - minimum (top) and the standard deviation (bottom) of 50 zaps to JS-002 calibration coins as a percentage of the mean; 26% relative humidity. Data were taken on an Orion2 FICDM system using an 8 GHz oscilloscope.

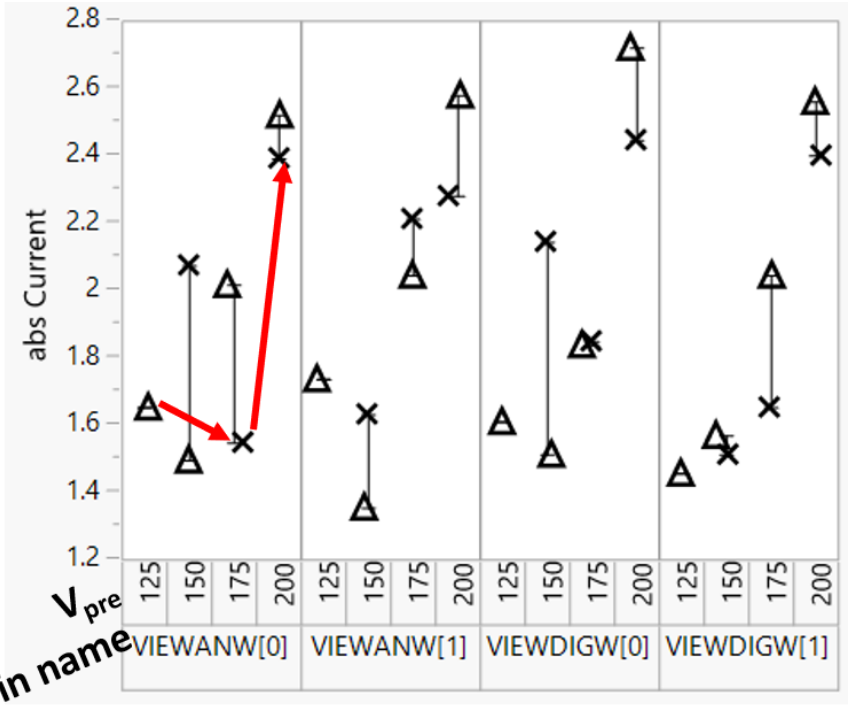

Figure C14 [15]: Measured I_{PEAK} from stress to a BGA packaged test chip at a given Vpre using JS-002. Data from four different I/O pins is shown coming from single zaps to two units. Each unit is represented by a different symbol. A non-monotonic relationship with Vpre is exhibited (red arrow).

C.3.3 Correlation Data for Different CDM Testers with the Same Standard

Given all of the sources of variation identified in this appendix, it should not be surprising that test results can vary from run to run and tester to tester, even within the same standard. To demonstrate this point, a CDM ESD correlation study was performed at ESD labs at Freescale using 130 nm CMOS IC devices. All devices were tested according to the legacy JEDEC JESD22-C101D standard [7]. The purpose of the correlation study was to compare CDM failure levels for the same IC devices tested on multiple CDM testers in different labs. CDM discharge current waveforms using the verification module measured before and during the evaluation tests met the legacy JEDEC standard specification. The test results showed the lowest failing voltage was at 650 volts for units tested on Tester1 in Lab 3, while units tested in Lab 1 and Lab 2 passed voltages as high as 750 volts. The test results differences (Table C-IV) were greater than 150 volts among the different fully calibrated test equipment. Measuring the peak currents resulting in a failure on calibrated systems would have provided deeper insight and would likely have explained the discrepancy in the test results.

Table C-IV: Freescale's JEDEC Multiple ESD Lab Correlation Test Results

	250 V	500 V	550 V	600 V	650 V	700 V	750 V	1000 V
ESD Lab1	pass	pass	n/a	n/a	n/a	n/a	pass	fail
ESD Lab2	pass	pass	n/a	n/a	n/a	n/a	pass	fail
ESD Lab3/Tester1	pass	pass	pass	pass	fail	fail	fail	fail
ESD Lab3/Tester2	n/a	n/a	pass	pass	pass	pass	n/a	n/a
ESD Lab4	pass	pass	n/a	n/a	n/a	n/a	fail	fail

C.3.4 Conclusions on Stress Variation

The existing CDM (non-socketed) standards for many years have accepted the non-contact mode or air discharge mode of operation. This type of test method attempts to model the "real" CDM discharge event even though this type of discharge event produces peak currents that are variable and erratic. The air discharge ESD event is intrinsically more inconsistent because of fundamental environmental issues that influence the discharge current waveforms.

Tester-to-tester variation can also occur, even when following the same standard. The test standards allow for a wide range of peak currents at a given test voltage. This can result in significant variation from tester to tester depending on where within the allowed range a tester is calibrated. High-frequency differences that cannot be captured by low bandwidth (1 GHz) oscilloscopes, and even missed by 6 GHz oscilloscopes, can also cause miscorrelation between testers.

When the above sources of variation are combined with advanced design of high pin IC devices with extremely tight ball-to-ball pitches, the success rate for achieving highly repeatable test results is low. When the voltage steps are 50 volts or less, determining an actual CDM pass or fail voltage is very difficult. This is especially true when testing below 200 volts.

The goal of reproducing "real world" CDM discharges comes with a very high price; the primary casualty is achieving very tight repeatability and reproducibility of the ESD discharge event.

C.4 Emerging Test Methods

In the last few years, efforts have been made to develop test methods that can replicate the stress of non-socketed air discharge CDM while achieving the reproducibility of a relay-driven tester without giving up the high-frequency behavior of the air discharge. These methods are still non-socketed, thereby avoiding the unwanted parasitics associated with sockets. CC-TLP and LICCDM are two emerging relay-based test methods covered in this section. Also reviewed in this section is "Contact First CDM" – an air discharge method aimed at improving the repeatability of the air spark.

C.4.1 Capacitive Coupled Transmission Line Pulsing (CC-TLP)

Capacitive Coupled Transmission Line Pulsing (CC-TLP) [18-21] is an alternative method to generate CDM-like stress on devices and reproduce the electrical and physical failure signatures of CDM ESD events. The CC-TLP test system injects a rapid rising narrow, well-reproducible high-current pulse generated by a VF-TLP, into a single stress pin of a device after an electrical contact is established to this pin. This eliminates the high variation of the peak currents caused by an air discharge as it is occurring during the CDM stress procedure. The exponentially decaying charging current distributes over the full device under test similar to a rapid charging during FCDM testing and generates voltage drops internally across the device. Figure C15 shows the principle of the CC-TLP method. For a given stress, the pulse amplitude, the package or background capacitance Cb, and the stress rise time determine the injected stress current. Figure C16 depicts a set-up that allows testing at both the wafer and package levels.

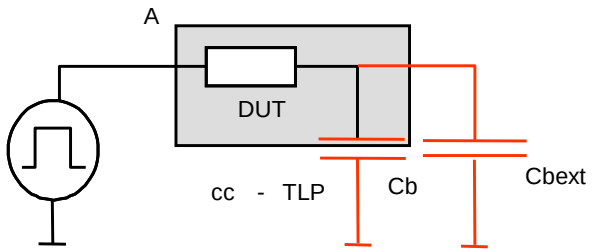

Figure C15: Principle of CC-TLP test. It is a one-pin stress. The stress current of the device under test depends on the amplitude and rise time of the VF-TLP pulse used for this test and on the capacitances.

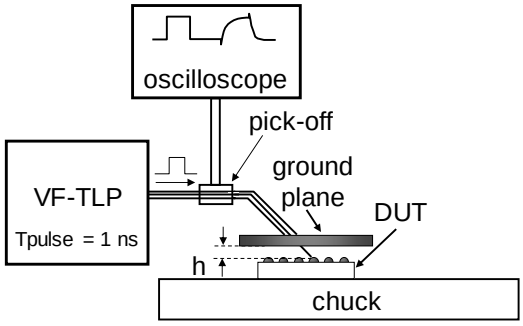

Figure C16: CC-TLP set-up that allows testing at both wafer and package levels.

The DUT is placed for example on the chuck of a wafer prober. The VF-TLP generates the pulse which passes the pick-off for the pulse voltage measurement and which is then injected into a semi-rigid transmission line TL (50 Ω). The outer conductor of the TL is connected to the ground plane, the inner one is connected to a probe needle which connects the DUT through a little hole in the ground plane. This hole is also used for the navigation of the probe needle by means of a microscope. The CC-TLP probe is mounted on an RF probe holder, which allows the correction of a tilt. The background capacitance Cb is formed between the ground plane and the DUT is influenced by the height h. The injected current is calculated from the incident pulse passing the voltage pick-off and the reflection from the DUT (TDR method). Typical stress pulses and an example of the correlation of physical failure signatures are shown in Figures C17 and C18.

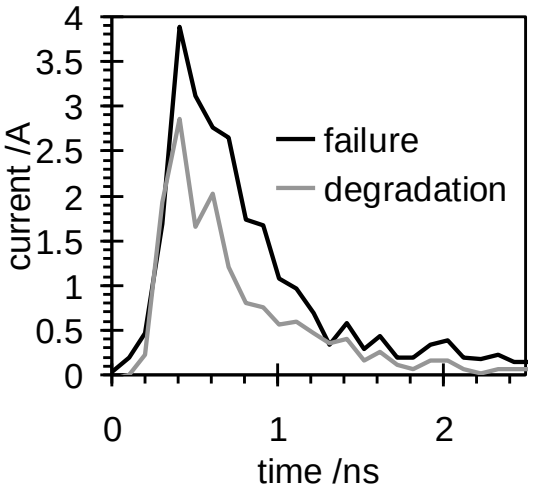

Figure C17: CC-TLP current waveforms for two pulses with increasing voltage levels. The lower one induced degradation, the higher one induced the failure of the DUT.

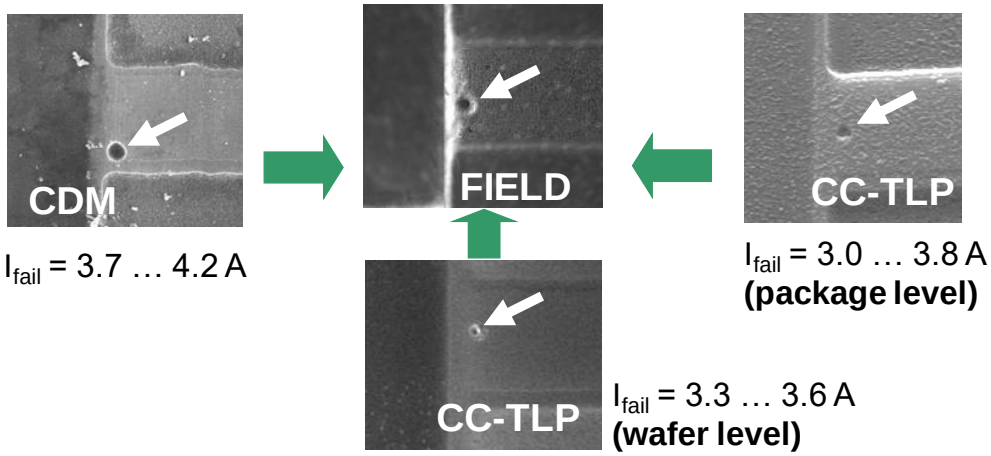

Figure C18: Comparison of physical failure signatures in the field, and from CDM and CC-TLP test. CC-TLP reproduced the gate oxide failure signature of failures from the field and after the CDM ESD test.

While this test method is currently already used to determine the robustness of products and for CDM failure debugging, this method is currently not applicable for qualification purposes. However, a standard practice document is in preparation by the ESDA.

C.4.2 Low Impedance Contact CDM (LICCDM)

Low Impedance Contact CDM (LICCDM) is another relay-based, contact-first discharge method for generating CDM-like stress [14-16]. Like the CC-TLP, LICCDM also injects a stress impulse into a single stress pin of a device after an electrical contact is established to this pin. However, the system impedances of the two systems differ. While CC-TLP has a system impedance of 50 Ω, LICCDM has been tuned to a 16.7 Ω impedance. An earlier version of LICCDM known as Contact CDM (CCDM) utilized a 50 Ω impedance [23]. Comparisons of failures induced by CCDM to those from field-induced CDM showed miscorrelation in some cases [24]. It was subsequently found that a better correlation to JS-002 could be achieved by reducing the system

impedance to more closely match the impedance of the air spark. A standard practice for LICCDM testing has been released by the ESDA [16].

A simplified hardware schematic of LICCDM is shown in Figure C19. The charge cable is charged and then discharged through a relay. A transmission line pulse is delivered through a rise time filter to the device under test (DUT) by way of a coaxial cable connected to the pogo pin. A second coaxial cable is connected in parallel to the first and delivers the transmitted pulse to an oscilloscope. A 50 Ω resistor is also connected between the pogo pin and ground. The effective impedance of the system as seen by the DUT is hence 50 Ω || 50 Ω || 50 Ω = 16.7 Ω. Displacement current stresses the DUT during the pulse rising edge. The RC termination at the far end of the charge cable results in a slow decay of the falling edge of the incident pulse, thereby preventing dual-polarity stress to the DUT. By subtracting the transmitted voltage waveform from the incident waveform and dividing by the system impedance, the current through the DUT can be determined. The pogo pin is in contact with the DUT both before and after the stress; hence, the only spark that occurs is within the relay.

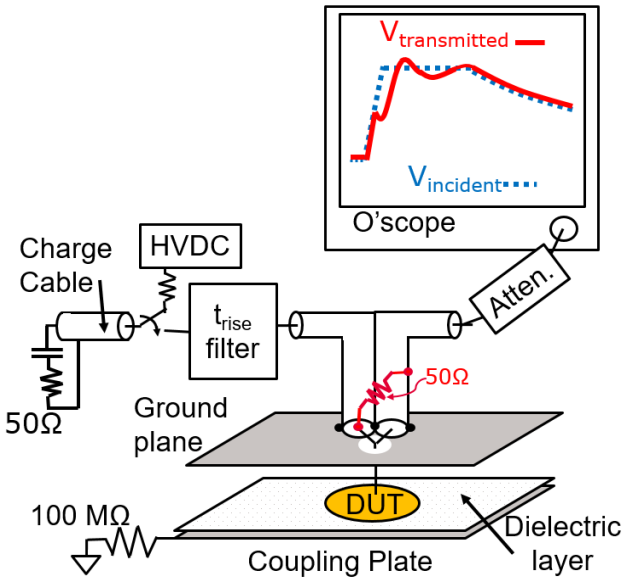

Figure C19: Simplified hardware schematic of Low Impedance Contact CDM (LICCDM).

Figures C20 and C21 show the discharge waveforms of LICCDM compared with those of JS-002 when stressing the small and large verification modules. The pulse width and damping factor of the waveform are dependent upon the effective discharge impedance. Because LICCDM has been tuned to approximate the impedance of JS-002, the pulse width and ringing of the two systems are nearly matched.

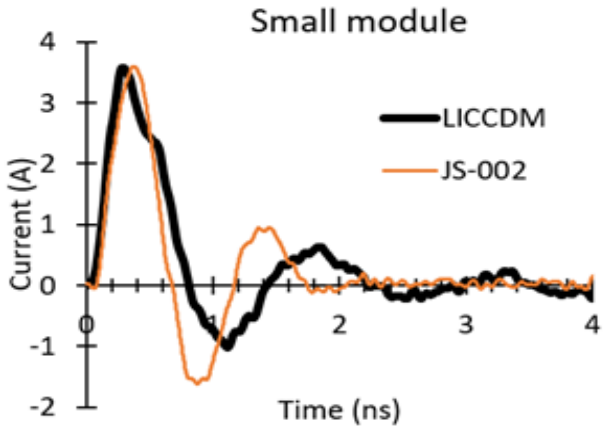

Figure C20: Comparison of the discharge waveforms from LICCDM and JS-002 when stressing the small verification module.

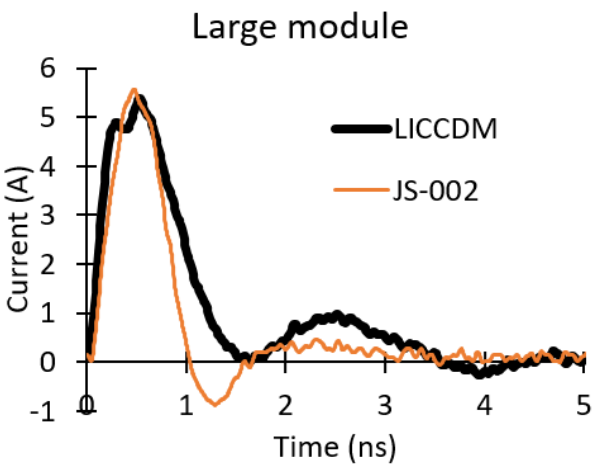

Figure C21: Comparison of the discharge waveforms from LICCDM and JS-002 when stressing the large verification module.

LICCDM and JS-002 were used to stress a test chip fabricated in a 32 nm CMOS process. A 37 mm x 37 mm LGA package was used. Thermally-induced voltage alteration (TIVA) analysis was conducted to determine the failure location on an input pin (Figure C22) and an output pin (Figure C23). As shown in Figure C22, the input termination resistor was damaged by stress from both the JS-002 and the LICCDM testers. The output driver transistor itself was damaged similarly by both test methods as shown in Figure C23. The failure currents were also matched between the two test methods on a variety of pins (not shown), as described in [15].

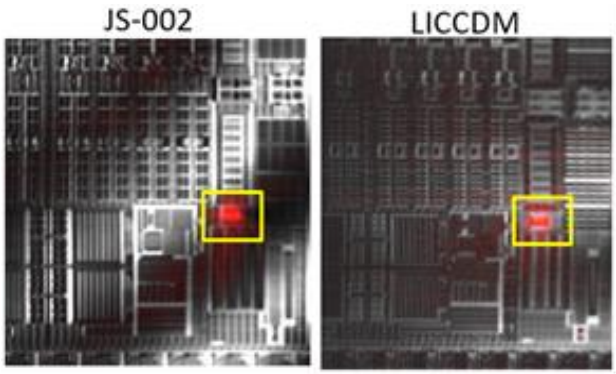

Figure C22: TIVA image of an input pin showing damage in the termination resistor after JS-002 and LICCDM stress.

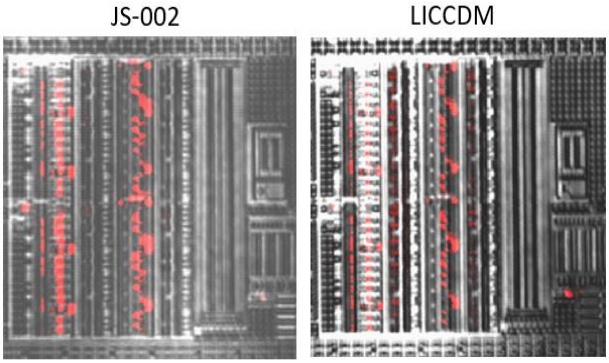

Figure C23: TIVA image showing the same damaged regions of an output driver after JS-002 and LICCDM stress.

C.4.3 Contact First CDM

The Contact First CDM method was developed under the premise that if the air discharge was moved away from a pogo pin contacting a DUT pin to a well-controlled environment the discharge would be more consistent. To accomplish this an entirely new ground plane and test head were developed, but one that would comply with the JS-002 field-induced CDM method.

The test head is shown in Figure C24. The ground plane includes a contact pin, which is physically, but not electrically connected to the ground plane. In operation, the ground plane is lowered until the contact pin touches the device under test. Since the contact pin is floating and has low capacitance, it does not ground the DUT. At this point, the ground plane stops moving, and the remainder of the test head continues its downward motion until a discharge pogo pin touches the top of the contact pin, which initiates the CDM arc. The discharge pogo pin is connected to the 1 Ω resistor and current measurement electronics. The top of the contact pin and the discharge pogo pin is enclosed in a small chamber, which is flooded with dry nitrogen. This method provides a spark geometry that is independent of DUT pin geometry, can be optimized for improved arc performance, and has a stable gas environment for the arc.

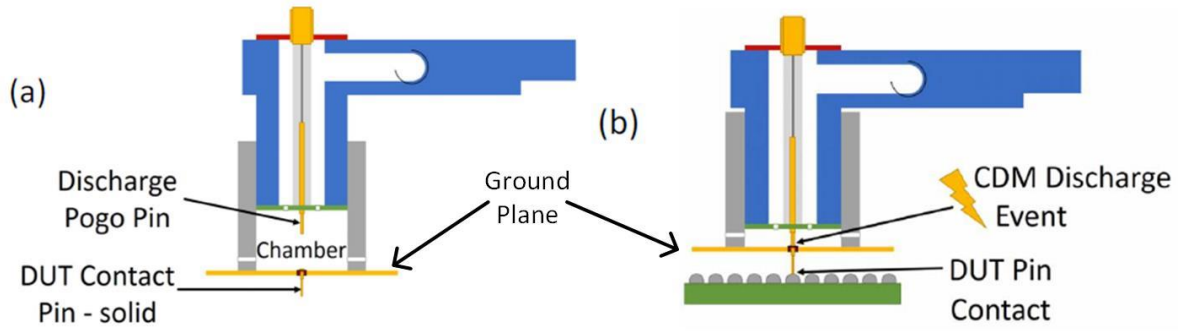

Figure C24: Contact First CDM test head, (a) with the head separated from DUT and (b) shown in the stress position

Measurement results with the First Contact CDM method were reported by Grund et.al. in 2018 [22]. The results were found to meet the requirements of JS-002 in terms of waveform parameters such as peak height, rise time, peak width, and undershoot, but unfortunately only marginally better in terms of variability from arc to arc. The real strength of the new system has turned out to be in its ability to reliably test packages with very fine pitch connections. With fine-pitch packages, it is not always clear with standard CDM measurements if the proper pin has been stressed, since the DUT pins are often smaller than the pogo pin tip. In standard CDM sharper tipped pogo pins cannot be used because they degrade arc properties. With Contact First CDM sharp contact pins can be used since the arc does not occur between the contact pin and the DUT pin.

C.5 Conclusions and Outlook: CDM Test Methods

This appendix briefly compared the different CDM ESD test methods and standards released by JEDEC/ESDA, IEC, AEC, and JEITA. The analysis has shown that the specific set-up parameters for each of these CDM standards vary. JEITA in particular has several significant differences from the other methods. Hence, when CDM ESD test results are discussed for a certain IC device, the standard for which the units were tested should always be considered.

Understanding the results of CDM testing and obtaining consistent test results between different standards and test systems is much more difficult than the HBM component-level test. The air discharge ESD event intrinsically produces peak currents that have a significant statistical variation. Many external environmental factors, like humidity, temperature, size and shape of the IC pin or ball, and the diameter of the ground pogo pin, strongly influence the air discharge current

waveform parameters. The test standards allow for a wide range of peak currents at a given voltage, which makes it possible for testers following the same standard to be tuned differently to satisfy the standard while resulting in different failure voltages. High-frequency components to the waveform can also be a significant source of tester-tester miscorrelation. Recent modifications to JS-002 encourage the use of 6 GHz oscilloscopes over 1 GHz, but even 6 GHz isn't sufficient to capture some of the influential high-frequency waveform components.

Current and future trends in technology will make CDM testing and design increasingly difficult. As this document has argued, testing and designing below 200 volts will become increasingly common for high-speed pins in advanced technology nodes. The variation in CDM discharge current becomes increasingly significant at these voltages. Advances in packaging technology with tighter bump pitches also adds uncertainty to test results given that the discharge spark can arc to any nearby bump. It is important that engineers take these points into consideration when testing these advanced technologies.

This appendix has also described three emerging, alternate methods for CDM testing: Contact First CDM, CC-TLP, and LICCDM. Contact First CDM improves reliable testing on tight-pitch packages while maintaining the air spark called for by JS-002. Both CC-TLP and LICCDM utilize relays to generate consistent stress waveforms, unlike the air discharge of JS-002. This enables reliable testing down to extremely low voltages with no repeatability issues, and it also enables ultra-fine step sizes to enable users to determine the true failure current of a design. To-date, both relay-based test methods have been shown to replicate the failures generated by air discharge testing. All three alternative methods generate the stress after the tester probe needle or pogo pin has made contact with the device. This contact-first approach to testing eliminates the difficulties that can arise when testing devices with small package pin dimensions.

While CC-TLP and LICCDM are promising future alternatives to CDM product testing, to-date these are only approved as characterization tools, not standardized test methods. In the interim, until such contact-based methods are in place, users of the field-induced CDM test method must understand the variability that may exist as testing at lower voltages is completed. Steps such as controlling the humidity, ensuring pogo pins, field plate surface, and devices are clean and free of any dirt are all critical to ensuring as repeatable a waveform as possible can be achieved. Additionally, it is imperative that the waveforms for *each* pin tested are logged so that peak currents can be checked/analyzed to ensure a clean waveform is produced. This is a good practice to have in place at any voltage level but becomes especially critical the closer testing goes to 125 volts.

It is imperative that future test standards allow for the use of contact-based CDM testers. It is likely a standard could be developed allowing for both air discharge and contact-based testers to be used alternatively, as is suggested in [15]. Further work is needed to enable such a standard, but this will become imperative as device, packaging, and signaling needs scale.

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Appendix D: Some Aspects of CDM Tester Circuit Modelling

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Summary – charged device model (CDM) non-socketed ESD testers as specified by ESD Association and JEDEC, and now in the merged document, ANSI/ESDA/JEDEC JS-002 produce waveforms in devices and calibration fixtures that can be understood through circuit models. At frequencies up to 1 GHz or so, waveforms are simple enough that the very simplest lumped series LRC model can be used to describe the behavior. Simple extensions of the model, to consider distributed transmission line effects for both the CDM test head and the device or fixture being tested, allow many reported high-frequency (e.g., 3 GHz) features to be explained and calculated. For the basic LRC model, peak currents are calculated and plotted in the L-C plane for typical values of spark resistance as well as L and C for CDM testing of semiconductor components. This highlights and explains some key differences between the ESDA and JEDEC CDM testers. Throughout the analysis, the Laplace transform viewpoint, and its related circuit modeling methodology is useful in transferring between the time and frequency domains. Such analysis also provides enlightening ways to look at methods proposed to duplicate the main features of CDM testing on silicon with wafer-level testing.

D.1 Introduction

The non-socketed CDM (ns-CDM) tester, according to [1, 2], can be circuit modeled as in Figure D1 and the immediate charge packet Q_{imm} can be calculated. In Figure D1, Cfrg is approximately the capacitance from the ground plane to the field plate. Cf is the capacitance of the device under test (DUT) to the field plate, and Cg is the capacitance of the top ground plane to the DUT. A CDM event happens when the discharge pin makes contact with DUT, thus closing the switch. The resulting Q_{imm} is

$$Q_{imm} = Vf\left[\frac{Cf}{Cg+Cf}\right]\left[Cg+\frac{Cf*Cfrg}{Cf+Cfrg}\right] = Q_1 + Q_2. \quad (1)$$

The effective capacitance C_{imm} thus satisfies the relation $Q_{imm}=C_{imm}*Vf$. This circuit model has shown close agreement with charge packet measurement done through the 50 Ω line shunting the 1 Ω disk resistor.

The equation above can be simplified without altering the sum if certain conditions hold. Usually, because of the thin dielectric, Cf >> Cg, which implies that Q1 << Q2. It also means the quotient Cf/(Cg + Cf) ≈ 1. We are left with the following equation

$$Q_{imm} \cong Vf \cdot (Cf \parallel Cfrg). \quad (2)$$

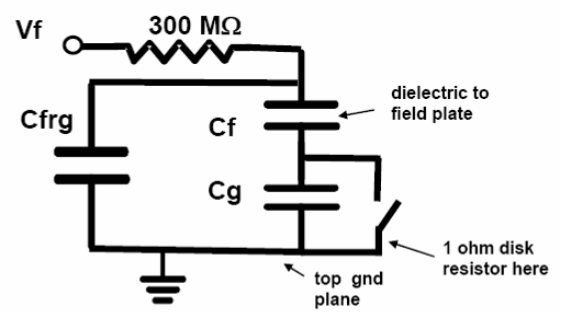

Figure D1: Circuit model for a field-induced ns-CDM tester. The switch closes when the discharge pin hits the DUT.

D.2 CDM Tester Model

The essential ESDA ANSI/ESD STM5.3.1 or JEDEC JESD22-C101 ns-CDM test circuit can be modeled as a single LRC series loop as long as certain parasitic elements are negligible. Let us first look at a more complete, yet simplified model for the CDM tester.

Various references on CDM testers [1, 3-4] have shown the utility of a 3-capacitor model of the device in the tester, and that a series-parallel combination of the three capacitors can be used to extract a single equivalent device capacitance C_{imm} for the resulting fast event. Then for field plate charge V_0, the immediate charge is $Q_{imm}=C_{imm}V_0$. The main resistive element in the circuit is the spark resistance Rs, which can vary considerably and is also time-dependent [5], but a typical deduced value for the CDM tester might be 25 Ω. That leaves the inductance, which appears mostly in the test head pogo pin probe [5] and the packaged device itself. In order to match the required waveform, the JEDEC JESD22-C101 CDM test head has extra electrical length, either because of an inductor or because the 1 Ω current detecting resistor, feeding the 50 Ω scope cable, is recessed behind a small cavity. Also, the packaged device can have up to 2-3 cm of trace length from the pin to the die for large packages. Signals on these traces may be impedance matched to 50 Ω all the way to the die, but in the ESD regime, diodes or other highly conductive protection devices turn on and reduce the terminating impedance to low numbers of ohms. Thus, we have nearly-shorted transmission lines on either side of the spark resistance and switch. Before returning to the transmission line model, let us picture that 1 Ω terminated transmission lines as equivalent T-networks as shown in Figure D2, in order to focus on the principal RLC poles and zeros of the network.

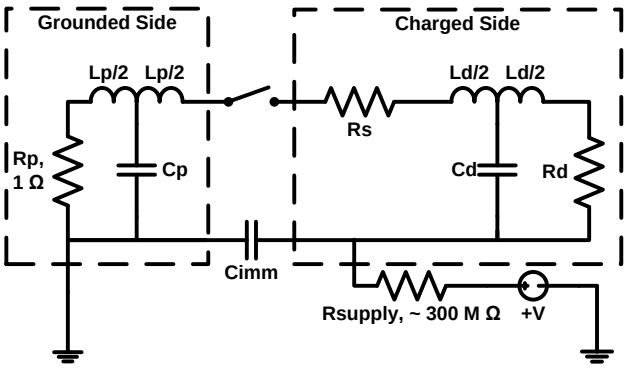

Figure D2: CDM tester equivalent circuit, with (charged) device circuit on the right and (grounded) test head and probe on the left. Rp = 1 Ω is the test head current detector and Rd ≈ 1 Ω is the on-chip protection.

In Figure D2, the charged (hot) side, with the device model, is on the right and the grounded side, with the pogo pin and test head model, is on the left. The related approximate values of Cp and Lp for package options, calibration fixtures, and test head options are shown in Table D-I. Our principal concern is the outer loop of Figure D2, which is reducible to the well-known series LRC. It has two poles and a zero in the admittance function, and resistance dominated by the spark. This admittance function is

$$Y(s) = \frac{Cs}{LCs^2 + RCs + 1}, \quad (3)$$

where the L, R, and C values are clear from the totals in the outer loop.

The usual observation, particularly on oscilloscopes of 1 GHz bandwidth or less, is of a single sharp spike and limited or nonexistent ringing, indicating an overdamped or slightly underdamped solution. This is the outer loop current through the 1 Ω detector. But note that the effective capacitances of the transmission lines form inner loops, all with the same resistor Rs, on each side of the circuit. This introduces several options for high-frequency poles, as the device or probe capacitors bypass some of the outer loop inductance. These new poles are manifested at a higher frequency than the outer loop because of the lower inductance, and the series capacitance with C_{imm}. Thus, we have the high-frequency ripple and double peaks that have been reported when multi-GHz measurement systems are used [6], and not seen for lower-frequency measurements where the outer loop alone is visible. Figure D3 is a scope trace from Ref. 6, showing these features. Note that all of these complex resonant frequencies depend on the interaction between the test head and the device under test; if the device trace length is changed, all the poles will move. Thus, it is no surprise that peak currents (and much else) vary with package location [7], even aside from the C_{imm} variations due to field plate and ground plate movement. As the calibration fixtures each have few parasitics of note, and a stable C_{imm}, they should work as intended for checking out the CDM events.

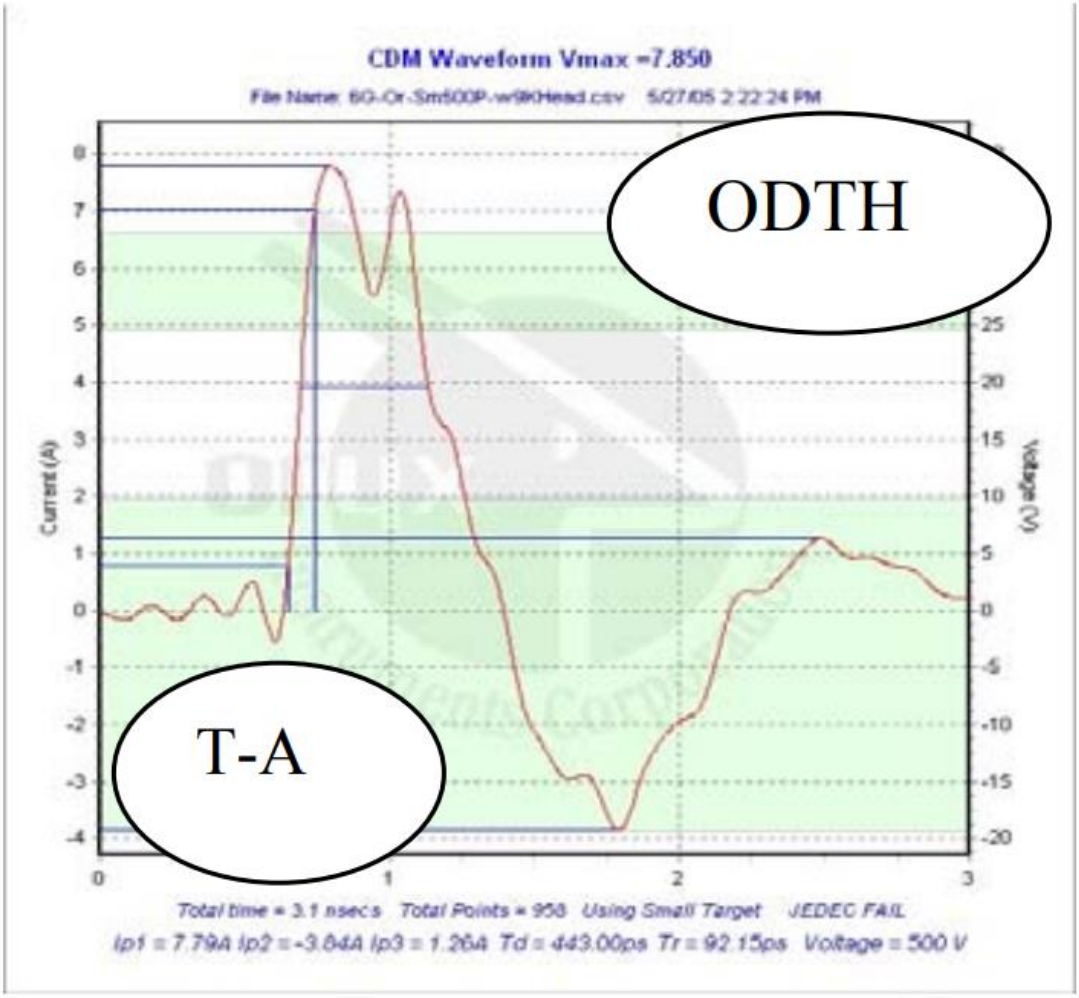

Figure D3: JEDEC CDM pulse measured with a high-speed oscilloscope, sensitive to higher natural frequencies and thus showing double peak. From [6]. Figure D2 or Figure D4 circuit models can explain.

The entries in Table D-I for Figure D2 also make it clear why there were occasional problems with devices tested on the JEDEC JESD22-C101 CDM test head of note—the longer electrical length in JEDEC creates higher parasitic inductance and capacitance than the ESDA ANSI/ESD STM5.3.1 test head. This lowers the outer loop frequencies a little, but those are already heavily modulated by C_{imm}. This test head affects the inner loop frequencies because of its higher Lp and Cp. Note also that a loop through Cd can have a low frequency for a long enough package trace, which should even have an effect on the use of the ESDA ANSI/ESD STM5.3.1 test head.

The admittance zeros of Figure D2 should be noted along with the poles. The two zeros are easily seen as the parallel LC tank circuits on the right and left, corresponding to quarter-wave shorts in the associated transmission lines. Stopping the current with a zero in the admittance function may not seem to be a bad thing, but both the 1 Ω detector resistor on the left and the protection device on the right, is in the midst of those tanks. Thus, each will feel some current at its own LC tank resonant frequency, even though the overall current is low due to cancellation in the tank. This means that there could be a detector current that is not felt at the device and vice versa. But note that the package resonance of a long 50 Ω trace in the dielectric, 2 cm as described in Table D-I, would be below 3 GHz (Table D-I is for well below quarter-wave frequency; 2 cm when dielectric

$\sqrt{\varepsilon_r}$=1.5 is quarter-wave for 2.5 GHz). This is below the 3 GHz frequency reported in [6] to be the JEDEC JESD22-C101 test head resonance, so it appears that between 2.5-3 GHz we have a vigorous half-wave series L-C resonator, which could easily cause destruction. Now, let's return to a more accurate transmission line model.

Table D-I: Approximate values of circuit elements as pictured in Figure D2.

	Lp, nH	**Cp, pF**	**Ld, nH**	**Cd, pF**
ESDA test head	3.6 nH	0.22	x	x
JEDEC* test head	10-12	~0.5-0.6	x	x
Calibration fixture	x	x	small	small
Device, short trace (2mm)	x	x	0.5	0.2
Device, long trace (2 cm)	x	x	5	2

*JEDEC test head with 1 Ω detector resistor is recessed behind a short high-Z cavity; effective electrical length of the pogo pin probe and the cavity is 2.5 cm in air, or 3 GHz resonance [6].

The CDM test system is well modeled by a loop as pictured in Figure D4, with two transmission lines in series, terminated by low-Z in each case. One line is for the device (impedance Z_{d0}, usually 50 Ω, with propagation constant and electrical length given by k_d), and one is for the test head and probe (Z_{p0}, k_p), with a presumed average test head impedance, upwards of 100-200 Ω depending on the test head. As a further refinement, the probe and test head section could be modeled as two or more line segments if needed.

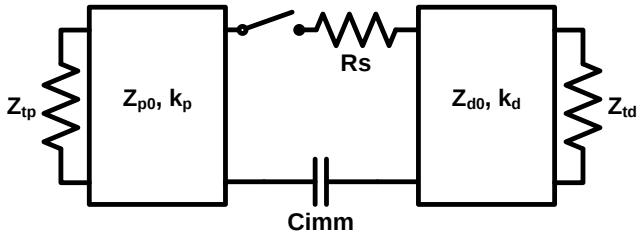

Figure D4: Generalized transmission line model for the CDM test system; test head and probe side on left and (charged) device side on right.

Terminations Z_{td} and Z_{tp} are generalized forms of Rd and Rp from Figure D2. The general expression for Z_{din} is

$$Z_{din}(s) = Z_{d0}\left[\frac{Z_{td} + Z_{d0}\tanh(k_d s)}{Z_{d0} + Z_{td}\tanh(k_d s)}\right], \quad (4)$$

and there is a corresponding expression for $Z_{pin}(s)$. The admittance function for the network becomes

$$Y(s) = \frac{1}{R_s + Z_{din}(s) + Z_{pin}(s) + \dfrac{1}{C_{imm}s}}. \quad (5)$$

Clearly, the zeros of this function (aside from the usual s=0 for series LRC) occur when one of the lines goes through a singularity and we have tan(π/2), i.e., quarter-wave resonance on a line. The poles occur when the expression in the denominator goes to zero, and the lowest frequency poles are our outer loop of interest. Because s is a complex frequency, σ+jω, it is important to note that these lowest frequency poles could be real and negative (overdamped), as the negative s-dependent terms balance Rs. The events in standard CDM testers will have major real components in their lowest frequency poles as a result of the short duration and subdued ringing of the pulse.

The higher-frequency poles of Y(s) will occur beyond the first quarter-wave resonance, when one Z_{in} goes negative and (largely) imaginary, and eventually joins with the ever-smaller C_{imm} term to balance the other Z_{in}. This will happen at the lowest frequency when both Z_{in} functions approach quarter-wave near the same frequency; when one moves beyond π/2, goes negative jtanθ and soon zeros out the denominator. Reducing the electrical length of one line pushes out this pole (or conjugate pair of poles, most likely) to a higher frequency, but not above half-wavelength for the longer line. This higher frequency pole resonance can be destructive because the termination current (i.e., across our protection device) is raised by the high (equal and opposite) voltages appearing across both lines in series L-C resonance. It should be much more destructive than anything felt by the termination at a zero of Y(s). The lesson for CDM testers is that the electrical length (k_p) of the test head and probe pushes the half-wave resonance to a lower frequency due to the combination of the test head and device. But since the package trace effect is part of the intrinsic factory CDM event, the high-frequency stress appears to be appropriate when those package conditions exist.

Solving Eq. 5 for all relevant complex roots and inverting to the time domain would be very revealing but will have to be the subject of a future study. We shall now return to Eq. 3, our basic low-frequency LCR loop, for insight into our CDM testers and measurements.

D.3 Waveform Analysis

The admittance function of Eq. 3 is solved to give two poles, expressed in pole-zero form in the Laplace domain as

$$Y(s) = \frac{s}{L(s+a)(s+b)}. \quad (6)$$

In general, the poles at -a and -b are complex frequencies. These poles are given by

$$a,b = \frac{R}{2L}\left(1 \pm \sqrt{1 - \frac{4L}{R^2 C}}\right), \quad (7)$$

where the solution is overdamped if $R>2\sqrt{(L/C)}$. The sign convention is chosen so that the time domain solution will be a sum of complex exponentials e^{-at} and e^{-bt} according to Laplace transform analysis [8]. Another expression for the poles is

$$a,b = \omega\left[-D \pm \sqrt{D^2 - 1}\right] \quad , \quad (7a)$$

where damping factor $D=RC/(2\sqrt{LC})$ and $\omega=1/\sqrt{LC}$.

The CDM discharge current in the Laplace domain is I(s) = V(s)*Y(s), where V(s) is a step function for the switch arc, expressing the discharge of C_{imm} to zero. This could be an infinitely abrupt step function V_0/s, but we would like to build in the finite rise time of the spark itself, irrespective of any LCR-related rise times. This is believed to be 50-200 picoseconds (10-90% rise time), which we will capture as an additional pole so that the step has a gradual exponential approach, $V_0(1-e^{-ct})$, c positive and real. For a 10-90% rise time τ we must take c=2.2/ τ. Our source becomes $V(s) = V_0/(s(s+c))$ (neglecting normalization factors) so we now have

$$I(s) = \frac{V_0}{L(s+a)(s+b)(s+c)}. \qquad (8)$$

This 3-pole model should give the discharge current waveform for the basic LCR loop; this can be carried out by using methods of finding inverse Laplace transforms as in [8]. But at present, we're guessing and curve fitting to obtain resistance and spark rise time. In the discussion of peak current that follows, for simplicity we will revert to the two-pole model that is based only on single values of L, C, and R. The peak current I_{PEAK} for a series LCR network with initial condition V_0 across capacitor C, and perfect switch closure (i.e. 2-pole solution), depends on whether the solution is overdamped, D>1, or underdamped, D<1, D again the damping factor. The general expression is

$$I_{peak} = \frac{2V_0}{R} D \exp\left(-\frac{D}{\sqrt{\pm(1-D^2)}} \tan(h)^{-1}\left(\frac{\sqrt{\pm(1-D^2)}}{D}\right)\right) \qquad (9)$$

where the $\tan^{-1}$ and + sign refers to underdamped. Figure D5 shows how I_{PEAK} approaches V_0/R as D increases. In Figure D6, values of I_{PEAK} are plotted in the plane of L and C for 500 volts and a value of R, 25 Ω, that is commonly found for equivalent spark resistance [9]. The overdamped case is shown in red in the region at the lower right.

For an ESDA ANSI/ESD STM5.3.1 or JEDEC JESD22-C101 CDM test reduced to this equivalent LCR, the capacitance is C_{imm} and the inductance depends on both the component or fixture being tested and the test head. Figure D6 points out zones of general agreement with the JEDEC JESD22-C101 and ESDA ANSI/ESD STM5.3.1 tests for cases where the object being tested does not add much extra inductance to the test head, e.g., a component's Vss or Vcc plane being zapped. Note that while the JEDEC JESD22-C101 test head lowers the frequency of higher-frequency modes, as pointed out earlier, the peak current due to the principal LCR loop is actually a little lower for JEDEC JESD22-C101 due to the higher inductance. Thus, the ESDA ANSI/ESD STM5.3.1 failure voltage can be lower simply due to the higher I_{PEAK}, if high-frequency resonance effects are unimportant for the device under test.

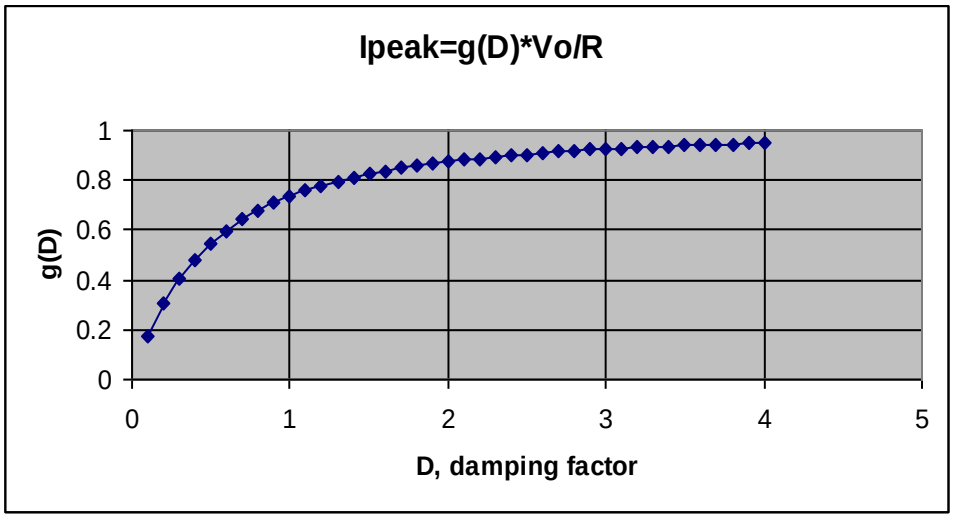

Figure D5: Plot of Eq. 9 showing how I_{PEAK} approaches V_0/R as a function of D.

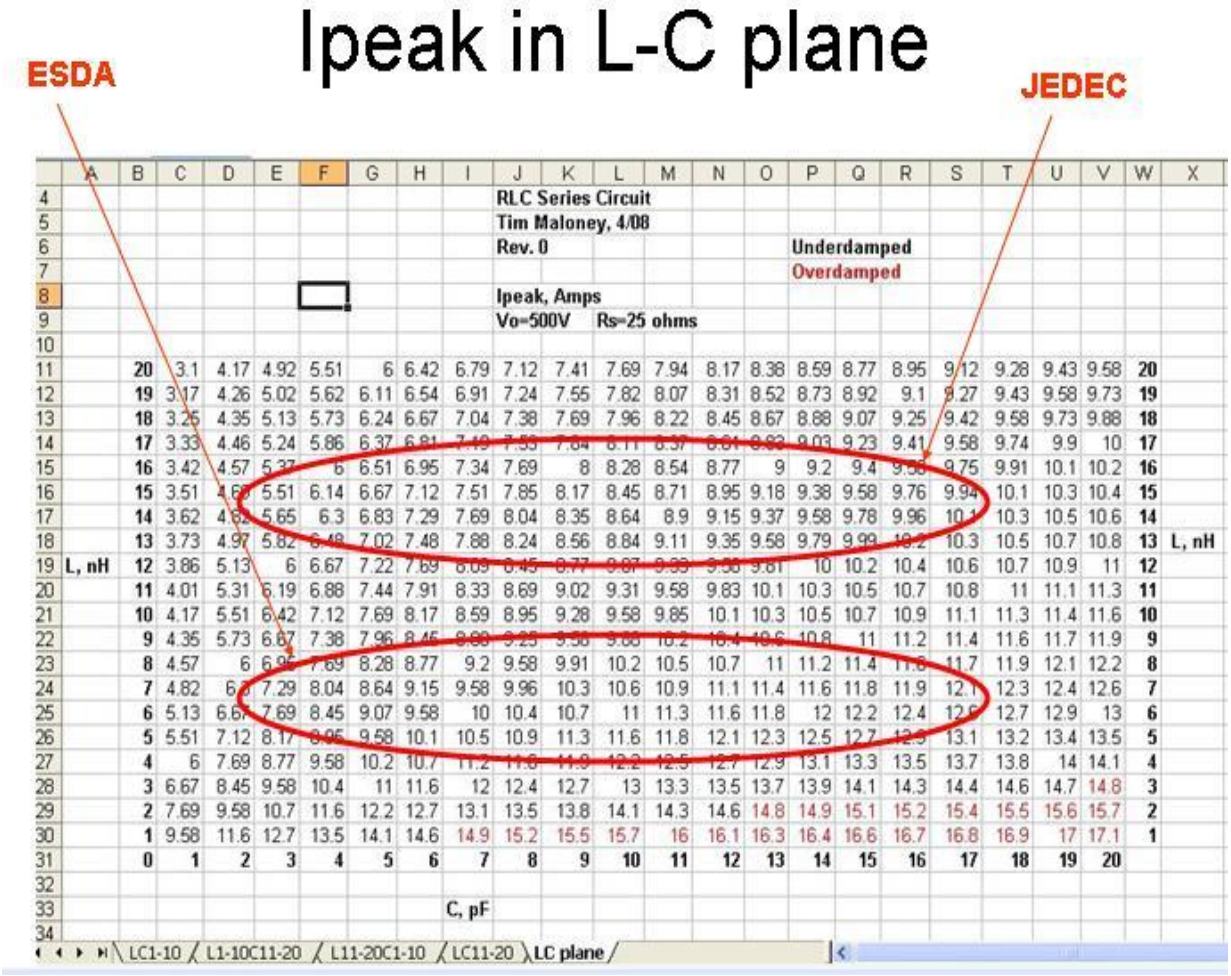

Figure D6: I_{PEAK} for simple series LCR discharge circuit, 500V, and typical values of L and C. R=25 Ω. Typical regions for the ESDA ANSI/ESD STM5.3.1 and JEDEC JESD22-C101 CDM testers are shown.

Figure D7 shows an example, from an Intel developmental test product, of a zap to Vss measured on a JEDEC JESD22-C101 CDM tester with a 1 GHz oscilloscope. The latter is low enough frequency to filter out any high-frequency effects that would give double peaks and such. The waveform looks to be underdamped, and the charge measurement from the integrated current gives a capacitance of 18-20 pF. The peak current is around 14 amperes.

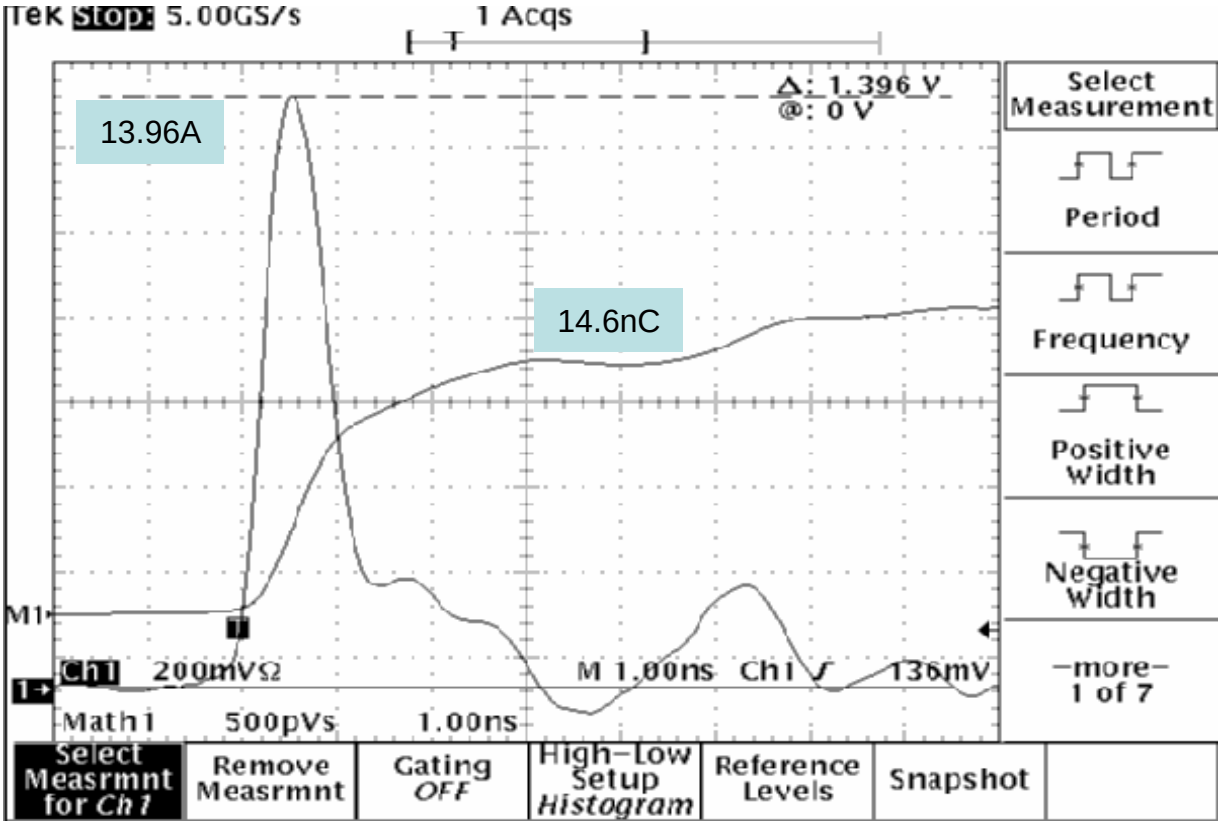

Figure D7: JEDEC JESD22-C101 CDM waveform at +800V on Vss plane of a developmental product; peak current and total charge is shown.

A best fit to these measurements then gives an equivalent spark resistance R of 38 Ω, as shown in Figure D8, another plot of I_{PEAK} in the L-C plane. This value of R is not unreasonable, particularly for a 2-pole model where we expect it to include the effects of intrinsic spark rise time, our would-be third pole in the analysis. As shown in Figure D8, the capacitance and peak current come out about as expected for the JEDEC JESD22-C101 CDM tester.

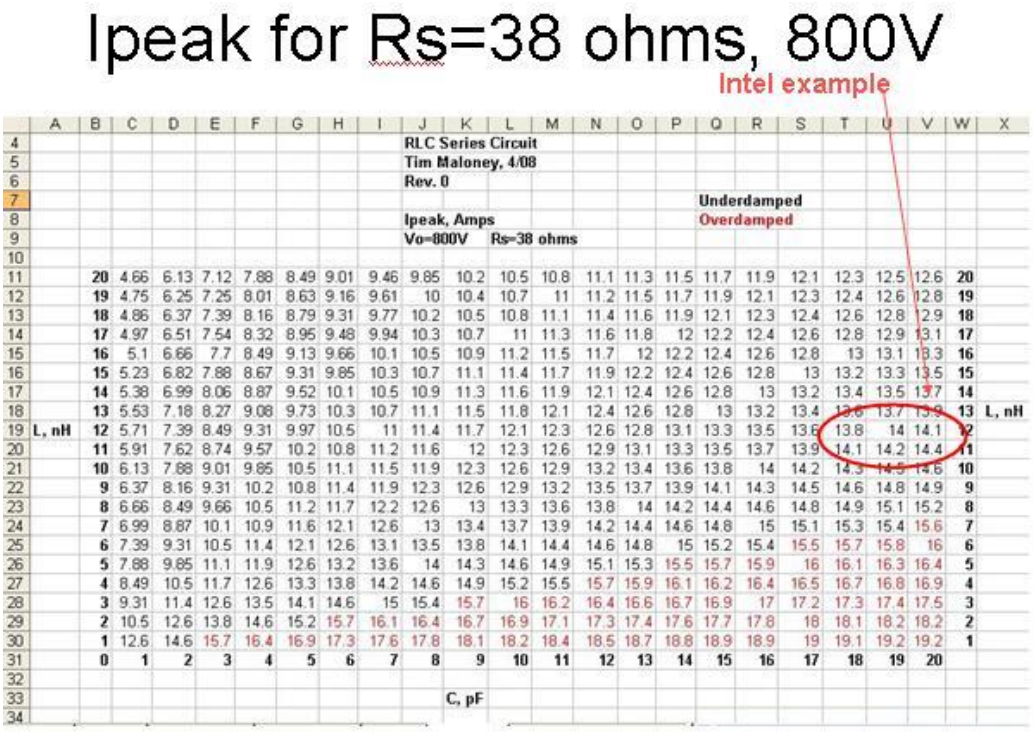

Figure D8: I_{PEAK} in L-C plane for series LCR discharge circuit, 800 V, R=38 Ω. The location of Figure D7 example is shown, consistent with the JEDEC JESD22-C101 CDM tester.

D.4 Conclusions

From the above analysis, it is clear that much can be understood about CDM testing of components from these relatively simple modeling considerations. A circuit model can focus on the primary lower-frequency effects and then be expanded to include higher-frequency effects if desired, using transmission line segments or appropriate approximations. The circuit models lead directly to solutions in the Laplace domain, which can convert to time-domain solutions through the inverse Laplace transform [8], or else be solved numerically using CAD tools like SPICE.

This kind of circuit modeling and related Laplace transform analysis can also be applied to two methods that have been used to achieve CDM-like pulsing on the wafer level and as a substitute for ESDA ANSI/ESD STM5.3.1 or JEDEC JESD22-C101 CDM testing. One is the present author's wafer CDM (WCDM) technique [10], using a charged plate and probe above a grounded wafer and discharging at the pad. Please see Ref. 10 for much overlap with this appendix's analysis of ns-CDM, and further analysis in the time and frequency domain of the WCDM method. The focus of WCDM is on simple overdamped solutions of the LCR circuit in order to achieve a CDM-like fast rise time and high peak current. The other method for CDM-like pulsing is capacitively-coupled transmission line pulsing (CC-TLP), which has been published for some time [11]. This method uses a step generator and 50 Ω line to force a pulse through a probe already connecting to a pad on the wafer. The ground return is through a grounded disk above the wafer (or grounded component) that forms the capacitive coupling. Spark resistance and rise time now reside in the TLP relay, although exclusive of any dispersion effects in the 50 Ω line. Also, spark resistance is remote from the 50 Ω line source and can be eliminated with attenuators or z-matching. It is

interesting to write an admittance function Y(s) for the CC-TLP case. Neglecting intrinsic or dispersed step function rise time, this would be

$$Y(s) = \frac{Cs}{LCs^2 + 50Cs + 1}, \quad (10)$$

very much like Eq. 3, except for the 50 Ω line impedance replacing the switch resistance. The inductance L is the very small inductance of the probe extending below the CC-TLP ground plate (there is some distributed probe capacitance too [12,13], but the probe impedance Z=√(L/Cp) is fairly high), C is the ground plate cap. The waveform will be a double exponential (two real roots, overdamped) as long as 50 > √(L/C); very likely given a small probe inductance and a ground plate of reasonable size. The WCDM scheme [10] in its simplest form also has an admittance function resembling Eq. 10, where L can be a low probe inductance, and an adjustable resistance is added to the arc resistance to replace the 50 Ω in (10) or R in (3).

In the time since this appendix was originally completed (2010 timeframe), major work by the author and a co-author has been published, work that advances these concepts further [14]. In addition, over the past few years, improvements in Excel Solver (a plug-in optimization program for Microsoft Excel) have made far more accessible a least-squares fit for the elements of an RLC model of the CDM waveform. Use of the generalized reduced gradient optimization usually is the best choice for convergence of RLC values to a least-squares fit to the measured waveform.

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Appendix E: CDM Tester Limitations in Representing Real-World Events

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E.1 Physics of Real-World CDM

E.1.1 What is the physics of CDM? How does CDM occur in the factory?

CDM discharge of a device occurs if the potential difference between the charged device and an external metal object exceeds the breakdown voltage of the small air gap between them. The typical breakdown voltage of air is defined by the well-known Paschen's curve. However real-world events depend on a variety of conditions including the following:

- The discharge contact shape
- Capacitance, potential, and gap distance variability due to DUT motion
- Inductance variability due to package geometry and the geometry of the conductive discharge surface

If the charged voltage is roughly 2000 volts or greater, a corona-like discharge can occur, which decreases the potential difference of the DUT before the CDM air discharge occurs. On the other hand, CDM testing requires good repeatability since it is a qualification tool in which capacitance, inductance, contact speed, environmental conditions, etc. are intended to be as constant as possible in order to meet the standard [3, 4, 13].

A basic CDM discharge is considered to be a rapid charge transfer between two objects as illustrated in Figure E1.

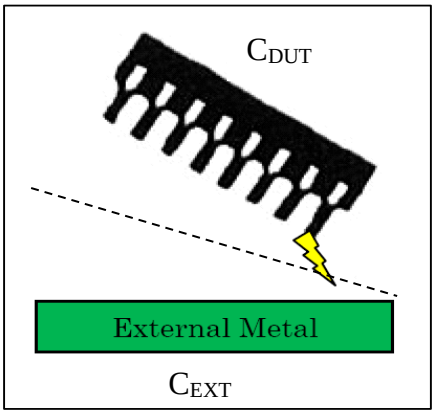

Figure E1: CDM Discharge between 2 objects. A single capacitance is partitioned into two series segments C_{DUT} and C_{EXT} as shown each with respect to a bisecting surface.

Figure E1 shows the discharge path between a DIP IC that has capacitance C_{DUT} and an external conductive surface with capacitance C_{EXT} (both with respect to a "reasonably drawn", but not rigorously defined surface between them). Depending upon the environment, inductance and resistance may exist in the discharge path and will contribute to the voltage and current waveform discharge characteristics. When the dipole collapses and the potential difference is balanced between C_{DUT} and C_{EXT}, the discharge is complete.

E.1.2 Real-World CDM Description of Device Potential / Charging / Discharge Mechanism

E-Field charging and tribocharging are the main methods of device charging:

E-Field charging: Changes in the electric field around a device change the potential of the device without changing the net charge on the device. The change in potential makes the device vulnerable to a rapid current pulse or CDM event when it contacts a conductor at a different potential. A charged person's sleeve nearing the device is an example of this type of charging.

Tribo-charging: Static charge is generated if a device slides on another surface. The generated charge depends on the materials of each surface, friction coefficient, and the slide speed of the device. Several common examples exist in automated IC handling in manufacturing:

- **Devices sliding inside an IC shipping tube** is an example of this charging
- **Picking up from tape or a tray**: When a device is picked up from a device carrier, such as carrier tape or tray, a charge is generated. This is a kind of tribocharging.
- **Peeling off a sheet/tape and reel**. If a protection sheet is removed from the surface of electronic devices such as a display device or CCD, the device is charged. This is also a kind of tribocharging.

When a charged metal tool contacts a device, it causes CDM-like stress. This may be somewhat different from field induction or tribocharging; however, it can be considered as a type of CDM stress, although the pulse width may be somewhat wider. This looks like a system-level stress depending on the size of the metal tool. Charged board events (CBE) may also be included in this category.

Advances in IC device and packaging technology have led to an increased incidence of CDM events in a modern manufacturing environment. In the early stage, IC packages were through-hole mounted and typically handled by machine or human hands. This has shifted to surface-mount packages, with more automated machines being used. In modern mass production factories, human handling is nearly nonexistent.

E.1.3 Early Stage Real-World CDM Events Examples

Figure E2 illustrates an example where an IC package was charged by the friction between a marking roller and the package surface [5]. Another example was found in the IC tester where a DIP package slides in the tube followed by loading into the test socket.

Figure E3 is another example that illustrates 1) a corona discharge, followed by 2) a higher resistance air discharge, and then 3) a low resistance air spark discharge for an initial device charging voltage over 1000 volts [6]. The corona discharge reduces the device voltage before the

air gap discharge is triggered. When the gap distance becomes smaller, a non-oscillation (higher spark resistance) discharge is detected, followed by an oscillation discharge (lower spark resistance) that is detected just before the contact. Spark resistance of the last discharge is less than 50 Ω, though 2nd spark resistance is typically over 100 Ω. If the contact speed is high enough, the second discharge is not typically detected. If the contact speed is too slow, more than two air discharges may occur until complete contact is made.

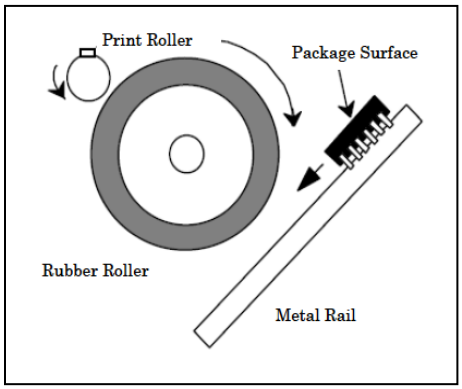

Figure E2: Early stage package Charging example

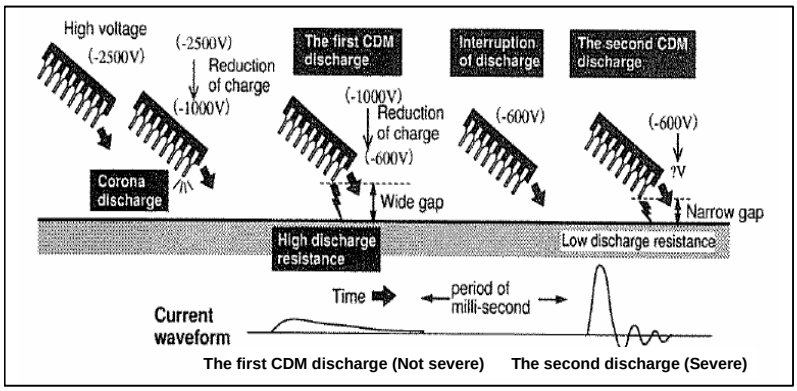

Figure E3: Example of multiple CDM discharge from High voltage devices

E.1.4 Real-World CDM Event Examples

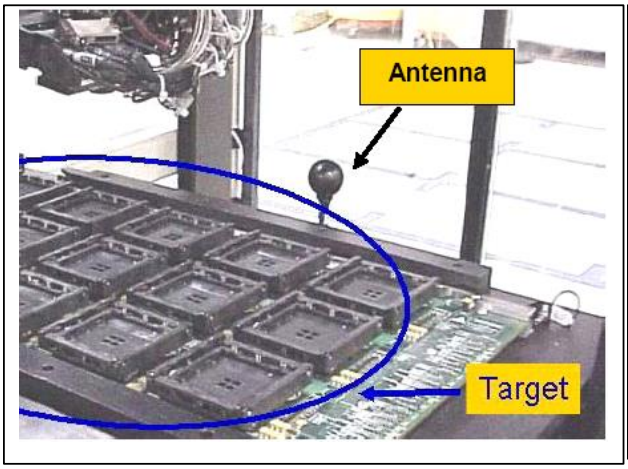

Figure E4: Advanced stage CDM example

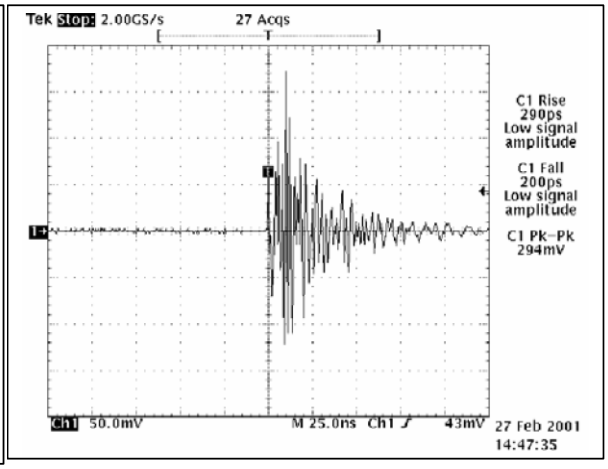

Figure E5: Scope waveform received by antenna shown in Figure E4

Since surface-mount packaging is more common, pick-and-place automatic machines are used everywhere in automated production lines. In this environment, more chance of field-induced charging is found. Figure E4 shows an example where the device is picked from a tray then loaded in the socket of a burn-in board. A CDM event happens if a sufficient potential difference exists just before the contact between a device pin and an IC socket. The near field antenna in Figure E4 receives the electromagnetic field generated by this event and can be monitored by an oscilloscope

as shown in Figure E5. It was reported that peak to peak voltage of this waveform is proportional to the CDM event charge if the distance between the antenna and CDM discharge source is constant [7].

E.1.5 Capacitance Change Effect on Real-World CDM Stress

Typical CDM discharges occur when one pin of a charged integrated circuit approaches an external conductive surface. It is an air discharge that occurs just before the contact. Examples include:

Contact between IC and test socket
Contact between IC and PC board
Contact between IC and IC tray that has non-uniform resistivity

In the real world, handling is automated and capacitance between the handled device and a target object, such as a PC board where the device will be loaded, changes. The rate of capacitance change (increase) is highest just before the contact, in other words, just before the CDM event. Figure E6 is an example of the capacitance measurement that varies with the distance between a DIP device and the ground plate [8]. Figure E6 shows that the capacitance of the device decreases down to roughly one tenth of the starting value as the distance increases to a few mm above the ground plate.

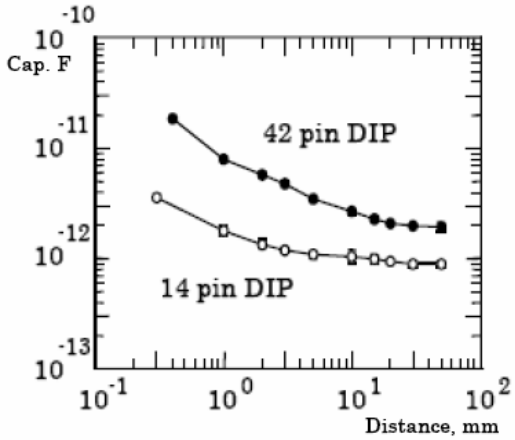

Figure E6: Device Capacitance vs. distance

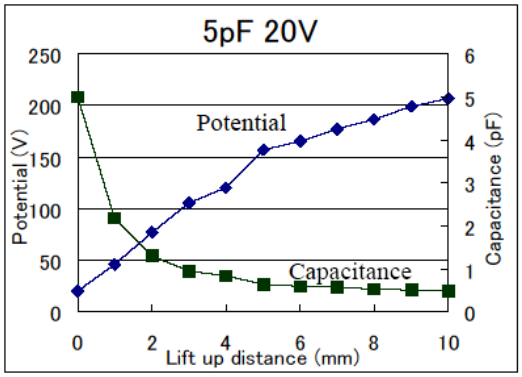

Figure E7: Device Capacitance vs. distance

This implies that if the amount of charge on the device is constant, the device potential decreases down to one tenth after approaching the ground plate from a distance of 10 mm. This can also be illustrated by plotting discharge current versus the distance between the source of capacitance (i.e., the device) and the ground plate [9]. Figure E7 shows this relationship between distance and potential/capacitance. This graph shows that the potential of the capacitance module increased from about 20 volts to over 200 volts by lifting up the device. Capacitance, on the other hand, decreased from over 5 pF to less than 0.5 pF. Since the peak current of the CDM event is proportional to the voltage across the gap, the peak current decreases if the potential difference decreases due to the reducing gap distance. This reduces the CDM stress to the device. These phenomena are very common in real-world CDM events.

E.1.6 Real-World CDM Event Failure Types:

Figures E8 [10] and E9 represent examples of component CDM failures. Figure E8 illustrates a gate oxide failure, the most common CDM failure mode. The white spot at the NMOS gate represents the emission site of failure in this picture. Figure E9 is another CDM failure example reported by Y. Fukuda, where a diode junction showed failure because diode diffusion spacing distance was not enough to limit breakdown.

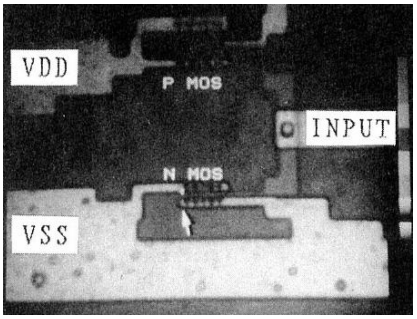

Figure E8: GOX Failure Example [10]

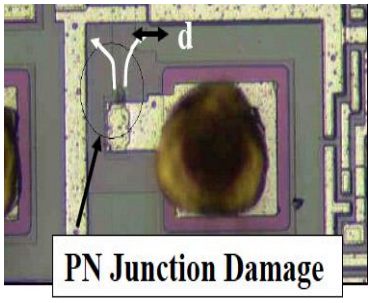

Figure E9: PN Junction Failure

E.2 Consideration and Analysis of Real-World CDM

E.2.1 Circuit Model Representation of Real-World CDM

Figure E1 can be described by the circuit schematic as shown in Figure E10. S represents the contact where the CDM discharge happens. R_{DUT} and L_{DUT} are series resistance and inductance in the DUT. L_{EXT} and R_{EXT} are inductance and resistance formed by the external conductive surface. Since all elements are serially connected, inductance and resistance values can be added together to create the simplified circuit model of Figure E11. R in Figure E11 includes R_{DUT}, R_{EXT}, and the spark resistance of S. Sufficient voltage differential between V_{DUT} and V_{EXT} causes the discharge.

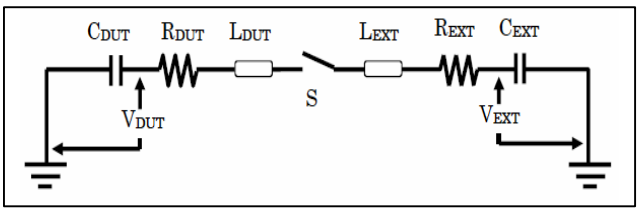

Figure E10: Real-World CDM, Circuit Model

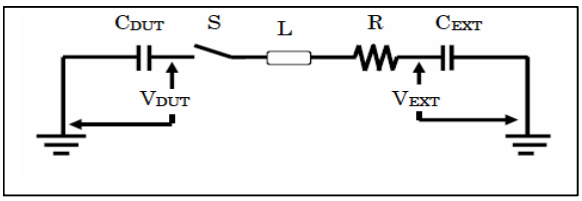

Figure E11: Simplified circuit of Figure E10

E.2.2 Real-World CDM Stress Dependence on Package Style/ Size and Grounding

Because there are wide variations in factors affecting the real-world CDM, it is difficult to compare every case. Typical cases are discussed here.

The CDM current is defined by the following equations [6] if the result of the portion of the equation inside of the square root is positive. V in this equation is the difference between V_{DUT} and V_{EXT} in Figures E10 and E11.

$$I(t) = \frac{V}{\omega L} e^{-\alpha t} \sin(\omega t) \quad , \text{ where } \alpha = R/2L \text{ and } \quad \omega = 2\pi f = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \qquad \text{Equations E.1}$$

On the other hand, the CDM Tester capacitance circuit model was reported as Figure E12 [7, 12]. If this model is applied to the real world, Cfrg (plate to plate capacitance through the air) is usually much smaller than Cf (device to field plate through a thin dielectric). The series combination of Cfrg and Cf resembles C_{DUT} in Figures E10 & E11 while Cg resembles C_{EXT}; however, they combine in parallel in the tester, not in series. As a result, the capacitance C in equations E.1 can be defined by the serial capacitance of C_{DUT} and C_{EXT} in Figures E10 & E11. For the tester, as described in Appendix D, Cg adds to the series combination of Cf and Cfrg. In both cases, a single equivalent capacitance results.

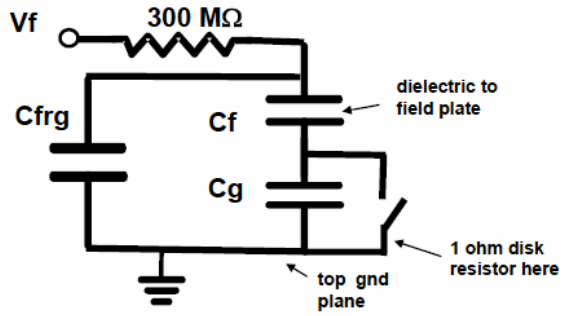

Figure E12: Capacitance model of F-CDM Tester

In Equations E.1 each parameter has the following meaning in the real world:

V: Voltage difference across the gap just before the discharge (V_{DUT} - V_{EXT})
L: Inductance of the discharging path. This includes inductance inside the package such as bonding wire and lead length and any external wiring such as the PC board pattern and the socket contact lead.
R: Series resistance of the discharge path. Arc resistance dominates real-world CDM events and varies from about 10 Ω to above 100 Ω depending on the environment. Depending on the L and C values, the condition of the above equation ($R<2\sqrt{(L/C)}$) is not satisfied which gives a non-oscillating pulse (Figure E3 left).
C: Serial capacitance of C_{DUT} and C_{EXT} as described above.

Under the above assumptions, a comparison between packages can be done as follows.

Between small package and large package (Small BGA and Large BGA):

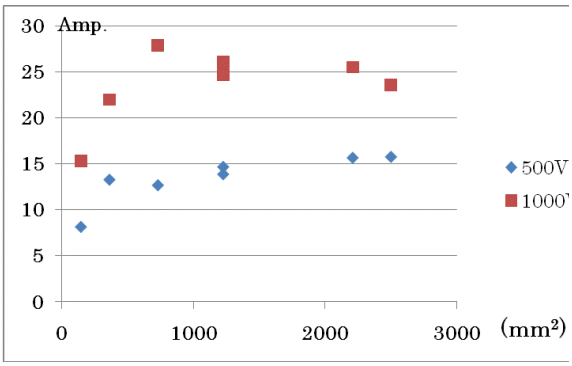

Figure E13: Peak current comparison between different BGA Package sizes

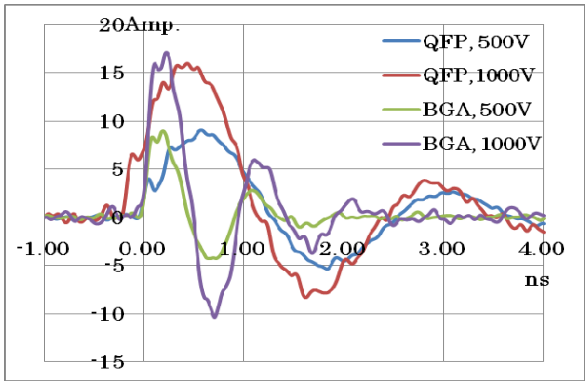

Figure E14: Peak current comparison between small BGA Package and large QFP both include same die

It is typical that a smaller package has a smaller C_{DUT} than a larger package. But it is the series combination of C_{EXT} and C_{DUT} that largely drives the peak current. C_{EXT} may be small, in the case of a small metal tool, and will drive the peak current accordingly. It is true in the tester world, too, where the equivalent C is defined by the standard [11]. Figure E13 shows a real-world peak current comparison of 6 different BGA packages ranging in size from 12 mm x 12 mm to 50 mm x 50 mm simulating the discharge to a small metal tool as shown in Figure E20. Because the tool C_{EXT} is typically much smaller than the device C_{DUT} in the real world (especially if C_{DUT} is high), current from a large package that has higher capacitance is almost constant. As shown in Figure E13, the peak current increases only in the small capacitance region with package size less than 1000 mm^2.

Between package types (BGA and QFP):

Figure E14 compares the waveforms from small BGA and large QFP packages containing the same die design. The package sizes of the BGA and QFP were 12x12 and 28x28 (mm^2 in both cases), respectively. The peak currents are equivalent, but the pulse width from the BGA is less than half of that from the QFP package. Note that these waveforms were measured using a 140 mm x 140 mm top ground plate. It should be noted that the same current amplitude for the same die will not always be observed for different packages. A change in measurement conditions may result in a different current amplitude comparison. For example, if a lower bandwidth scope is used; the actual peak current for the BGA package may be lower than for a QFP package due to the pulse width difference.

Through-hole type package and surface mount package:

Through-hole type packages are loaded on a PC board in such a way that IC leads connect through mounting holes on the PC board. In this method, the distance between the PC board and the IC body is greater than for a surface mount package where the IC lead tip contacts the PC board metal. This means that the C_{DUT} of the through-hole package during a CDM event is smaller than the C_{DUT} of the surface mount package. As a consequence, the voltage during the CDM discharge from a through-hole package is higher than for a surface mount package, assuming that both packages hold the same amount of charge. However, discharging inductance L from a through-hole package is typically higher than that of a surface-mount package. Bond wire length

differences between these packages should also be considered for the current comparison. To compare the current difference from these package types, both V and C as well as L, in equation E.1, should be considered.

The thickness of the package (Surface mount packages):
In general, thinner packages have more C_{DUT} than thicker packages if the footprint is the same. If it is assumed that both packages begin at the same potential as they start moving far from the PC board, the eventual peak current from the thinner package is smaller than that from a thicker package because V is lower for the thinner package when the CDM event occurs.

Weight and package surface:
When sliding was the major consideration in device handling, weight and surface flatness were important parameters of charging. As surface mount packages requiring pick and place have become more commonplace, these parameters are not as important. Surface material and flatness may cause a difference in charging. Mirror smooth surface packages have more chance of charging than coarse surface packages [10].

E.3 Differences Between Real-World CDM and Tester World CDM

Table E-I: Comparison between Real-World and Tester World CDM

Parameters	Real World	Tester World
Device capacitance (C_{DUT})	Depends on the package and environment. Typically smaller than tester world	Stable, but depends on the package, tester, and test standard
Discharging capacitance (C_{EXT})	Depends on the target object. Typically smaller than the tester world.	Stable, but depends on the package, tester, and test standard
Capacitance between field plate and top ground (Cfrg)	Negligible in most cases	Determines equivalent C_{DUT}; can exceed the real world
Charging voltage	Environment dependent.	Repeatable and definable
Discharging resistance	Depends on the package, environment, and contact material	Nearly stable, environment controllable
Discharging Inductance	Depends on the package and the target object	Constant, but depends on the tester, test standard, and device package
Peak Current	Depends on the package and the target object Lower than tester world in most case, especially on large package	Largely repeatable but dependent on package and Standards
Current rise time	From less than 100 ps to a few ns	Stable, but accuracy limited by oscilloscope bandwidth

Note: Table E-I compares CDM parameters between Real World and Tester World CDM.

How is the real world represented by testers?

- The tester simulates the worst case of real-world events. However, the rise time of the real-world ESD event can be faster than observed in a CDM tester where the CDM test head has an upper bandwidth limitation of about 7 GHz.
- The tester provides a repeatable CDM evaluation.
- The tester stress level depends on the standard that the tester complies with, such as legacy JEDEC, legacy ESDA, legacy AEC, ANSI/ESDA/JEDEC JS-002, updated AEC, or JEITA.
- If the current level of the real-world CDM for the device is known, the same current can be applied to the device by the CDM tester. In the past, this comparison was difficult to make, due to inadequate oscilloscope bandwidths during tester verification and waveform monitoring. The JEDEC and AEC test methods specified oscilloscopes with 1 GHz bandwidth, while JEITA specifies a 2 GHz bandwidth. ANSI/ESD STM5.3.1-1999 and ESD DS5.3.1-2007 had an option to use a 3 GHz oscilloscope, although many organizations continued to use the 1 GHz option. ANSI/ESDA/JEDEC JS-002, with its verification requirement of using a 6 GHz or greater oscilloscope improves the validity of real-world to tester CDM comparison considerably.
- Voltage or Current: Using only damage voltage does not well define the CDM ESD sensitivity since C (Capacitance) or I (current) is unknown.

E.4 CDM Waveform Comparison Between Real World and Tester

All CDM ESD Standards require that the commercial CDM tester conforms to the current waveform specification [1-4,13]. Peak current discharged from small and large verification (capacitance) modules should fall within the ranges of Table E-II. Capacitance values of the small and large module in JEITA may be different (about 15% less) from what is listed in Table E-II since the JEITA standard recommends a nominal 4.0 dielectric constant insulator sheet above the ground plate (although the coin modules are very close to the JEDEC standard). These standards also specify current pulse rise time and width. Since the verification modules do not include any inductance, only tester inductance is included in the discharge path.

Table E-II: Peak Current Comparison Table Between CDM Standards at 500 V

	Legacy JEDEC[1]	Legacy ESDA[2]	Legacy AEC[3]	JEITA [4]	ANSI/ESDA/JEDEC JS-002 [13]
Small Module	5.75A ±15% 6.8 pF±5%	7.5A ±20% 4 pF±5%	4.5A ±20% 4 pF ±5%	4.0A ±10% 4 pF ±5%	7.2A ±15% 6.8 pF ±5%
Large Module	11.5A ±15% 55 pF±5%	18A ±20% 30 pF±5%	14A ±20% 30 pF ±5%	5.5A ±10% 30 pF ±5%	12.1A ±15% 55 pF ±5%
Scope BW Min.	1 GHz	3.5 GHz	1 GHz	2 GHz	6 GHz

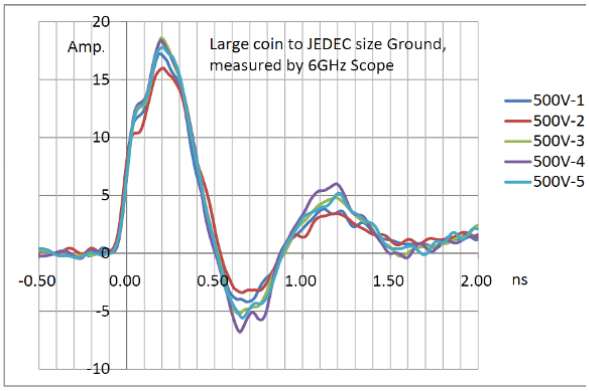

Figure E15: Large Coin to JEDEC size ground

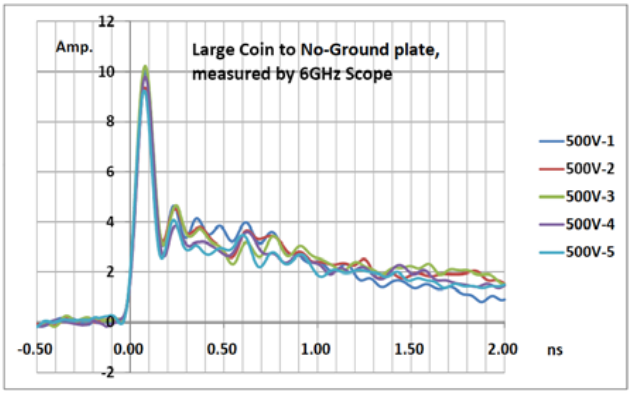

Figure E16: Large Coin to no top ground plane

Figure E15 shows current waveform measurements from a large JEDEC verification module to a JEDEC size ground (63.5 mm x 63.5 mm) at a charge voltage of 500 volts. Figure E16 shows the current waveform from the same large coin module without a top ground plane. The current waveform is very different between these figures. The current for the JEDEC size ground plate is 50 to 80% higher than the current for a module without a top ground plane. While the waveform of the module with a ground plate is a damped oscillation, the waveform of the module without a ground plane shows a short single pulse. Figure E16 is closer to the real-world CDM event waveform than Figure E15 since the top ground plane in a real-world CDM event is not usually as large as for CDM in the tester world.

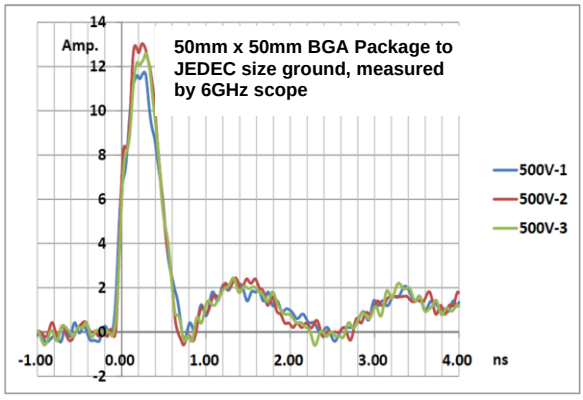

Figure E17: Large BGA Package to JEDEC size ground

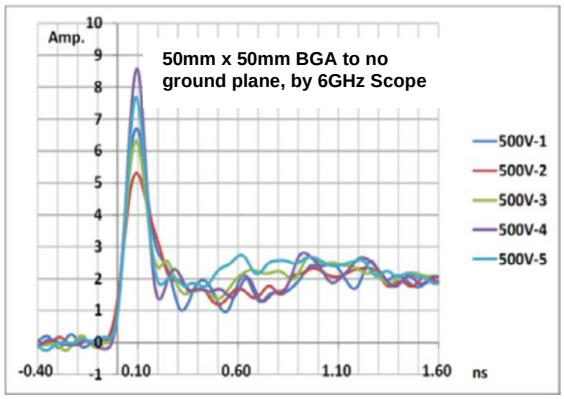

Figure E18: Large BGA Package to no top ground plane

Figure E17 shows the current waveform discharged from a 50 mm x 50 mm BGA package device to a JEDEC size ground plate with a charge voltage of 500 volts. If the ground plate is removed, the waveform in Figure E18 results. The relationship between Figures E17 and E18 is very similar to the relationship between Figures E15 and E16. If the ground plate is removed, the discharge current does not oscillate, and the pulse width is very short compared to the waveform with a ground plate. The capacitance of this BGA package when placed on a 0.4mm thickness JEDEC insulator was about 100 pF.

Figure E19 illustrates the discharge path inductance effect on peak discharge current for a small coin, a large coin, a small BGA, and a large BGA at 500 volts. The top ground was a JEDEC size

plane. Contact rod lengths of 2 mm, 5 mm, and 10 mm were used. Figure E19 indicates that the peak current decreased to roughly 1/2 with a contact rod length increase from 2 mm to 10 mm for the large capacitance devices. Peak current from smaller capacitance devices is not affected as strongly as higher capacitance devices.

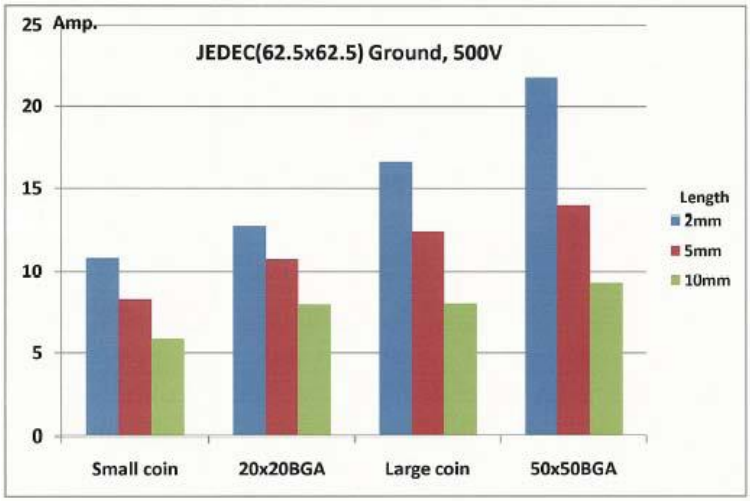

Figure E19: Contact Rod Length Effect to Peak Current of Devices

In real-world CDM environments, the discharge "ground" does not resemble a large ground plane as in the worst-case tester environment. This means that the peak current of the real-world CDM event is not as high as the tester world. The current probe used in the above experiment is shown in Figure E20.

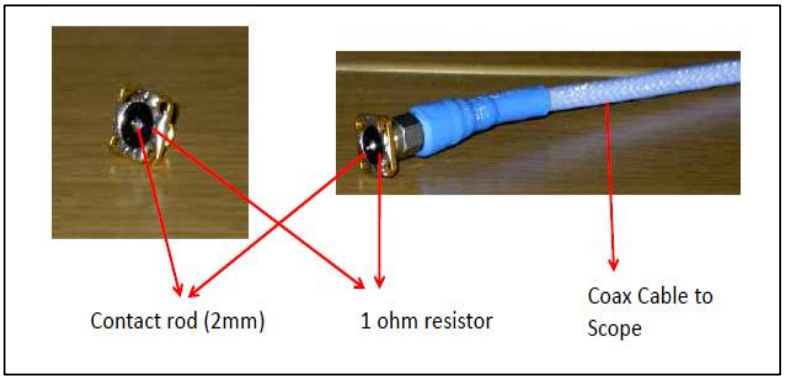

Figure E20: Current probe used in the above experiment: Different size top ground plane was mounted by the 4 holes on the connector corners

E.5 Conclusions

Real-world CDM events were evaluated and compared to the tester world, with the following conclusions:

- Real-World CDM events are not as repeatable as a tester world CDM discharge.
- Discharge current from higher capacitance devices increases if the top ground size in the tester world is larger.
- In real-world CDM events, a very low inductance discharge to a large upper ground is extremely rare. Since the serial inductance of a real-world CDM event is typically higher than in the tester world, the peak current is not as high as in the tester world. If a 10mm wire (roughly 13 nH) exists in the discharge path, the peak current from a higher capacitance device will be 50% less than if a 2mm wire discharge were used. (Figure E20)
- Charged Board Events (CBE) are not included in this discussion of real-world CDM events. CBE should be handled separately and is discussed in Appendix G.

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Appendix F: CDM – Does it Correlate to Other ESD Stresses?

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This appendix addresses possible relationships between CDM [1] and other ESD-like phenomena. Therefore, it explores the correlation between CDM and the other component-level tests, HBM [2], and MM [3]. It has been shown that HBM and MM are generally very well correlated [4]. In the spirit of conciseness, we will therefore only refer to HBM when comparing to CDM. Further, the correlation to other tests or phenomena, such as system-level ESD [5], Charged Board events [6], and EOS are discussed. The analysis will start from a theoretical point of view and will be illustrated by examples and case studies. Finally, the conclusion will summarize the consequences of the recommendations.

F.1 Theoretical Analysis

ESD failures arise due to two distinct mechanisms: high local power dissipation and breakdown due to high electrical fields. The first mechanism typically leads to damage due to the melting/dislocation of material. The second mechanism typically leads to damage in dielectrics or as a trigger for the first mechanism. Obviously, the nature of the damage will depend on the available energy and the location of the dissipation. A study of possible correlations between ESD-like phenomena therefore requires that the electrical parameters determining the conditions for the failure mode need to be compared.

Thermal failures depend on the energy content of the discharge, the power in the discharge, and the duration of the discharge. The latter two are related via the so-called (non-linear) Wunsch-Bell relation [7]. Dielectric failures are due to high electrical fields, i.e. high voltage differences in the network. These arise from two reasons. First, there is a large peak current. Second, the dv/dt of the discharge event induces high peak voltages on ESD protection circuits prior to turn on [8].

Relevant parameters describing the different phenomena, such as energy content, pulse width, rise time, and peak currents differ significantly. Some of these parameters are defined mainly by the method, e.g. in the case of HBM while others depend significantly on the DUT, e.g. in the case of CDM. Table F-I summarizes the fixed parameters and calculated quantities for a 1000-volt event for all phenomena. Where applicable the values are given for a realistic range of DUT parameters. Clearly, there are large differences between the models. The consequences will be discussed in the next sections.

There are significant differences in how the discharge currents are distributed within the DUT, due to the different nature of the test mechanisms. Many of the phenomena can be described by a 2-pin experiment. The discharge current enters the DUT at a given pin and exits at another pin. In a normally designed ESD protection network, these tests evaluate the robustness of predefined paths

specifically designed with ESD current capability in mind. For CDM however, one of the pins is the capacitive coupling of the DUT to the outside world/tester. The energy of the pulse is stored in the chip/package capacitance itself, as the reference voltage of the chip is different than ground. A discharge to ground of any one pin causes a multitude of parallel paths of current within an IC. The CDM path of discharge is from the internal circuit out, and internal circuitry derives a voltage from the power and ground domain capacitance developing a voltage from the pin discharge. Due to different delay times, this may generate voltage differences over devices.

Table F-I: Comparison of some typical network values and electrical quantities for a 1 kV stress.

	C (pF)	R (Ω)	τ (ns)	Q (nC)	E (µJ)	P (kW)	Ip (A)
HBM	100	1500	150	100	50	0.330	0.67
CDM	1-100	15-100	1-2	1-100	0.5-50	0.25-25	1-25
System	150	330	50	150	75	1.5	3.0

F.1.1 HBM vs. CDM

It is well known that the time constant associated with CDM is much smaller than that of HBM. The difference is so large that the two types of stress may address two different regions in the Wunsch-Bell diagram. As is clear in Table F-I, the peak current for CDM can be much higher than for HBM. Thus, even assuming all power is dissipated in a single location, it is clear there will not be a strong relation in general between CDM and HBM. Second, the high dv/dt of the CDM discharge event induces higher peak voltages on ESD protection circuits prior to turn on [8]. Therefore, the internal gate oxides of cross-domain logic can be exposed to high voltages before protection turn on, and thus more prone to damage.

It is generally observed that most of the samples that fail a CDM test show gate oxide failures, whereas samples failing an HBM test show melt failures. Thus, a correlation between HBM and CDM is not expected. The next section will show this by FA examples and a correlation calculation.

F.1.2 System-level ESD vs. CDM

The history and model of system-level ESD (IEC) is described in Chapter 6 of Industry Council White Paper 1 [4] and the IEC 61000-4-2 Standard [5]. It is well-known that the unique feature of the system-level ESD waveform is that it is composed of two distinct portions, the first a very fast (~ 1 ns) high peak current portion and the second a medium speed (10-100 ns) medium current portion. The initial portion resembles the first peak of a CDM-like waveform where a large potential difference tends to be generated. The second portion is similar to HBM or the first peak of MM stress that has more energy. It should be noted that this holds for a calibration waveform of the ESD gun into a defined short. Depending on the system board circuit and system pin of discharge, the energy seen by the board will be different in different parts of the board as the paths taken can vary, and the failure mode is not predictable.

It has been shown that system-level pulses can produce failures that look like CDM damage as well as failures that look like HBM damage. This has been shown on products [9] and test structures [10], as shown in Figure F1. Although the physical mechanisms of the damage are the same as those that occur during product qualification, it is in general not possible to relate product and component-level results. The failure mode of the IC in the system, as well as the failure voltage, depends on the printed circuit board (PCB) design and the way to assemble the system.

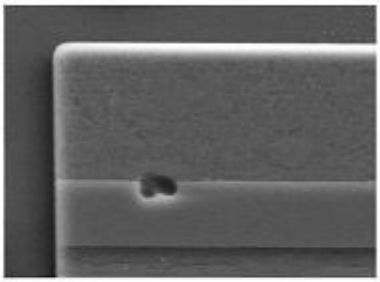
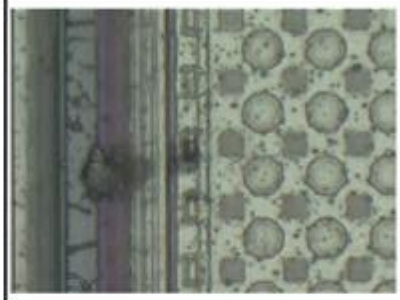
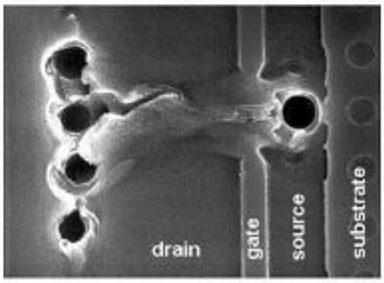
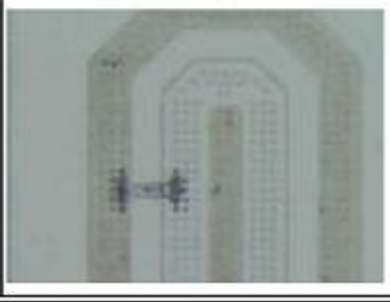
Failure mechanism	failure device level	failure system level
Breakdown of an isolation (left: gate oxide, right: LOCOS)		
Thermal melting of silicon		

Figure F1: Different failure modes from component level and system-level stress [9]

To address the application of system-level ESD stress to the pins of a component the human metal model (HMM) standard practice [11] was developed. In addition, as described in White Paper 1, it is known that EMI generated by system-level ESD test may cause latch-up like failures that cannot be caused by the device-level ESD test since the device level tests are always done in an unpowered state for the IC. Typically, these do not lead to physical damage, but if they do, they will be of the thermal category.

F.1.3 CDM vs. EOS

The term EOS stands for "electrical overstress". For electronic components, overstress is divided into two general energy spectra: ESD, which applies to overstress signals less than 1 µs in duration, and EOS which covers overstresses beyond 1 µs in duration [7]. ESD manufacturing controls (in machines, equipment, and personnel) will prevent EOS events. However, when electronics come in contact with materials that are unprotected or otherwise have a voltage on them, discharge into the circuitry can occur which can cause an EOS event. Examples of EOS events include unpowered devices inserted into "hot" test sockets with voltages applied to them, or improper power supply sequencing. The latch-up test [12] applied to integrated circuits qualifies as an EOS event as it is performed at voltages above that of normal operation for durations up to several milliseconds. However, shorter overstress events of higher voltage, or longer overstress events, can cause EOS damage.

The total energy of CDM events is much below that of the transition between an ESD and EOS event. The failure modes seen in CDM demonstrate this, as the damage is normally much less extensive in area and material impact than that of an EOS event. The clear distinction between the failures ascribed to electrical overstress (EOS) and the failures ascribed to electro-static discharge (ESD) have been demonstrated [13, 14]. The mechanisms associated with the ESD current flows through the chip have been demonstrated [15, 16]. The mechanisms associated with the EOS

failure have also been demonstrated [17], where EOS failures occur mostly in the bond wires (burnt, fused), on the die surface (glass and top metal) in the form of deformed glass on burnt/fused metallization. This is characterized mainly by discoloration at the site of the failure. This is in direct contrast to the lack of discoloration characteristic of ESD failures in general and CDM failures in particular. For EOS, low magnification (up to 1000X) is enough to see the failures while for ESD, very high magnification is required. The ESD failed device must be deprocessed down to the silicon level. Since the ESD and EOS simulations require different pulse width and rise times, there is no correlation expected.

F.1.4 CDM vs. Charged Board Event

CDM failures result from the discharge of stored charge in the device capacitance. The device capacitance, which is charged as a result of the CDM event depends on chip size and package size and is typically a few tens of pF at most. On the other hand, in CBE, the relevant capacitance depends not only on the device and package but also on common system board capacitance and other IC capacitances connected to it [6]. So, CBE total capacitance around the IC is much higher than the single DUT CDM case. Because this large amount of charge discharges through some IC in a CBE discharge, discharge current may be several tens of times more than the device level CDM and are more likely to produce thermal failures than CDM [18]. More details are given in Appendix G.

There are some CDM-like discharge scenarios where real-world discharge events can have a higher peak current and faster rise time than found in a CDM tester [19-22]. In this discharge scenario, for example, a charged on-board connector with signal wires discharges into the IC. In this case, the source capacitance can be less than 1 pF and the total series inductance of the discharge path less than 0.5 nH. These short and fast ESD events can be understood as ultra-fast CBE with a peak current around 0.5 – 3 amperes and a rise time well below 20 ps as shown in Figure F2. These current pulses can bypass on-chip CDM protection structures and damage sensitive transistor inputs. Due to the small total energy of the event, this type of ESD event poses higher risks for ultra-fast I/Os with a low gate oxide breakdown voltage. The breakdown voltage can be exceeded due to the fast di/dt during the initial part of the pulse.

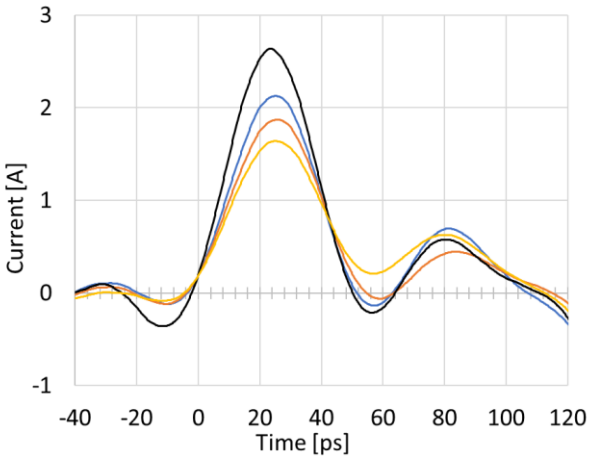


Figure F2: Four measured discharge current waveforms from a charged connector with initial voltages between 200 V and 400 V. The fastest measured rise time is 15.9 ps due to a 23 GHz bandwidth limitation.

F.2 Example and Case Studies

In previous sections of this appendix, the differences between CDM and other ESD models have been described. These differences include the energy/duration of the pulse, the source of the energy, and the generated failure modes. Thus, we need to compare FA from CDM and otherwise stressed samples. This section will describe classic failure types observed from CDM tests and compare/contrast this to those of the other failure types.

F.2.1 CDM

Figure F3 shows two photos of typical CDM damage. Figure F3a is a CDM failure at -500 volt, illustrating a classic CDM failure type involving the gate/source of two NMOS transistors in one domain whose gate is driven by logic from another domain. Figure F3b results from a CDM failure at -300 volt on an input buffer. It should be noted that in both cases the transistor is small and while the damage is clearly visible, it only takes a relatively small amount of current to cause this damage.

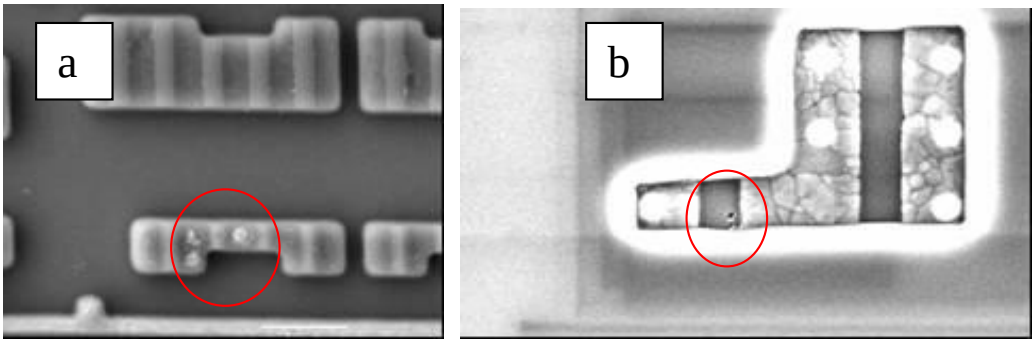


Figure F3: CDM failures of two NMOS transistor gates driven by cross-domain logic (a) and an input transistor (b).

F.2.2 HBM

Figure F4 shows two HBM failures. Figure F4a is a 2000-volt HBM failure illustrating a classic HBM failure type involving the drain/backgate junction of a larger MOS I/O transistor. The current path of this zap was a positive zap between the damaged pin and a nearby ground pin. Figure F4b is the failure of a core transistor for a stress between Vdd and Vss.

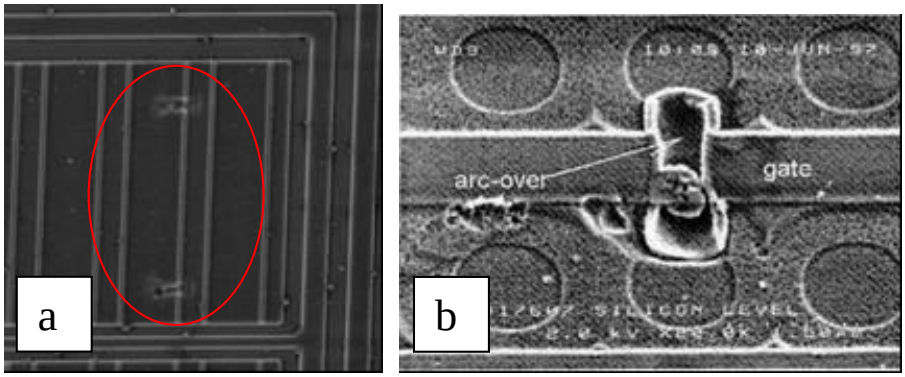


Figure F4: 2 kV HBM failures showing contact spiking/silicon damage.

Without a doubt, CDM failures look very different from the HBM failures and they occur at different locations on the chip. Electrical and ESD Simulation testing of these failures can show both leakage and functional changes and are not sufficient to determine the root cause of a field return. FA must be performed on product returns to find similarity with qualification fails.

It is clear that a correlation between HBM and CDM is not expected. A scatter plot of data of many products from different manufacturers, presented in Figure F5, makes clear that indeed a correlation is not observed. The correlation coefficient is just 0.26, which is equal to the correlation observed on an unrelated dataset in [14].

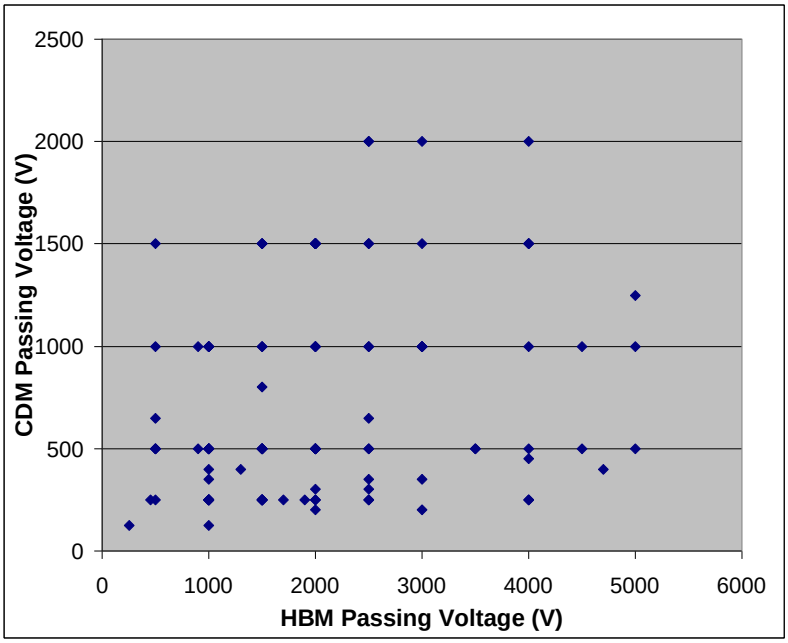


Figure F5: CDM vs. HBM levels for >100 different products.

F.2.3 System-level ESD

Some case studies that show little correlation between CDM failures and system-level (IEC) failures will now be discussed.

Case Study 1:

This case involved an IEC discharge directly applied to a device, where a CDM-like potential difference and high current resulted in failure at discharge to the enclosure. As the ESD gun discharged into the system enclosure, spark discharge was detected at a small gap between the enclosure and system PCB. This gap was close to a ground trace of the PCB where the damaged device's ground pin was connected. A power supply clamp between a power supply and ground was damaged as is shown in Figure F6a. The damage was caused by the uncontrolled discharge through the clamp, started by the spark. It was observed that the damage voltage was dependent on system enclosures, where the gap between the enclosure and PCB was varied.

Case Study 2:
This case resulted from direct discharge to a system board connector terminal, where no correlation to device CDM failure was observed. In this case, the connector contact was badly damaged as a result of a high current applied to the terminal. An examination of the PCB revealed a printed circuit parasitic pattern from the connector to the device. The initial high frequency / high current portion was blocked off because this pattern worked as an inductance. When the applied waveform was measured at the IC, no initial pulse was detected. Only the second peak reached the IC. The resulting damage is shown in Figure F6b.

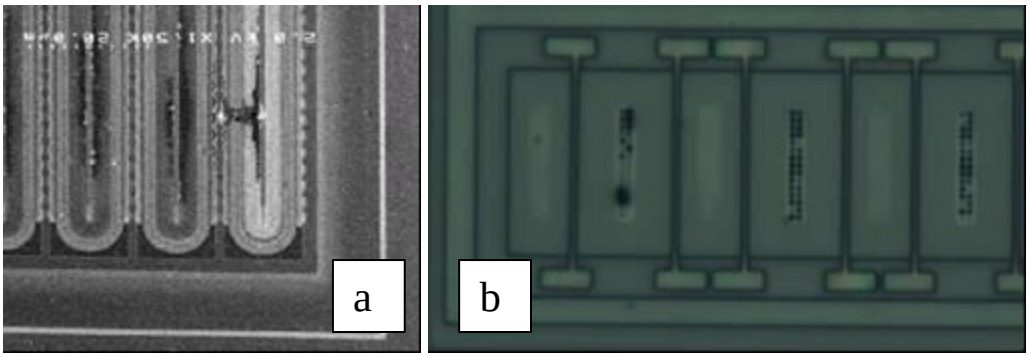


Figure F6: Damage in a power driver LDMOS (a) and damaged drain contacts of output buffer NMOST (b) due to system-level ESD.

These case studies illustrate that non-correlation between CDM and system-level (IEC) was observed. Additionally, these studies illustrate that component-level ESD protection alone is not sufficient to achieve high system-level protection.

F.2.4 EOS

Two examples of EOS damage are shown in Figure F7. Figure F7a shows the result from a 2-pin test, with stress to the input pin with respect to ground. The stress was an over-voltage of 1.5*Vcc value, using a parametric analyzer. Figure F7b shows the damage due to a 1.5*Vdd stress on a power supply pin with respect to ground. This was performed while the device was otherwise normally powered. The damage occurred in the core of the IC. The characteristic discoloration is easily observed.

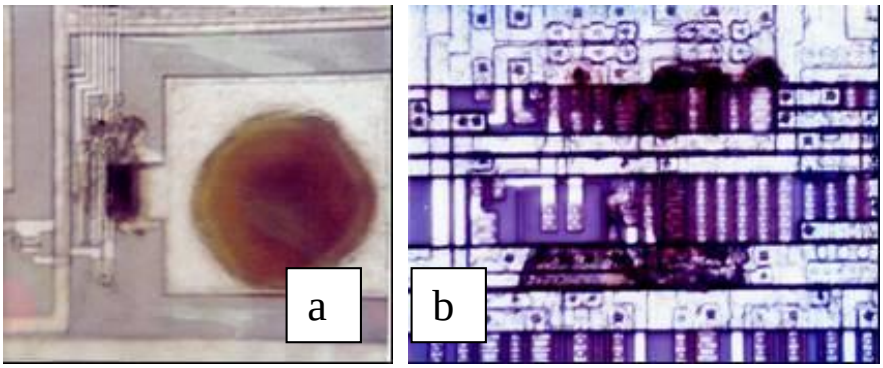


Figure F7: EOS damage, at an input pin (a) and in the core (b)

F.2.5 CBE

This case study involved melting of an ESD protection diode, shown in Figure F8, at the IC terminal of a device on a system board. A TLP tester was used to apply the stimulus to simulate the CBE. The failure charge of the diode was measured as 3.6 amperes / 100 ns, corresponding to 360 nC. Given the device capacitance of this IC was 12 pF, a 30 kilovolt CDM event would be required to produce the same charge. This is much higher than levels achievable from a single component CDM test (1ns time constant discharge).

The PCB capacitance containing the IC was measured to be 20 times that of the device capacitance, or, 240 pF. The discharge time constant of this higher capacitance was 2.5 times that of the CDM time constant. If the PCB is charged at 500 volts, the total energy will be at the same level as above. This illustrates clearly that CBE is not correlated to CDM. Section G.5 gives more details on comparable case studies.

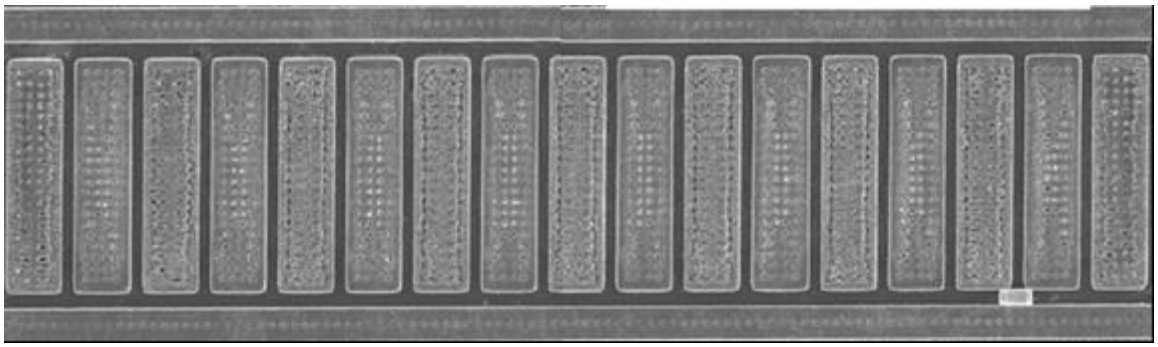


Figure F8: All contacts of the ESD protection diode were damaged.

F.3 Conclusions

This appendix shows that there is no correlation of CDM to any other stress types expected. Therefore, CDM cannot be replaced by, nor replaces, any of the other stress types. An increased CDM level will not lead to higher performance for other stress types.

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Appendix G: Charged Board Events and Relationship to CDM

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G.1 Charged Board Event Problem Statement

Printed circuit board (PCB) ESD failures have received significant attention from the 1980s to today. The PCB ESD focus until recently has been largely on ESD protection at the system level which has been discussed in Appendix F as well as in the Industry Council on ESD Target Levels White Paper I.

There are four distinct mechanisms for discharge transients associated with a PCB [1]. In the first mechanism, if a charged person touches a PCB that is already grounded, the discharge transient represents HBM and the resulting damage will be HBM in nature. In the second mechanism, if a charged cable (which gets charged by triboelectric friction such as dragging) comes into contact with a grounded PCB, a cable discharge may result in a PCB component experiencing damage. In a third mechanism, if an ungrounded charged machine comes into contact with a grounded PCB, a component experiencing damage results from a machine model-like discharge. ANSI/ESD S20.20 & IEC 61340-5-1 do protect against cable discharge in ESD-controlled manufacturing environments, but for systems built for the non-ESD controlled environment of home or office, such systems should be ESD protected to withstand cable discharge.

Since the late 1980s, theory and evidence have indicated a fourth ESD threat mechanism due to the charging/sudden discharging of system boards.

Pierce [2] initially described a relationship for ESD failure voltage by comparing the capacitance characteristics of a component versus a PCB and the failure voltage of a component, relating the ESD failure energy of a component to the system delivering the energy to the IC. For the same energy, a much lower failure voltage was found to result. Boxleitner [3] in 1991 further described circuit board layout characteristics and variations in discharge paths to result in a wide variation in component failure voltage on a system board, down to $1/100^{th}$ of the failure voltage of the individual component. Lin [4] described AT&T work attempting to model a FICBM (field-induced charged board model) discharge on a 6” by 12” circuit board, with hardware closely approximating common non-socketed CDM testers. A FICBM waveform specification for such a circuit board was developed including peak current, rise time, and pulse width.

The majority of the literature refers to the charged board event as the charged board model (CBM). There is, however, no standard document describing a charged board stress test such as exists for the device level tests of HBM and CDM. It can therefore be misleading to refer to charged board ESD events as CBM since that implies a standardized test. For that reason, this document will use the charged board event (CBE) nomenclature.

G.2 Charged Board Event (CBE) Overview

Conceptually, a CBE is similar to the charged device model (CDM) event for a packaged component. During a CDM event, the charge stored by a packaged IC discharges just (nanoseconds to picoseconds) before contact is made with a conductive object at or near ground potential. During a CBE, the charge stored by an entire PCB discharges just (picoseconds to nanoseconds) before contact is made with a conductive object at or near ground potential. Thus, a CBE can be thought of as an extension of the charged device model where the PCB is the "device" that stores the charge. However, since a PCB can store far more charge (due to higher board plane capacitance) than a single IC, the peak discharge current for a CBE is typically much higher compared to a CDM event. Consequently, the damage from a charged board discharge can be quite severe and can be easily mistaken for electrical overstress (EOS) damage.

There are three different methods to charge up a board, and similar means of discharge. In the first method, if an ungrounded PCB is held by a charged person and a metal component such as a bare metal heat sink is then exposed to a ground potential, any resulting component damage will be CBE in nature. In the second method, the off-board edge connector on the charged PCB usually makes contact with the card-frame connector into which the PCB is being pushed. The PCB rapidly discharges via whichever connector makes contact first, and the susceptible ICs in its path may fail. In a third method, board-mounted ICs can be damaged by the discharge current which flows when a charged PCB is grounded via wave soldering, an input connector, by an electrical tester, or contact with a metal object having a large capacitance. Here the PCB is in the electric field of a charged object or surface, the insulating materials on the PCB (such as plastic sockets, plastic covers, or connectors) develop a charge, the conductive portions of the PCB including the components develop voltage upon discharge by becoming grounded in the field from charged insulators on the board. Damage resulting from the discharge of this voltage to ground is also a charged board failure.

G.3 Relation of Charged Board Events to Component-level ESD Test Methods

Component-level electrostatic discharge (ESD) standard models in widespread use in the electronics industry include the human body model (HBM) and the CDM. For integrated circuits (ICs), ESD testing to these models is conducted on an individual component basis, i.e., ICs are not mounted to a Printed Circuit Board (PCB) when stress-tested for qualification. This component-level ESD testing is effective at simulating manual and automated real-world ESD events that occur on ICs before PCB mounting. However, component-level ESD testing is not a good predictor of how susceptible ICs are to ESD after they are mounted on a PCB. In fact, an IC mounted to a PCB may be much more or much less susceptible to ESD than when this same IC is handled individually. Supporting information can be found in Appendix F, Sections F.1.4 and F.2.5.

G.4 Charged Board and Related Failure Case Studies

Previous work details case studies of actual charged board events and lowered failure levels relating parasitics of a system compared to that of a component.

Olney [5] described the "Charged Strip Model" susceptibility of parts connected together as strips in an interconnected package leadframe. This susceptibility occurs when the individual pins are disconnected from the interconnected leadframe. Charge and subsequent discharge of

disconnected pins (both from a tester pogo pin issue and on a cut down strip with a CDM tester) showed much lower failure strip CDM voltage levels compared to CDM levels of the individual components. The net capacitance of the collective leadframe connected packages is a function of the number of packages with the discharge path through the very low interconnected leadframe resistance/inductance.

This work led to a more detailed study [6] documenting unique ESD field failures of components assembled on boards. Two examples from this paper served to illustrate board charging issues during manufacturing resulting in severe ESD damage.

G.5 Example Charged Board Event Testing Methods

In [5, 6] a commercially available non-socketed CDM test system was used to test the strip, the specially designed CBE test board, and a customer return board. This CBE methodology is acceptable as long as the board or board section fits inside the area of the field charging plate, which is generally less than 4 inches square. Figure G1a shows a photo of a board tested using the setup in [6].

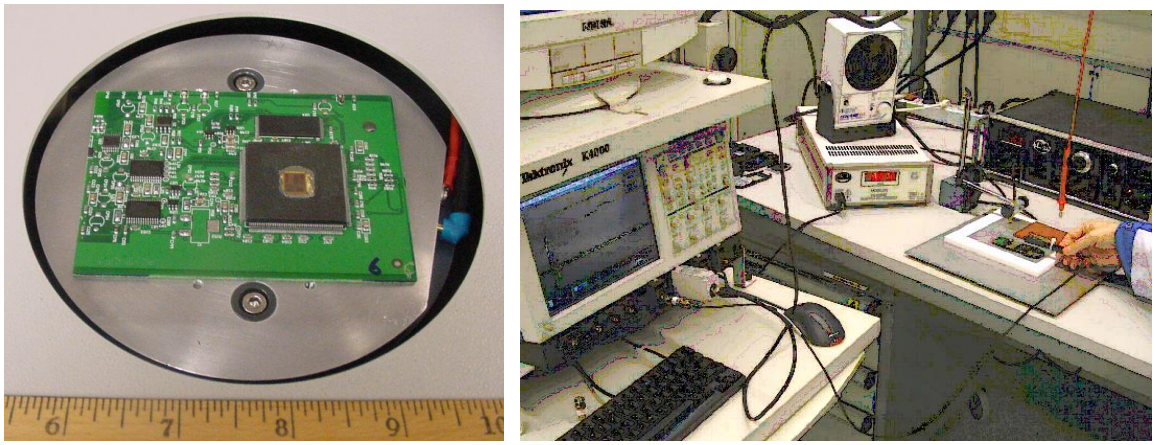

Figure G1a (left): Photo of customer PCB on commercial CDM tester. Figure G1b (right): Custom designed CBE evaluation system for PCBs.

A second setup used in the CBE evaluation of PCBs will now be described. The CBE ESD stress test principle can be used to validate ESD sensitive components on a system level. The method is adequate to evaluate ESD withstand of sub-assemblies and modules [7]. CBE withstand is valid also in the manufacturing environment and ESD risks can be estimated by using electrostatic source circuit parameters such as capacitance, potential, and charge.

The test setup for the CBE method is shown in Figure G1b and its corresponding circuit model is shown in Figure G2. The PCB under test is placed on an electrically floating induction plate. A dielectric foil separates the PCB from the plate. The capacitance of the PCB is set according to the required stress level by setting the correct thickness of the dielectric layer. Thin dielectric represents the highest CBE stress level for the PCB and a thicker dielectric can be used to adjust stress level to represent a real-world situation. The induction plate is separated from the ground plane by a second dielectric plate. The induction plate capacitance can be adjusted according to

the influence found in the process, or to evaluate a general level (as an example, four times higher than the PCB capacitance) by changing the area of the plate or thickness of the dielectric.

CBE stressing is carried out as follows. The PCB is placed on a thin dielectric foil and both the PCB and the induction plate are neutralized. Then a high voltage generator is used to apply a stress voltage on the floating induction plate. The induction plate will induce a potential on the PCB, and as soon as the potential stabilizes the voltage source is disconnected. The point discharge location of interest on the PCB is touched by a probe with a short grounding wire. The initial and residual potential of the induction plate is recorded before and after a discharge. Equations (1-4) are used to calculate discharge parameters and the stress level is given by Q_{mobile}, E_{ESD}, and stress voltage. In addition, $C_{induction}$, C_{PWB}, $C_{ESD,}$ and L values have to be given to validate the stress level. An oscilloscope can be used to measure the discharge current and transferred charge.

$$C_{ESD} = \frac{C_{Induction} \cdot V_{Initial} - C_{Induction} \cdot V_{\mathrm{Re}sidual}}{V_{Initial}} \quad (1)$$

$$Q_{Mobile} = C_{ESD} \cdot V_{Initial} \quad (2)$$

$$E_{ESD} = \frac{Q_{Mobile}^2}{2 \cdot C_{ESD}} \quad (3)$$

$$L = \frac{\left(\frac{1}{2\pi f_0}\right)^2}{C_{ESD}} \quad (4)$$

Where:

$V_{Initial}$ is a potential of the induction plate before the ESD event.

$V_{Residual}$ is a potential of the induction plate after the ESD event.

$C_{Induction}$ is a capacitance between the induction plate and a ground plane. C_{PCB} is a capacitance between discharge circuit of the PCB and the induction plate which can be measured.

C_{ESD} is a source capacitance of the discharge circuit, which consists of a serial capacitance $C_{induction}$ and C_{PCB}.

Q_{Mobile} is a transferable charge of the discharge circuit.

E_{ESD} is the calculated energy of the discharge.

L is the inductance and is calculated from a resonant frequency when applicable.

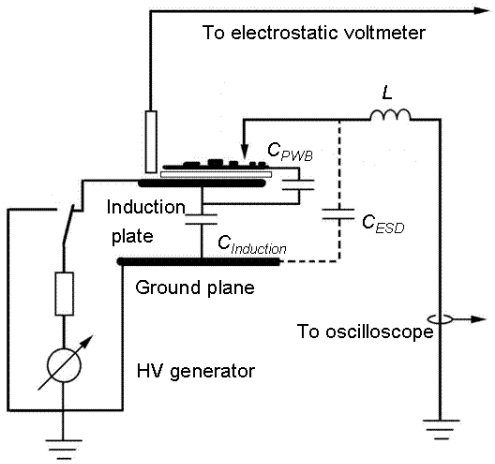

Figure G2: CBE method allowing variability in measuring CBE board risk to devices.

G.6 Charged Board Event Test Results

An example of the CBE discharge from the setup described in the previous section is shown in Table G-I. Discharge parameters are captured from a small PCB (size 40 mm X 100 mm) and a single PGA component (size 10 mm x 10 mm). Here the PCB represents the CBE discharge and the PGA gives the CDM parameters with the same setup. CBE discharge parameters depend on the electrostatic source circuit and discharge circuit. In this example, the discharge was made through a 40 mm long ground wire and a CT-2 current probe was used to capture the discharge current. Measured discharges are presented in Figure G3 and the discharge circuit parameters in Table G-I.

Table G-I. Source circuit parameters and calculated discharge parameters

Stress Level	**$C_{Induction}$** [pF]	**C_{PWB}** [pF]	**C_{ESD}** [pF]	**$V_{Initial}$** +/- [V]	**$V_{Residual}$** +/- [V]	**L_{Stray}** [nH]	**Q_{Mobile}** [nC]	**$E_{Potential}$** [uJ]
CBE	89	33	24	1024	748	< 30	25	13
CDM	89	3	3	1024	995	< 30	2.6	1.3

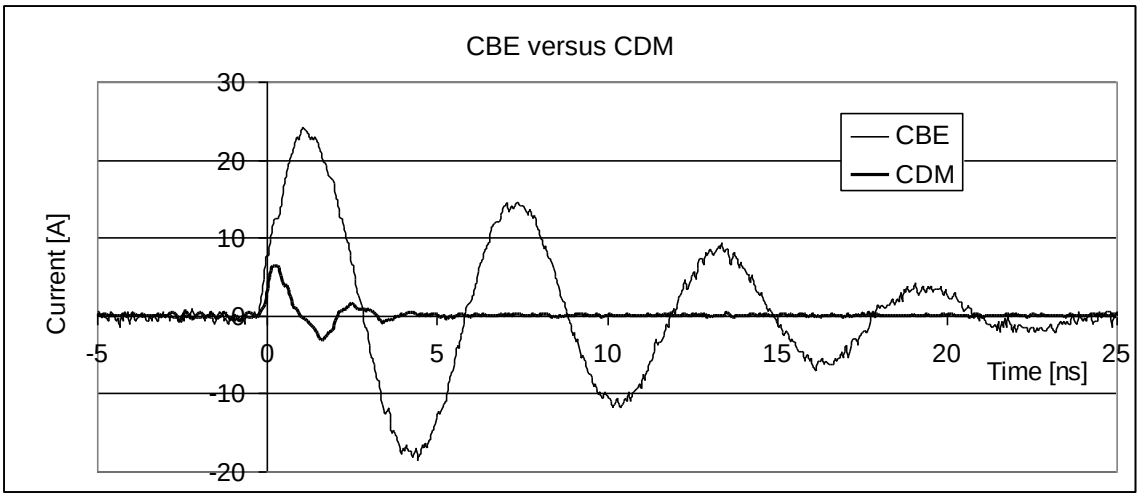

Figure G3: Comparison of CBE and CDM discharges from the CBE discharge setup.

Returning to the CBE test setup in [6], Figure G4 compares the CDM discharge waveform for a single digital signal processor (DSP) IC to the charged board waveform for the same DSP device mounted to a customer return PCB shown in Figure G1a. Not surprisingly, for a given charge voltage (250 volts in this case), the CBE discharge has a much higher peak current than the CDM discharge. This is because the PCB capacitance is much higher than the IC package capacitance. Also, the CBE event has a faster rise time than the corresponding CDM event. This is because the inductance of the discharge path, in this case, is lower on the PCB than on the stand-alone DSP device. This was primarily because the traces on the measured PCB are much wider and thicker than bond wires on an IC, which is generally the case. The net result of the much higher peak current / faster waveform rise time for the PCB is that a given IC that is effectively immune to ESD damage at the device-level may be quite susceptible to ESD damage at the board level. If the mounted IC is in the primary discharge path on the PCB, the CBE ESD damage on the IC will be much more severe. Consequently, such ESD damage can look like EOS damage.

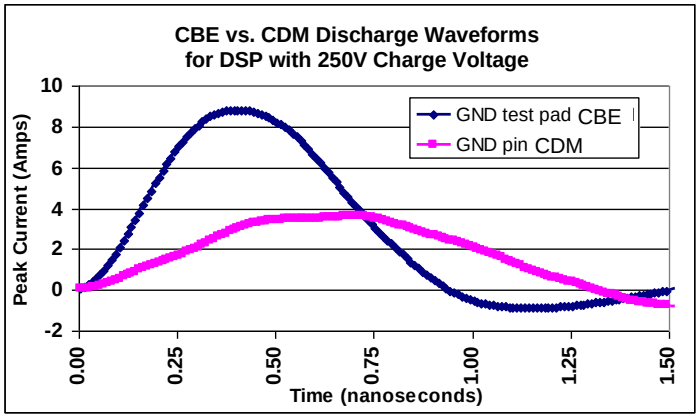

Figure G4: Comparison of CBE vs. CDM discharge waveforms.

G.7 Identifying and Minimizing Charged Board Event (CBE) Failures

ICs are most susceptible to CBE ESD damage if one or more of the following conditions apply:

1. The IC is adjacent to large insulators such as plastic sockets, plastic covers, or plastic connectors that can develop a charge.
2. The IC is close to PCB edges, especially PCB edge connectors, mounting holes, or test points.
3. The IC has numerous supply/ground pins that are soldered to board supply/ground planes, especially if the board supply/ground planes are large relative to the IC.
4. The IC has a large die that results in a very low impedance discharge path, especially if the IC is the primary discharge path for the PCB.
5. The PCB does not include explicit EOS/ESD protection such as Transient Voltage Suppressors and Schottky diodes across the supply planes.

ICs and other components on PCBs are most susceptible to CBE ESD damage during the processing steps from when they are first populated with components until they are inserted into a case or other enclosure that provides adequate ESD protection. Balanced ionizers should be used throughout PCB manufacturing lines to minimize PCB charging, particularly during steps when insulating components (sockets, connectors, etc.) are mounted, and just prior to convection/IR reflowing or wave soldering. This is also supported by a case study in CDM Control, Chapter 3 (Section 3.2.2) of this document.

Also, it is a design mistake if a connector is designed so that an I/O pin can make the first electrical connection. Typically it is the ground pin or EMC shield around the connector that must make the first contact.

CBE sensitivity is a function of the board size/layout, charging potential of the board/materials used on the board, and particular assembly steps. A particular CBE test setup cannot duplicate all possible scenarios of CBE discharge. The measured peak current is also a function of where on the board the current is measured. CBE sensitivity analysis is best suited to individual applications; where the particular combination of CBE conditions can lead to assessments of CDM withstand voltages needed for the particular application.

Adherence to a certified ESD control program such as ANSI/ESD S20.20 from the ESD Association when assembling or handling circuit boards and installation of boards into systems can help prevent such failures from occurring [8]. However, it does not guarantee that CDM / CBE failures will not occur. For example, an assembly step of pulling protective tape from an LCD screen and subsequent assembly of the LCD onto a PCB may only take a second or two, not long enough for a balanced ionizer to remove the developed charge from the LCD.

G.8 Summary

Charged Board Event ESD is not as well documented as other ESD models but they represent a major real-world ESD threat in electronics system-level manufacturing. Even if all the individual components used for a given PCB have high device-level ESD robustness, one or more of these components may be very susceptible to ESD damage after mounting to a PCB. Since a PCB has much higher capacitance than an individual device, CBE damage can be much more severe than CDM damage. Therefore, before attributing an IC failure on a PCB to EOS, the possibility of charged board ESD damage should be explored. Adherence to a certified ESD control program, such as ANSI/ESD S20.20 from the EOS/ESD Association when assembling or handling circuit boards and installing boards into systems can help prevent such failures from occurring, but further analysis of the manufacturing environment is critical to understand the development of charge/subsequent rapid discharge of boards.

In 2016, WG25 within the EOS/ESD Association published ESD TR25.0-01-16, a technical report on CBE [9]. It summarizes much of Appendix G's work up to this time and provides more CBE test hardware/simulation information.

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Appendix H: Impact of CDM Requirements on Products

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H.1 CDM ESD Requirements

As described in Chapter 1, an understanding of CDM ESD has developed since the 1970s. Over the years, levels for CDM have been an ever-changing target. As shown below in the roadmap for ESD [1] Figure H1, in the earlier years, CDM design target levels were significantly lower. As demands for improved CDM levels in manufacturing sites continued, design goals were adjusted upwards reaching levels in the mid-1990s which became unrealistic to maintain for advanced technologies. An improved understanding of the manufacturing environment [2, 3] and the ever-present need to push for higher I/O performance (see Chapter 2) in advanced technologies have combined to push down design target levels.

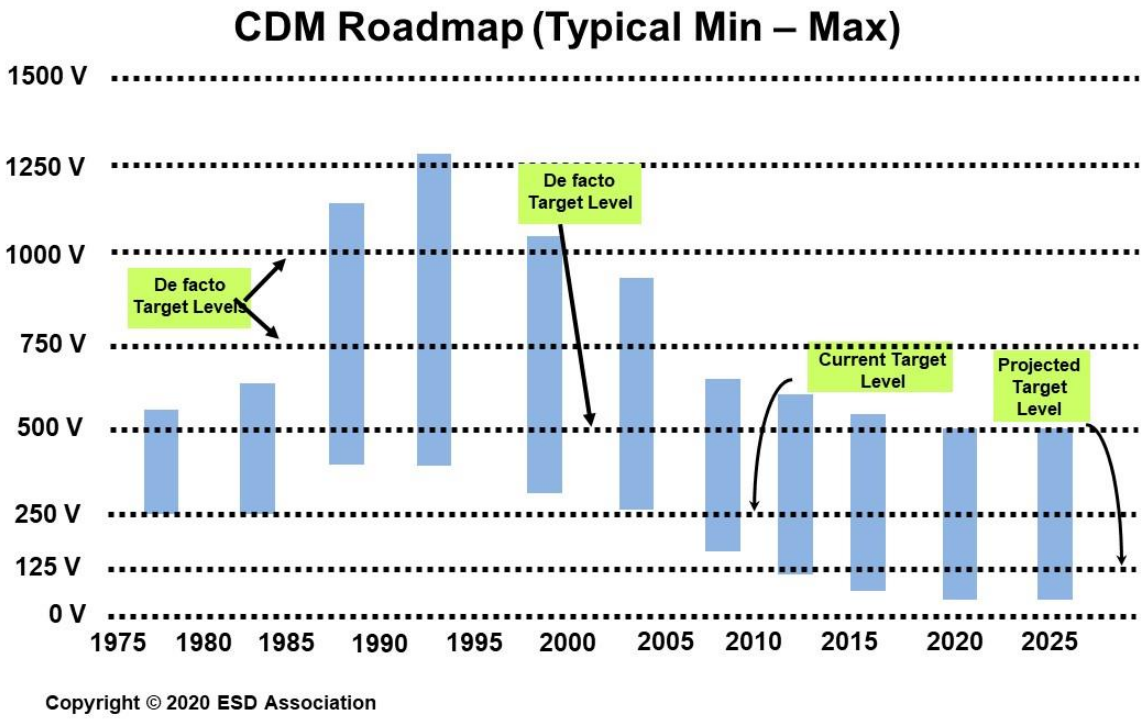

Figure H1: Evolution of CDM Design Levels vs. Time [1]

In the past, most major semiconductor suppliers quoted a CDM target level of 500 volts or less for CDM protection. But even with the reduced CDM targets, the demands of ESD protection devices create a constant chip design challenge, balancing I/O performance against CDM targets. The next section reviews the impact on products from many major semiconductor manufacturers.

Looking at CDM ESD levels from the customer side of the semiconductor industry, one finds a broader list of requirements ranging from 250-500 volts with many customers to as high as 750

volts to 1000 volts. Customers requesting 1000 volts do not appear to have a clear justification for these target levels other than organizational inertia. Some customers have no target level at all. In the automotive industry, the AEC-Q100 specification still calls out a 750-volt requirement for corner pins, although a separate corner pin requirement becomes more difficult to justify in today's advanced packaging. Within the Telecommunications market segment, the need for high-performance I/Os has dictated a much more flexible CDM ESD environment in which many customers allow significantly lower CDM target levels and are still able to manufacture these products with minimal risks.

In general, there is a wide variation within the electronic industry in regard to target levels needed for CDM ESD and over the years the acceptance levels have varied greatly.

H.2 Impact of Goals on Products

Looking at the impacts these goals have on products, we see that it impacts both suppliers and customers. Table H-I summarizes some real-life examples supplied from various semiconductor houses on the impact of a CDM goal of 500 volts.

Table H-I: Work Effort to Improve ESD Levels to 500 V

Product	Impact	Schedule delay	Effort Impact	Tech node
P1	Package modification	No	5 person-months	-----
P2	ESD performance de-rated	Yes	30 person-months	90 nm
P3	Circuit redesign	No	10 person-weeks	180 nm
P4	Circuit redesign	Limited	5 person-months	SOI
P5	Minor circuit redesign	Limited	2 person weeks	250 nm
P6	ESD performance de-rated	Yes	40 person-months	65/90 nm
P7	Circuit redesign & ESD de-rate	No	18 person-months	65/90 nm
P8	ESD de-rate	No	5 person-months	65 nm
P9	Circuit redesign & ESD de-rate	No	8 person-months	90 nm
P10	Circuit redesign	No	9 person-months	45 nm
P11	Circuit redesign	Yes	10 person-months	180 nm
P12	Circuit redesign	Yes	12 person-months	180 nm
P13	ESD de-rate	No	2 person-months	90 nm
P14	Circuit redesign	No	30 person-months	45 nm
P15	Tester artifact	Minor	4 person-months	130 nm
P16	Circuit redesign	Yes	1 person-yr.	180 nm
P17	Circuit redesign & ESD de-rate	Yes	4 person-months	130 nm

As can be seen, the impact included significant costs to the supplier in terms of work required to improve the CDM level and significant costs to the customer in regard to schedule delays. Also, in several cases, even with a re-design effort the CDM target levels were still not achieved, resulting in a lowering of the product CDM levels. This effort in many cases was unnecessary as the impact on the manufacturing environment was insignificant. More details on manufacturing environment impact can be found in Chapter 3.

Looking at this data from Table H-1 in a slightly different way, it can be shown that this challenge is only getting worse. Moving into more advanced technologies will tend to aggravate the risk that circuit redesign is required to meet the current target levels. This will inevitably lead to additional delays in product launches and/or more products de-rated with respect to the current CDM targets. Please refer to Figure H2 in which the work effort to improve CDM target levels is compared to the technology node.

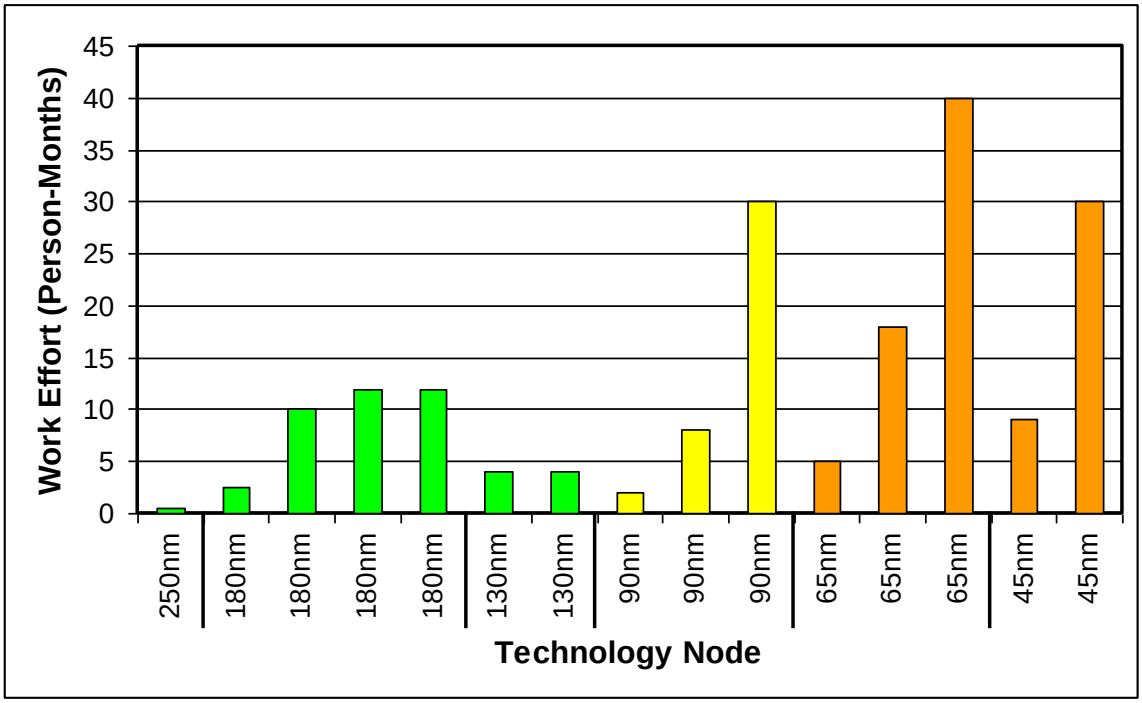

Figure H2: Increasing CDM Redesign Effort with Successive Technology Nodes. Each column represents the additional effort of a single design project to raise the CDM level above 500 V

Additionally, end customers will continue to see de-rating of CDM levels for certain pins and/or pin types to be an increasing solution to the problem of hitting the CDM target levels. As was shown in Chapter 2, this is due to the ever-increasing challenge of balancing ESD protection against I/O performance. In many cases, an I/O cannot meet the CDM target level without significant performance hits to the product and a negative impact on the product launch. Additionally, semiconductor houses today may relax CDM goals in one of the following ways:

-Reduction in CDM target levels based on the operating frequency of the pin
-Reduction in CDM target levels based on the package size

Some of these actions are readily accepted even today in market segments where the demands of I/O performance outweigh the ESD risk. Products today have been shown to be handled with CDM target levels even as low as 50 volts.

H.3 Supplier / Customer Impact of a Revision to the CDM Target Levels

The reduction in the CDM ESD target level to 250 volts has resulted in a significant benefit to both the supplier and the customer:

- Elimination of a significant number of circuit redesign efforts and corresponding work effort/requalification that results
- I/O area savings with a reduction in ESD protection area
- I/O performance improvements from a reduction in capacitance/resistance
    - An ever-increasing demand for higher I/O performance can be achieved. Capacitance on I/O's can be reduced by 40-50% with a reduction in the target levels
- Improvements in time to market for many products
    - Improved time to market with higher performance I/O's will greatly benefit end customers

These changes would have no significant impact on the manufacturing environment.

Elaborating on the I/O performance benefit and referencing again Figure 19 from Chapter 2, one can see the significant upside in the pin count of packages that can accommodate higher frequency pins. In many cases the pin count is increased by nearly an order of magnitude over a package limited by a 500-volt CDM goal, making 500 volts an unrealistic target for large packages.

References

[1] ESD Technology Roadmap from the ESD Association, https://www.esda.org/standards/

[2] T.J. Maloney, "CDM Protection, Testing and Factory Monitoring is Easier Than You Think", 2007 Taiwan ESD Conference Proceedings, pp. 2-8 (invited keynote speech and paper).

[3] J.A. Montoya and T.J. Maloney, "Unifying Factory ESD Measurements and Component ESD Stress Testing", EOS/ESD Symposium pp. 229-237, 2005.

Revision History

Revision	Changes	Date of Release
1.0	Original release	March 2009
2.0	Grammar corrected throughout. Technical corrections in Appendix A, B, and D.	April 2010
3.0	A major revision to address high-speed I/O CDM target levels in the regime of 56 Gb/s and higher, new process assessment techniques, and better alignment of the document with the latest technology trends with the following high level updates: -Executive Summary updated -Major revision to Chapters 2, 3, and 5 with many figure updated/added -Two new appendices were added (A & B) -Previous Chapter 4 moved to Appendix H and updated -Improvements in Industry test standards have been reflected in a major revision of Appendix C. -New questions added and many questions updated in FAQs -Previous Appendices A/B/D/E changed to Appendices D/E/F/G respectively -Appendix F Section F.1.4 updated -Appendix D Section D.3 updated -Formatting/grammar/minor updates throughout. -New figures added: 20-26, 36-38, 45, A1, B1, B2, C8, C9, C13, C14, C16, C17, C24, D5, F2 -Figures that were updated/modified: 1, 2, 5, 8, 9, 12, 13, 15, 16, 18, 27, 28, 44, C5, H1 -New tables added: B-I, C-I -Tables that were modified: I, IV, C-II, C-III, E-II, F-I	May 2021