White Paper 1: A Case for Lowering Component Level HBM ESD Specifications and Requirements

Industry Council on ESD Target Levels

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Revision 4.0

Abstract

For more than 20 years, IC component level ESD target levels for both HBM (2 kV) and MM (200 V) have essentially stayed constant, with no focus on data to change these levels. Today's enhanced static control methods required by OEMs do not justify these higher HBM/MM levels as data will show in this document. ESD over-design to these levels in today's latest silicon technologies is increasingly constraining silicon area as well as performance, and is leading to more frequent delays in the product innovation cycle. Based on improved static control technology, field failure rate, case study and ESD design data, collected from IC suppliers and contract manufacturers, we propose a reduction to a more realistic and safe HBM ESD target level which ensures a minimum MM performance level. This new HBM level (1 kV HBM) is easily achievable with static control methods mandated by customers and with today's modern ESD design methods.

As discussed in JEP172, MM testing is redundant to HBM and produces the same failure mechanisms. As a result, target level discussions for MM have been removed from this document as they are not applicable in component level testing (see JESD47 [1]). In addition, Chapter 3 from the previous revision of this document has been moved to Appendix A. This is to preserve the data for future reference.

[1] JEDEC JESD47, "Stress-Test-Driven Qualification of Integrated Circuits", www.jedec.org

About the Industry Council on ESD Target Levels

The Council was formed in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, original equipment manufacturers (OEMs), ESD tester manufacturers, ESD consultants and ESD intellectual property (IP) companies.

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Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products for allowing safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for the future ESD target levels. The Council Members and Associates will promote these recommended targets to be adopted as company goals. Being an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Preface

This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD level requirements. We will show through this document why realistic lowering of the ESD target level for HBM component level ESD is not only essential but is also urgent. The document is organized in different chapters to give as many technical details as possible to support the purpose given in the abstract. We begin the paper with an Executive Summary and chapter highlights followed by frequently asked questions (FAQ) so that the reader can readily find critical information without having to scan through the whole document. Additionally, these FAQ are intended to avoid any misconceptions that commonly occur while interpreting the data and the conclusions herein. All component level ESD testing specified within this document adheres to the methods defined in the appropriate JEDEC and ESDA/ANSI specifications.

Since the first release of White Paper 1, additional work has been completed to show that MM qualification testing is not needed. This has been released as a separate JEDEC publication, JEP172 [1]. MM qualification testing is not a required component level qualification test per JEDEC (see JESD47 [2]), EOS/ESD Association, AEC and JEITA. HBM and CDM testing are sufficient component level qualification tests to assess IC ESD robustness. In response to JEP172, this update to White Paper 1 will remove references to MM qualification testing, with Chapter 3 being moved to Appendix A. It should be noted that this discussion is only for MM *qualification testing*, this does not imply that there are no risks in an ESD protected area (EPA) due to isolated conductors. The Industry Council recommends an appropriate ESD control program is put in place as per ANSI/ESD S20.20 or IEC 61340-5-1 in order to ensure low risk to isolated conductors. An assessment of MM performance can be determined by the HBM qualification test data as discussed in Appendix A.

It should be noted that several figures related to technology nodes are from the initial release of the white paper in 2007. While the data is older, the trends and conclusions from that data still hold true today.

[1] JEDEC JEP172, “Discontinuing Use of the Machine Model for Device ESD Qualification”, www.jedec.org

[2] JEDEC JESD47, “Stress-Test-Driven Qualification of Integrated Circuits”, www.jedec.org

Scope

The intent of this white paper is to document and provide critical information to assess and make decisions on safe ESD level requirements. The scope of this document is to provide this information to quality organizations in both semiconductor companies and their IC customers.

1.1 Special Notes on the System Level ESD:

1. This work and the recommendations therein are intended for Component Level safe ESD requirements and will have little or no effect on system level ESD results.
2. Systems and System boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations from this work, and that all proper system reliability must be assessed through the IEC test method.

1.2 Special Notes on the Machine Model:

1. The machine model (MM) method as specified by some customers and suppliers is not a qualification methodology by JEDEC for use in place of or in addition to HBM and CDM test qualification.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by independent ESD experts from different semiconductor supplier companies as well as contract manufacturers. The data represents information collected for numerous different products selected for the specific analysis presented here; no specific components are identified. The readers should not construe this information as evidence for unrelated field failures resulting from electrical overstress events or system level ESD incidents. The document only refers to component level ESD recommendations which should have no impact on system level ESD requirements.

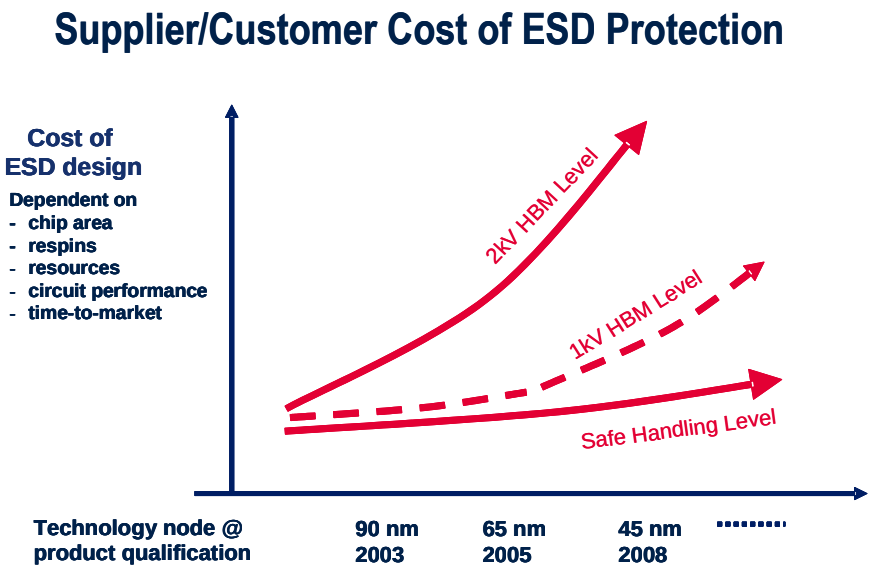
The Industry Council while providing these recommendations does not assume any liability or obligations for parties adopting these recommendations.

Executive Summary

In this summary we would like to offer an overview of the White Paper to present the most important issues and conclusions. Further details can be found in the various chapters of the document.

The ESD Challenge

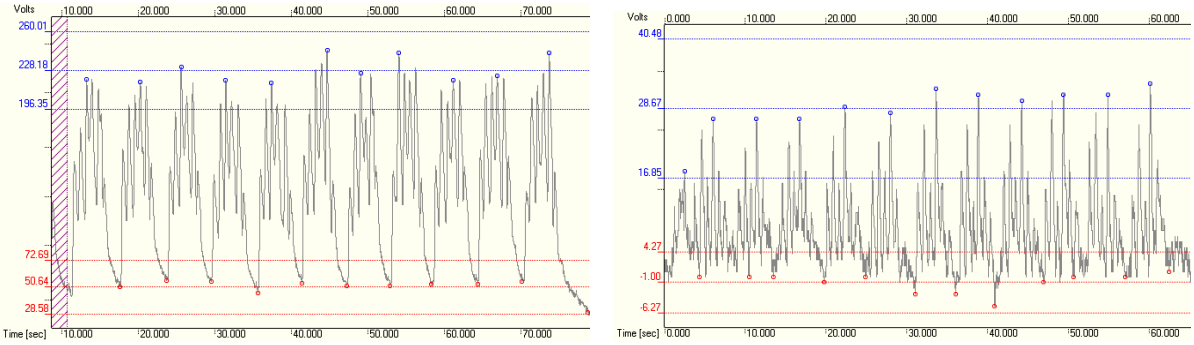
Problem:
The current industry ESD qualification target level for HBM is unsupportable, both in terms of what protection level is needed in a modern manufacturing environment, and what protection level can be practically achieved in an advanced technology IC, especially with high performance circuits. Across the industry we are today failing too many ESD qualification tests based on failures to target levels which have no bearing on real-world stress levels. These issues are having a severe and unnecessary impact on time to market and customer confidence.



Data:
While the commonly accepted 2 kV HBM requirement was set more than 20 years ago, we have ample evidence showing that this is an over-specified level both in terms of the existing ESD control methods which are effective to control at <500 V (**Chapter 2**), and the lack of any significant ESD field returns from products shipped with ≤2 kV performance (**Chapter 3**).

Executive Summary (cont.)

The voltage on a person's body as they walk in a controlled manufacturing environment



(a) (b)

(a) ESD levels with basic but less than ideal control methods: Generated Levels @ <500 V
(b) ESD levels with proper basic control methods: Generated Levels @ <100 V

The Proposal:

We propose a reduction in the HBM ESD target level to specify realistic ESD level requirements that accommodate both circuit design and safe handling and mounting in ESD protected areas.

HBM Level of IC	Impact on Manufacturing Environment
2 kV	Basic ESD Control methods allow safe manufacturing with proven margin
1 kV	
500 V	
100 V to <500 V	Detailed ESD Control methods are required

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Terms and Definitions

BGA	ball grid array
CDE	cable discharge event
CDM	charged-device model
CM	contract manufacturer
DIP	dual-in-line package
DSP	digital signal processor
DTSCR	diode-triggered SCR
EMS	electronic manufacturing supplier
EOS	electrical overstress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
FinFET	fin field-effect transistor
FOD	field oxide device
HBM	human body model
HF	high frequency
HSS	high-speed serial link
IEC	International Electrotechnical Commission
LNA	low-noise amplifier
MCM	multichip module
MM	machine model
MugFET	multigate field-effect transistor
PCB	printed circuit board
RF	radio frequency
SCR	silicon controlled rectifier
SERDES	serializer/deserializer transceiver that converts parallel data to serial data
SiP	system-in-package
SoC	system-on-chip
SOI	silicon-on-insulator
TDDB	time-dependent dielectric breakdown
TLU	transient latch-up
TVS	transient voltage suppressor
ULSI	ultra-large-scale integration
VDD	positive voltage supply
VSS	negative voltage supply

ESD design window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional.

It2: The current point where a transistor enters its second breakdown region under ESD pulse conditions and it is irreversibly damaged.

node: Within a circuit, a point of interconnection between two or more components.

protection impedance: The turn-on impedance of any ESD clamp during the ESD current flow

Highlights of the Document

Chapter 1: The origin of both the HBM and MM specifications are presented to give a historical perspective.

Chapter 2: The much improved ESD control methods that are in practice across the industry are described with illustration of how ESD is controlled to << 500 V HBM.

Chapter 3: Consolidated data from the Industry Council members is presented to show that the field returns are independent of the HBM level for which the products are shipped, and also making the important point that 2 kV requirement is outdated.

Chapter 4: The so called "cost" of ESD is described in terms of circuit performance, silicon re-spins, product delays, and unwarranted frustration for both suppliers and customers.

Chapter 5: The continued trend of silicon technology scaling to achieve high performance circuits is having a severe impact on ESD design. These issues are presented in detail to explain why the current standard spec of 2 kV HBM through protection design would soon become impractical to impossible.

Chapter 6: The differentiation between Component Level ESD and System Level ESD is outlined to show that reduction of the component level requirement does not have any relation to the system level reliability.

Chapter 7: Overall recommendations and justifications for modified ESD levels are presented. An overall ESD classification for IC products recommended for immediate application is presented.

Appendix A: The intrinsic MM performance as derived from the HBM protection levels is summarized to demonstrate that a MM evaluation is often redundant.

Frequently Asked Questions

Q1- Will the lowering of the HBM component ESD level have an impact on the overall system reliability?

*This is an often misunderstood concept. There has been no proof that components with lower HBM performance have seen more system level failures. As described in **Chapter 7**, since the system level test applies only to external interface pins this protection design strategy is quite different. In fact, as stated in **Chapter 7**, the Industry Council is in agreement that system levels ESD protection, cable discharge protection and transient latch-up are critical areas where future focus is needed.*

Q2 - If system level ESD testing does not guarantee system level (including component) ESD performance, isn't higher target component level HBM ESD better than nothing?

*This would only give a false sense of security while again going through extensive cost of analysis and customer delays and circuit performance impact. Our data and analyses in **Chapter 3** and **Chapter 7** clearly show that the system level ESD and component level ESD are not related to each other while the system ESD protection depends on the pin application and requires a different strategy. This document further argues that system level ESD is clearly important and targeting focus on excess component level requirements could pull resources away from addressing and designing better system level ESD.*

Q3 - Is the root cause of EOS failures related to prior ESD damage?
Do devices with lower ESD levels result in more EOS failures?
Do devices with lower ESD levels result in more system failures?

*This is not only an incorrect assumption, but it has persisted for many years. Whereas ESD (1 nS to 1 uS) is a subset of EOS, EOS events are much longer in time domain (microseconds to several tens of milli-seconds) and represent orders of magnitude higher thermal energy. EOS failures occur for different reasons. Several major studies in the past and within corporations have found no linkage between the two after tracking millions of products. The data presented in **Chapter 3** clearly supports this by showing that the tracked field returns are independent of their respective HBM ESD level when the devices were shipped. As described in **Chapter 7**, the system level protection requires a different test method and a different protection strategy. We have seen case studies that showed products passing a system level ESD of 8 kV based on the IEC System Level test method that were shipped with a corresponding HBM level of 500 V or less on a few pins. These lower level HBM pins as well as the 2 kV pins all equally performed well for the IEC test in the total system. Thus, lower component level HBM ESD results do not translate into poor system level ESD performance as the failure mechanisms & protection schemes are not the same.*

Q4 - While we agree that 1 kV or 500 V HBM is adequate and safe, how would one deal with competition that uses ESD as a marketing advantage?

Most customers who are informed, especially through this document, we hope would see that the only things that matter are consistent circuit performance to specifications and on-time product delivery. As long as the minimum required component ESD levels (as recommended here) are met, and basic ESD static control methods are in place, having a product ESD level at 1 kV, 2 kV or 4 kV does not enhance its system level ESD performance nor its susceptibility to EOS failure causes. For details on these please see ***Chapter 3*** *and* ***Chapter 7****.*

Q5 - Will the modified ESD level as recommended here shift the burden to manufacturers?

No, manufacturers have an obligation to provide basic ESD controls. Verification of these controls in their manufacturing and handling processes are necessary no matter what ESD levels are accepted. The current HBM ESD target level has been over specified. The modified levels reflect what is realistic and represent no shift of burden to the customers. Basic ESD controls from ***Chapter 2*** *as well as the substantial data of* ***Chapter 3****, collected on products shipped to different manufacturing sites with no special rigorous ESD control programs, strongly support these assertions.*

Q6 - Would basic ESD control methods be sufficient to tolerate 1 kV to 500 V HBM, or would one need special precautions?

Basic ESD controls ensure that devices with a HBM robustness of at least 500 V can be handled safely. The details are given in ***Chapter 2****. With detailed ESD controls, such as the ANSI ESD S20.20 and IEC 61340-5-1, even devices with a HBM robustness of 100 V can be safely handled with only a minimal incremental cost.*

Q7 - Will all CMs be able to guarantee that there is good control to safely meet these levels?

CMs handling electronic components typically have the expertise in basic ESD control programs. They are already generally required to provide and verify ESD control programs as a condition for doing business with their customers. As ***Chapter 2*** *describes, just the basic control methods easily ensure that devices with a HBM robustness of 500 V can be safely handled.*

Q8 - If these proposals address only HBM and MM, does it automatically mean that the CDM level requirements are reduced as well?

The Council has decided to first focus on HBM/MM and after collecting all the relevant data the proposals for realistic and safe levels for these models are presented. Likewise, CDM is also critical as a real world failure mode and in fact poses a more serious threat as a technology and design constraint. There has not been as much research to understand the real necessary CDM requirements level and how the CDM tester stress is correlated to the real world events. Also, there is much confusion in requiring a specific CDM level when it is known that the package dimensions have a significant impact on the stress level as mentioned in ***Chapter 5****. The Council has studied the CDM effects and collected data in order to recommend a safe and realistic level, studies have been completed and published in WP2.*

Q9 - Why is the Industry Council pushing reduction of the component ESD level now?

It has been widely observed for almost 10 years that the current requirements, while nearly universally accepted by customers, have been over specified and that lower levels are very safe. This realization about the component level ESD is also stated in ***Chapter 1****. As technology scaling continues and demands for even higher circuit performance prevail, it has become necessary that these specifications be reexamined and modified to realistically meet the current practices.* ***Chapter 5*** *outlines the IC technology changes that necessitated the reexamination of the specifications, while* ***Chapter 2*** *describes the state-of-the-art in basic ESD control methods that support a reduction of component ESD target levels. The recommendations for safe target ESD levels are given in* ***Chapter 6****.*

Q10 - Will the automotive lines handling lower 1 kV or 500 V HBM parts require any additional care?

Since basic control methods should apply equally effectively to all manufacturing lines the automotive products are expected to be just as safe with no additional special care. ***Chapter 3*** *illustrates this point by showing automotive versus non-automotive field return rates versus HBM robustness. However, this is not to be confused with requirements for IC pins with external interfaces that may be required to pass high ESD stress coming from the IEC System Level test. This differentiation of the component level HBM test and the IEC System Level test is discussed in* ***Chapter 7****.*

Q11 - How do we know there is enough data to convince us that the conclusions are correct?

The Industry Council has gathered enough consolidated data to show that the current component ESD levels are over specified. The data in ***Chapter 3*** *gives ample evidence for this conclusion, and the basic static control methods that are universally in practice as described in* ***Chapter 2*** *gives a high level of confidence for these recommendations.*

Q12 - There has been an assertion in a recent publication that the Industry Council is rushing in for modified ESD levels. Is this a valid assertion?

No. The Council has carefully researched the topic, collecting substantially relevant failure rate data, and coordinating this data gathering with product and quality engineers in our respective companies. These engineers, focused on continuous improvement in product quality, are equally convinced that there is enough evidence from their own experience after shipping billions of parts representing a wide range of product types that the modified ESD levels (as proposed here) indeed do make sense. A sample of this data is presented in ***Chapter 3****.*

Q13 - If these new recommended levels are safe, why was this not done before?

Both suppliers and customers have been comfortable in the past in meeting the required levels as long it was not a significant cost / schedule constraint to them. But over the last couple of years, it has become increasingly difficult to meet these current levels. An inordinate amount of time and resources as discussed in ***Chapter 4*** *is being spent to go through the complicated ESD testing for large pin count devices in an attempt to meet the target levels even if the failures had no real world consequences. However, the bottom line is that by bringing the ESD levels to more realistic levels much of the unnecessary cost of ESD design can be reduced allowing faster time to market as well as higher performance products to meet the customer needs. All of this can be attained with no impact to product reliability.*

Q14 - If we as customers are happy with the status quo why would we want a modified HBM component ESD level? What is in it for us?

We are quite certain that the IC product customers will gain confidence that this modified HBM component ESD level is safe and reasonable. By allowing this freedom to the suppliers the customer can expect higher performance products delivered with shorter design cycles. In other words, this should be a win-win proposal. This potential impact is presented in ***Chapter 4****.*

Q15 - Suppliers look at products that are shipped at lower HBM levels and say that no field return failures are seen. If not all the pins are weak, how can we be sure if this type of data has any relevance?

This is somewhat of a misunderstood concept. The data presented in ***Chapter 3*** *clearly show that the tracked field returns are independent of their respective HBM ESD level when the devices were shipped; i.e. most the field returns are due to EOS and not due to ESD. What is interesting from the* ***Chapter 3*** *data is that these failures are not often seen on the pins with the lowest HBM levels. The returns seen with EOS seem to depend more on the function of the pin on the application board.*

Q16 - In the early 1970s the 2 kV HBM level was discussed as a possible standard and by the 1980s it became the widely accepted level, so why would this not be relevant anymore?

*The 2 kV HBM target level was set when not much was understood about the ESD control methods. These have improved dramatically, as discussed in **Chapter 2**. At the same time, the assembly methods for the IC chips have undergone major changes as well. When basic ESD control elements are installed, HBM is no longer a risk for the devices in modern assembly lines.*

Q17 - If, according to some IC suppliers, they can deliver a cheaper more efficient ESD protection methodology, would it not make sense to keep the same levels as before?

*It does not matter what type of protection device is implemented. In the end, all are limited by the same physics as outlined in **Chapter 5**. The "target level" is not independent of the physics. Independent of the protection device implemented, if the HBM ESD target level is reduced, then the ESD layout area and impact on normal electrical performance may be similarly reduced. The problem is then to choose the appropriate HBM ESD target level. ESD over-design is inefficient and wasteful.*

Q18 - Does the modified HBM target level apply only to technologies of 45 nm and beyond?

*There is enough data to show that products from 180 nm and above were just as safe and that the design cycles were considerably affected even more than 5 years ago. Some of this information is given in **Chapter 3** and in **Chapter 4**. At 45 nm and 32 nm and below the problem of ESD cost will keep getting worse.*

Q19 - Is this modified HBM target level only limited to CMOS, or are they independent of the silicon technology?

*IC products in all different technologies may suffer from ESD over-design. Hence there is no reason to consider only CMOS products. The data in **Chapter 3** gives comprehensive information to illustrate that the same arguments apply independent of the silicon technology.*

Q20 - Is the Industry Council making these recommendations to save money for the supplier?

*The concept of "ESD Cost" applies to both suppliers and customers. The suppliers go through repeated testing, debugging, and design re-spins to meet the existing specified ESD requirements. Both customers and suppliers go through joint meetings to understand and negotiate solutions for improvements. These efforts delay the product delivery and can also have an impact on product circuit performance. The cost curves are discussed in **Chapter 7**.*

Q21 - What about multiple cumulative HBM events which are just below the controlled ESD levels? Is there a risk at these lower levels of higher field failure rate?"

No. There has never been any data that indicates repeated ESD events occur on the same device at any level.

Q22 – If the recommendations from this white paper are based on volume of products failing the 2 kV HBM target level, why were these shipped in the first place? What drove the customers to accept them?

The answer to this question is varied. In some cases the customers agreed to accept the devices based on the intention of the supplier to improve these levels at the next design cycle. But as large product volumes were shipped with the waived levels and no field returns were seen, both the customer and the supplier gained increased confidence that the 2 kV target level is more artificial than real. ***Chapter 4*** *documents several cases where, for products that were passing 1 kV a tremendous amount of resources had to be expended to meet the 2 kV level while these same products as reported in* ***Chapter 3*** *do not show any ESD returns but only insignificant unrelated EOS returns. The product and quality groups across the industry have had numerous similar experiences, and this became a driving reason for revising to more realistic ESD requirements.*

Q23 - Does the Council propose to make further reductions over the next five years?

The first objective of the Council is to get an industry wide acceptance for the proposed modified HBM ESD target level. As technologies progress even further, it is not unreasonable to expect that eventually the ESD protection responsibility will shift further away from the IC designers to much better static control throughout the manufacture and application of IC devices. This also would be consistent with industry focus shifting to System Level ESD performance over the coming years.

Chapter 1: Historical Perspective on HBM/MM ESD Requirements

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1.1 Motivation for the HBM Target Level

The early 1970s saw the first systematic measurements of HBM on people (e.g., H-P study) including people in moving chairs. A good summary of some of this early work on the human body model was published at the first EOS/ESD Symposium [1]. Workers in these early HBM studies found that even while wearing wrist straps, one could easily generate 1-2 kV HBM. Later in the 1970s and early 1980s, the automotive industry began instituting ESD pass levels, with Ford adopting the MM and 200 V, GM and Chrysler more focused on the HBM, and Chrysler specifying 2 kV HBM minimum after lengthy consideration of even higher voltages. Meanwhile, RCA TV division settled on 2 kV HBM and a specially devised "Kinescope" test model, but no one accepted the latter [2].

Following these kinds of requirements from customers, by the mid-1980s, semiconductor companies began to set internal HBM standards for components, and the 2 kV HBM specification became most common among them. Even at that time, CDM was recognized as a major cause of device failure, not necessarily predicted with HBM testing, so design turnaround from CDM testing was also sought.

Most of this early HBM testing was with various testers that were aligned with HBM as described by Mil Spec 883C, Method 3015.X. Workers who were active in the greatest improvements in that spec in the 1980s will remember 3015.4 through 3015.7 (the last being in 1989) in particular, where major changes in the waveform standard followed studies showing that the testers aligned to the earlier versions of 3015 produced widely differing failure voltages in semiconductor devices [3, 4]. Only after a short-circuit current waveform spec was introduced were the internal tester parasitics brought under control to an extent that allowed some consistency among testers aligned to 3015. All the while, 2 kV remained as a convenient target for a “passing” voltage. When the HBM test reached Method 3015.7 (1989), the tester waveforms were much improved, but at that point the US Military stopped revising the spec and further HBM spec development passed on to standards committees at the ESD Association and JEDEC.

1.2 What was the Motivation for Introducing Machine Model (MM)?

The reasons were:

- **A.** MM simulated the failures caused by an ungrounded soldering iron contacting a semiconductor pin lead.
- **B.** MM simulated field damage failures such as CDM at that time better than HBM did.
- **C.** The zero-ohm discharging resistance in the machine model results in a higher peak current than HBM test for the thermal damage, a lower voltage MM test can be done.

Reason A does not exist anymore due to the dramatic improvement of ESD controls in the advanced automated manufacturing. Reason B also does not exist anymore because the newer CDM test method reproduces these failures better than MM testing. As for reason C, the HBM test itself is not meaningful now because it does not correlate to overstress failures in the field (see **Chapter 3**).

MM has been used for many years to verify the ESD performance of semiconductor devices in Japan. Historically, the first MM ESD test was reported before 1977. Discharging inductance was not defined as it is now, and no discharging waveform was defined either. It was adopted as the Japanese standard, EIAJ IC-121-1982. Because of no discharging resistance and inductance, it was closer to a real metal to metal contact ESD than the existing HBM standard.

Several years later, a MM standard returned from the US with a discharging inductance and oscillating waveform. Since then the MM standard has not simulated metal to metal contact which is now simulated better by CDM. Because of these reasons JEITA dropped the MM standard and added it in the HBM standard as a reference in 1994 (EIAJ ED4701).

References

[1] W.M. King, "Dynamic waveform Characteristics of Personnel Electrostatic Discharge", EOS/ESD Symposium Proceedings, EOS-1, 78 (1979).

[2] L. Avery, private communication.

[3] D.L. Lin, M.S. Strauss, and T.L. Welsher, "On the Validity of ESD Threshold Data Obtained Using Commercial Human-Body Model Simulators", Proceedings of the 25th International Reliability Physics Symposium, 77 (1987).

[4] M.S. Strauss, D.L. Lin, and T.L. Welsher, "Variations in Failure Modes and Cumulative Effects Produced by Commercial Human-Body Model Simulators", EOS/ESD Symposium Proceedings, EOS-9, 59-63 (1987).

Chapter 2: Changes and Improvements in ESD and Control Environment

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2.1 Historic ESD Handling Procedures

ESD control programs have been in place for many years. One of the earliest programs involved the production of gunpowder. This simple program simply kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronics were not that sensitive to ESD events. The devices of the time could withstand most events without a problem. Even if they did fail for ESD events, the failures were a very small proportion of the overall failure rates.

In the late 1970s, with the introduction of large scale integration (LSI), ESD was noted as a problem. A group of industry experts realized that this was a problem and organized the first ESD Symposium in 1979 in the US. At the time, technical papers were exchanged and there were workshops on problems and solutions. Companies at this time also started to implement ESD control programs. Each company had their unique program and did not share the information. The need for standardized programs was not recognized at that time.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was Mil-STD-1686 released in May of 1980. This standard along with its companion handbook Mil-HBK-263 represented the first ESD control standard in the industry. All of the suppliers of electronics to the military were required to comply with this standard. However, most of the private sector still followed company developed procedures.

These early standards were focused on people and packaging. Controls in place for insulators were left mostly to the end user without much consideration except for the removal of non-required insulators. Tools, machines and automated equipment were not addressed or really considered as most of the processes were manual. The basic instructions were to keep everything and everyone at the same potential.

An additional issue with these first ESD control programs was that the materials that were used to control static electricity did not have standards to qualify the materials. This lead to many different types of testing, different methods and different instrumentation that caused different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a technical association, the ESD Association (ESDA) was formed to try to resolve some of the issues surrounding material testing. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces and flooring. The standards did create a way to compare one product with another product. Suppliers of these

materials were able to use the standards to improve the products to make them better. For example, the simple wrist strap has gone through many changes in the industry. What started out as a simple metal bead band has evolved into a system that makes better contact with a person and in some cases allows for continuous monitoring. They provide a much more reliable connection than before and last longer. The standards also provide a way to test the wrist straps in a consistent manner so that one that becomes defective can be removed and replaced. Before this, materials were used until they were physically damaged without regard to the electrical properties.

In the 1980s and 1990s the electronics manufacturing industry changed from each company having all the manufacturing reside within the company to a model that included many contract manufactures (CM) or electronic manufacturing suppliers (EMS). The military standard and the European standard, CECC 00 015:1991, became out of date. They were either too restrictive or did not address all aspects of a control program.

The ESDA in 1995 was given the task of replacing Mil-Std-1686 with an industry standard. The standard ANSI/ESD S20.20-1999 [1] was the replacement for ESD process control. Following this standard, a third party certification program was established to demonstrate compliance to the standard. Today, this standard has been updated and replaced by ANSI/ESD S20.20-2014. In parallel, the IEC updated IEC 61340-5-1 [8] to become technically equivalent to ANSI/ESD S20.20-2014. These standards when followed are written to safely handle 100 V Human Body Model devices. All of these standards have improved control materials, understanding and ESD control processes.

2.2 Global Implementation of ESD

Manufacturing of ESD sensitive products is currently performed in all parts of the globe. However, since the late 1990s there has been an ever increasing trend to move electronics production from high cost to low cost geographies.

Globally, there is a large difference in the types and levels of ESD programs that are in existence today. ESD control programs range from:

A. Little or no ESD control
B. Basic ESD controls
C. Detailed ESD control programs

The level of ESD controls is not strictly related to geography but in many cases is driven by customer requirement. There are many ways to establish an effective ESD control program. This leads to considerable differences in effective ESD program design and the controls that are ultimately used. However, every well established and maintained ESD control program is based on the following three fundamental principles:

- Ground and bond all conductors
- Control charges on insulators
- Use protective packaging for transit and storage

Let's look at each of these principles in more detail.

2.2.1 Ground and Bond all Conductors:

Maintaining ESD sensitive devices and every item that they come into contact with at the same electrical potential will ensure that ESD related events do not happen. This equi-potential situation can be achieved by attaching all of the conductors in the environment to ground (earth) or by bonding them together to maintain an equal potential. Conductors in this situation refers to people, working surfaces, ESD sensitive devices and any process related conductors and dissipative materials that come into contact with ESD sensitive devices. The grounding and bonding of conductors will minimize the chance of HBM and MM discharges from occurring.

2.2.2 Control Charges on Insulators:

Every good ESD control program will do the following:

1. Remove **unnecessary** process related insulators from the operations where ESD sensitive devices are handled.
2. Determine what constitutes an unacceptable electrostatic field on insulators that are required in the manufacturing / handling process (for details see ANSI/ESD S20.20).

Controlling charges on insulators will help to minimize the chance of CDM related ESD events from occurring.

2.2.3 Use Protective Packaging for Transit and Storage:

Finally, in order to ensure that ESD events do not occur between manufacturing process steps or during the shipment of ESD sensitive devices to other locations (customer or next processing facility) the devices should be packaged in ESD protective packaging. The adequate level of protection provided by the packaging can be achieved by different packaging systems and has to be defined by the responsible companies.

2.2.4 ESD Control Programs and Resulting Data:

A. Little or no ESD control

For the few companies that have not even implemented a basic ESD control program (this means little or no controls used and not verified on a consistent basis) it is very likely that these companies would not be able to handle ESD sensitive devices that have an ESD sensitivity of even 2000 V Human Body Model. Figure 1 shows the voltage on a person's body as they walk in a manufacturing environment that has no ESD floor or footwear. In this situation, the person could damage a device with an ESD HBM sensitivity of 2000 V.

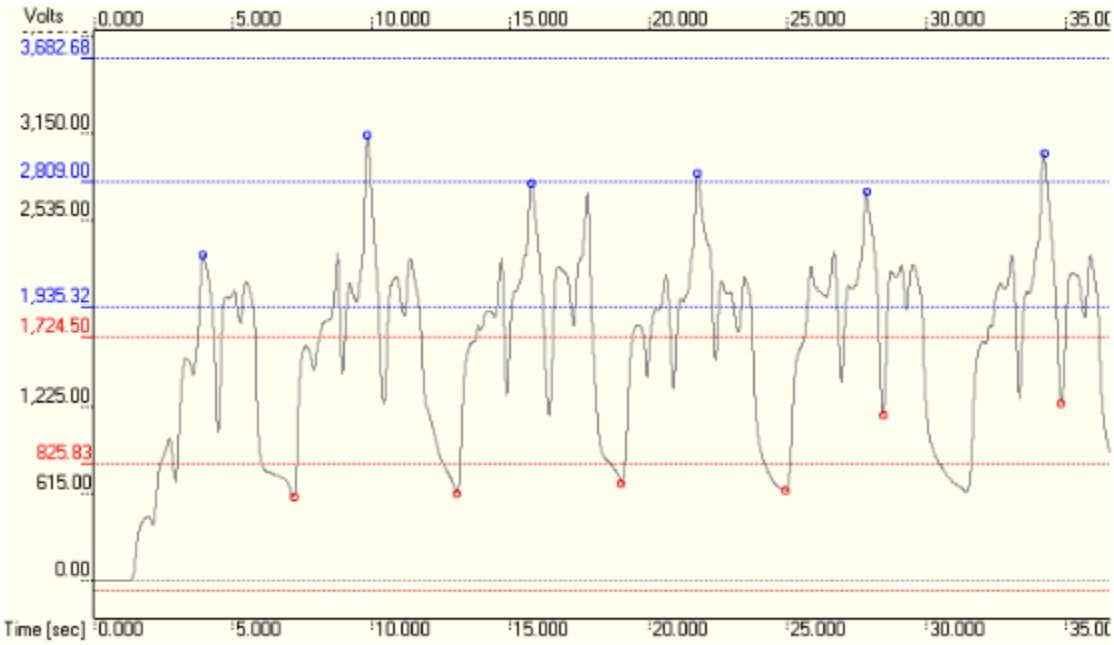

Figure 1: Voltage on a person's body when walking in a manufacturing environment without ESD floor or footwear.

B. Basic ESD Controls

Some companies have implemented a basic ESD control program. A basic ESD control has all the required control elements but no redundancies. The simplest ESD control program consists of personnel grounded with wrist straps, a grounded surface where ESD sensitive devices are handled and all static generating materials are removed and protective packaging for movement of ESD sensitive devices through the process. This type of program is often used by companies where:

A. The manufacturing operation is confined to a small area.
B. The number of employees handling ESD sensitive devices is small.
C. The value of the product is low.
D. The reliability of the products being produced is low.

However, simple does not mean that the program cannot be effective. A well-grounded wrist strap system will keep the voltage on personnel to less than 10 V. As long as the program is audited on a frequent basis this program can be every bit as effective as one where multiple ESD controls are utilized.

C. Detailed ESD Control Program

Finally, many companies utilize detailed ESD control programs to ensure that the devices that they handle will not be damaged. The use of constant monitors, ionization systems and ESD flooring and footwear can add a degree of redundancy and convenience to ESD programs where:

A. The devices are very ESD sensitive
B. The value of the finished product is high.
C. There is a large employee population with a high turnover rate.
D. The product has high reliability requirements.

All of these factors and more can drive the need for a more complex ESD control program to be implemented.

2.2.5 Advantage of Process Analysis

This example shows the difference between just implementing ESD control measures and doing a deeper ESD control process analysis. Figure 2 shows an example of a manufacturing location that had a conductive ESD flooring system installed. Unfortunately, the company did not make an effort to evaluate the ESD footwear system that was used for its employees. As you can see the voltage on personnel was well above the 100 V HBM threshold that the company had established for itself. The footwear used was chosen based solely on price. However even these shoes would provide adequate protection for a 500 V device.

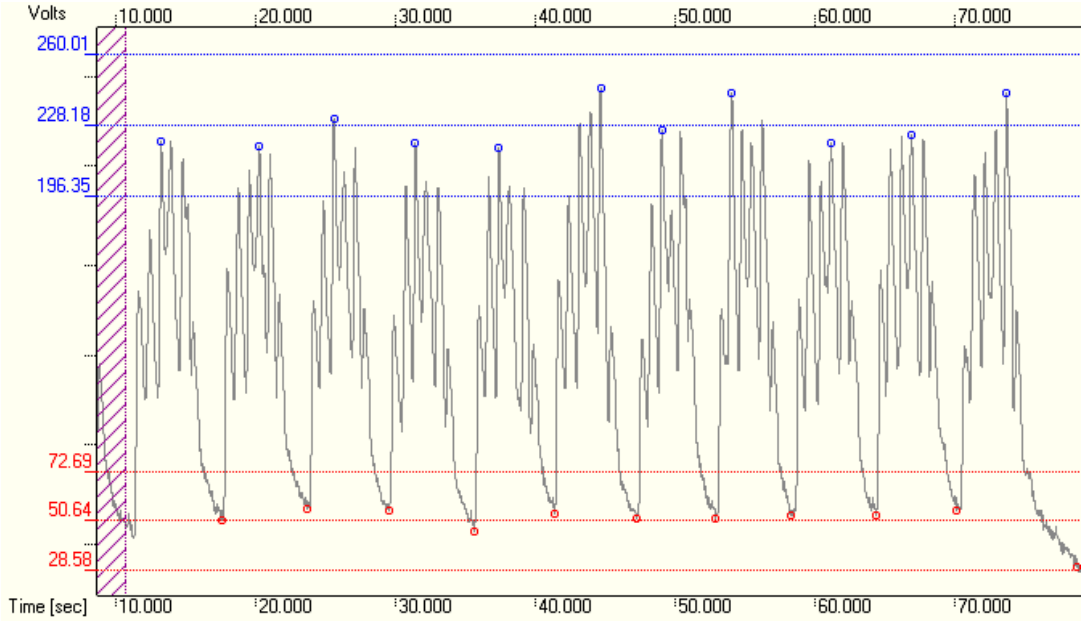

Figure 2: Voltage of a person in a manufacturing environment when a conductive ESD flooring system was installed (in comparison to Figure 1)

However, once the company understood the implications of their decision, properly selected footwear was implemented and the company was now able to safely meet their goal of handling 100 V HBM sensitive devices as shown in Figure 3.

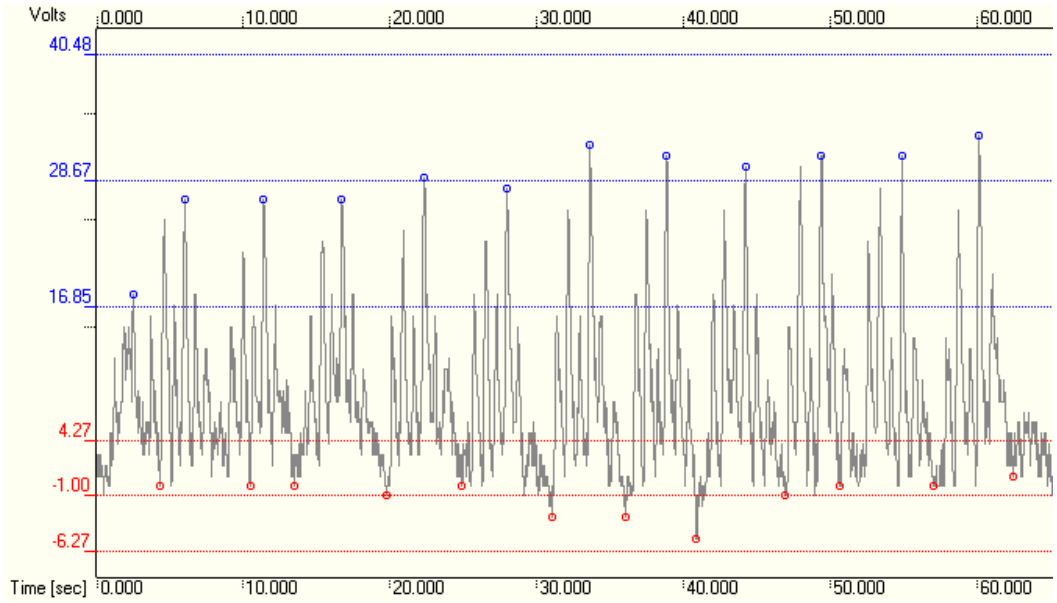

Figure 3: Voltage of a person in the same manufacturing facility / ESD flooring as Figure 2 but with properly selected ESD control footwear.

The other factor that can easily jeopardize an ESD program is infrequent verification that the ESD control elements are working. Most successful companies audit their ESD programs frequently to ensure that all of the control elements are functioning as intended.

Two good resources for establishing an ESD control program are through the implementation of ANSI/ESD S20.20 which is published by the ESD Association or IEC 61340-5-1. Both of these documents will provide the structure and guidance necessary to establish an ESD control program that can safely handle 100 V HBM sensitive devices and higher.

Conclusion:
By establishing an ESD control program and frequently verifying that the ESD controls are working as installed most companies can easily handle ESD sensitive devices with a sensitivity of 500 V HBM or higher. However, with slightly more attention to the selection of ESD control items a 100 V HBM program is easily attainable.

2.3 Change of HBM Hazard Scenario by Increasing the Automation Level

The complexity and automation level of printed circuit board (PCB) manufacturing has increased significantly in recent years. Years ago most devices used packaging with easily contactable pins, with pin counts being lower and pin-to-pin pitch relatively high. These devices were generally assembled manually by operators. In this environment there was the probability of human discharge to a single pin.

Modern packages today can contain up to thousands of I/O, and these I/O can be either pins on the package periphery, balls (as in BGA) or chip-scale packages. The I/O to I/O pitch has decreased dramatically to allow high pin count die to be packaged in a reasonable size. As a

result the packaged parts cannot be assembled manually, and the process is automated by non-human handling (grounded machines / tools / pick and place). Modern ESD control programs have evolved to become very effective in control in these types of handling environments, as discussed in Section 2.2. Therefore for automated assembly lines with modern, frequently audited ESD control programs, the risk of HBM or MM events is very low.

There will continue to be manufacturing areas, such as rework / optical inspection areas, usually smaller areas, where human contact with devices does happen. ESD control programs if effectively implemented and audited minimize the HBM / MM discharge risk in these areas.

This is also confirmed by literature, reporting that most of the ESD related field fails are due to CDM like stress and not due to HBM like stress [3].

References

[1] ANSI/ESD S20.20-2014; Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

[2] IEC 61340-5-1; Electrostatics – Part 5: Specification for the protection of electronic devices from electrostatic phenomena – Section 1: General requirements; 12.1998

[3] R. Gaertner; Do we expect ESD-failures in an EPA designed according to international standards? The need for a process related risk analysis; ESD Symposium 2007; Anaheim, CA, USA

Chapter 3: Consolidated Industry Data on HBM Levels vs. Field Returns

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Theo Smedes, NXP Semiconductors

This chapter discusses the relationship between the HBM qualification level of a product and the potential risk of failure related to that level when using the device. To this end a large set of data was collected for product shipped between 2000 and 2006 prior to the first release of WP1 in 2007. The next sections discuss the global findings from that database and present several case studies.

3.1 Field Return Rates versus HBM Level

A statistical comparison between number of shipped ICs achieving certain ESD qualification levels and their field return rate is given based on the consolidated data of the companies contributing to the Council (Figure 4). A total quantity of 21 billion parts was included in the statistics. 24% of the parts belonged to the 500 V pass/1000 V HBM fail category. 28% were passing levels between 1000 V and 1500 V. 4% had a robustness of less than 2000 V but higher than 1500 V. The remaining 44% met the 2 kV HBM level. The weakest pin combination determined the level of ESD robustness. Overall more than 600 qualified / released designs were considered, which were shipped in the years 2000 to 2006. Both designs with a lower ESD qualification level on a few pin combinations and designs with a reduced ESD robustness on many pins are included in the data. The IC designs considered belong to various application fields including communications, consumer, storage, automotive and discrete ICs. They were processed in several technologies ranging from a 1 µm node down to a 65 nm node. The assembly was done at a large number of sites located in America, Asia and Europe. All of them are running at least a basic ESD static control program as defined in Chapter 2.

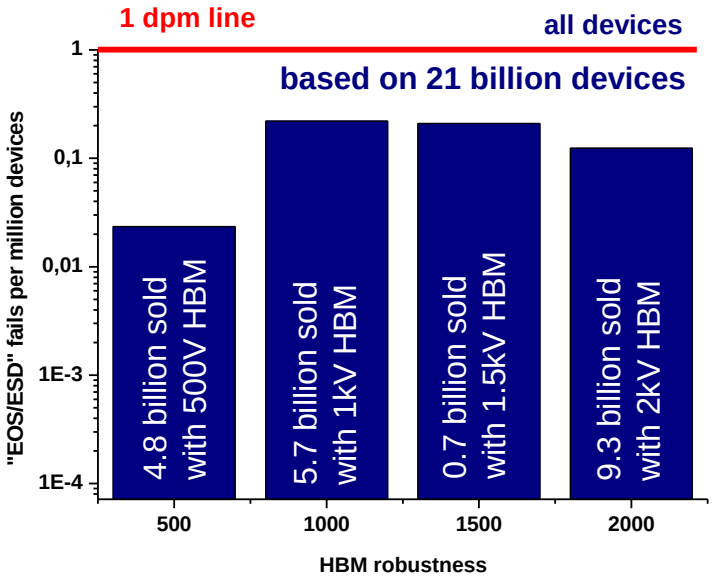

Figure 4: EOS/ESD fails returned to IC supplier versus the achieved HBM qualification level. A total number of nearly 21 Billion parts is considered.

The above EOS/ESD failure rate comprises all failed devices returned from in-house handling, board manufacturers' and OEM's analysed by failure analysis departments of many IC suppliers. It was included in the statistics if the root cause in the physical failure analysis report was given as 'ESD fail' or a fail due to 'ESD or EOS' (electrical overstress). This means the chart covers all kinds of possible electrically damaging mechanisms like discharge in the electrostatically protected environment, the discharge outside electrostatically protected areas and electrical overstress due to malfunction of the controlling board circuit.

Due to similar failure pictures and the missing information about stress conditions in the field a more detailed distinction between pure ESD events and EOS related fails cannot be made in this statistics.

However, even including EOS related fails the total return failure rate summed up over all ESD classes is below 0.1 defects per million (DPM). Clearly not all failing devices are returned to IC suppliers. Especially in cases of consumer ICs and other high volume, low cost products the effort for analysis is not often performed by the board manufacturer or the OEM. However, extracting just the data for automotive parts (where the awareness of defects is very high) provides the same distribution of EOS/ESD fails versus HBM qualification level as non-automotive parts (Figures 5 & 6). Both graphs prove that the fail rate due to electrical stress is independent of the achieved HBM level above a threshold of 500 V. It can be concluded that a qualification level of 500 V HBM is sufficient to safeguard against increased failure rate due to electrical damage.

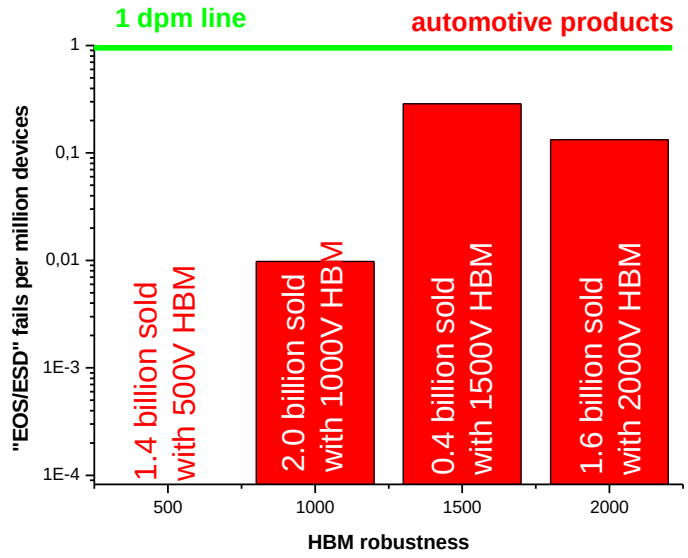

Figure 5: EOS/ESD fails of automotive ICs returned to IC supplier versus the achieved HBM qualification level. A total number of 5.5 Billion parts is considered.

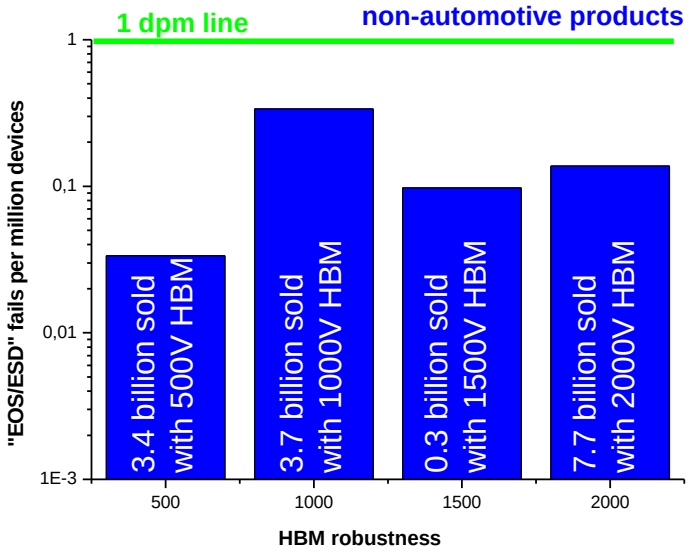

Figure 6: EOS/ESD fails of non-automotive ICs returned to IC supplier versus the achieved HBM qualification level. A total number of nearly 15 Billion parts is considered.

3.2 Case Studies

In the previous section the findings on the overall data, collected by the Council, were presented. It is not feasible to discuss each data point in detail. Therefore this section will highlight several interesting cases in more detail. Since these are case studies, each case is necessarily from a particular company, but examples of several companies of the Council are used. Also none of the cases by itself is evidence for the general conclusion. However, together they increase the confidence in the final conclusion.

3.2.1 Devices with Failure Levels below 500 V HBM

One company reports that they have 11 designs that fail between 100 V HBM and 200 V HBM. The die are produced in external foundries and in their own foundries, whereas contractors and their own assembly lines do the package assembly. In total over 4 million parts have been shipped without a single field return.

Another company has delivered several hundred thousand parts representing different ASIC designs, each failing between 100 V and 200 V HBM. In general, only a few pins limited the chip robustness level to these levels. No returns have been reported, despite the fact that several assembly companies were used.

Another example is given by a less than 500 V HBM part for a consumer electronics application. The device is produced in a 90 nm SOI technology, assembled by multiple low-cost Far East CMs. The low HBM levels were observed on approximately 10 out of 900 pins. 11 million parts were shipped with no customer returns for ESD. For a new version, the root cause of the lower failure levels was identified and improved. The redesign was qualified as a 1500 V part. Of this version, 3.8 million parts have been shipped to date, again with no customer returns for ESD.

An EPROM product in a relatively old and mature (early 1990s) technology showed handling problems. PPM levels are not known, but they were high enough to start an investigation. The failure mode could be reproduced by a HBM test, showing that the device was very weak (HBM robustness < 500 V) and would have needed detailed ESD control during assembly (see classification table). This control was not available at the time. After redesign the device reached an HBM level of 1500 V and did not show any further fails in the field.

Finally one company reported on a product that passed 400 V HBM and failed 500 V HBM on a limited number of pins. 16 million samples have been sold. In the past 3 years 1 incident caused above-average returns. This incident was traced to a problem in the assembly flow, unrelated to ESD, where it was subsequently eliminated. An improved design, meeting 2 kV, never showed problems, while 4 million samples have been sold of this version.

These cases illustrate that it is possible to handle even these extremely sensitive parts, if the necessary precautions are taken.

3.2.2 Devices that Fail between 500-1000 V HBM

A first example is given for a product that passes 500 V HBM, but fails 1000 V. The only returns that were received were traced back to system level stresses. The customer demanded a market

conform upgrade to 1000 V HBM. This was accomplished by a redesign. With the new design the same system level return rate was observed.

A second council company reports on 3 product types failing 1 kV HBM stresses. For one product the 1 kV level failed on all pins. For the other 2 designs only a few pins did not pass 1 kV. In total only 2 ESD complaints were reported. The first was due to system level qualification by the customer. The other showed damage on a pin that directly interfaces to the application. As far as known, this part was not deliberately stressed, but it is likely that this is also a case of system level damage. Neither of the ESD failures was on the lower HBM level pins. In addition, some clear EOS fails were reported. These occurred on random pins, not only on the pins with lower ESD qualification level.

3.2.3 Devices that Fail between 1000-2000 V HBM

A product failing 1 kV HBM / passing 1500 V HBM had a DPM level well below target. A deep analysis of the fails showed the following root causes: 58% of the fails had been due to EOS, 29% showed no problem, and only 1% of the fails were due to ESD. All EOS fails were traced to inappropriate use of the IC.

Several ASIC designs failing between 1000 V and 2000 V were reported. All products were accepted by the customers. Due to the relatively small sales numbers no ppm data is available. No ESD returns exist. For one product, failing 1200 V HBM, several EOS returns were received. All returns came from the same customer. This same customer also reported similar fails with a 2 kV HBM passing product.

Another company reported on two similar designs. One product passes 1500 V and fails 2000 V HBM. The other product passes 3000 V HBM. The products do not show significant reject rates, ppm levels are well below target. Also there is no significant difference between the reject rates of both products.

A microprocessor ICs was processed in 130 nm CMOS and an ESD robustness level of 1 kV HBM and 300 V CDM was achieved. For a shipped volume of 200,000 no field returns are known.

3.3 Conclusion

The conclusion is that ICs with 500 V HBM and above can safely be manufactured in existing IC and board manufacturing environments. This is an on average statement and can be invalid for single manufacturing sites where fundamental rules of ESD static control, as described in Chapter 2, are not obeyed.

Chapter 4: Impact of ESD Requirements from Customers and Suppliers

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Brett Carn, Intel Corporation
Larry Johnson, LSI

4.1 ESD Requirements and Specification Failures

With technology scaling and an ever increasing need for I/O performance, it is no surprise that during ESD qualification of processes, many ESD issues can come up. The failures most often may be related to only a few pins. The ESD failure debugging can take many weeks or even months of work involving ESD experts, product engineers, ESD test engineers, I/O design engineers and failure analysis engineers. Furthermore, participation from quality managers and customer interface engineers might be warranted in more urgent cases.

During this extensive analysis one usually finds that the original ESD failures may lead to more work if they are related to non-repeatable random events. Or, as in more recent cases, the tester-induced failures are not consistent with bench analysis, leading some to wonder if they are generated by the ESD tester itself.

During these product evaluation efforts a tremendous amount of time and cost is expended, but most important is the delay in time to market for the product. In most cases the analysis and the eventual improvement to meet the customer ESD requirement results in a product that is not any more reliable to the customer than it already was originally. This has been the experience of many IC suppliers.

4.2 Impact of "ESD Failures"

Both suppliers and customers are impacted by a result of ESD failures seen during the qualification process. Both supplier and customer automatically assume that an ESD failure generated by the ESD tester means failure certainty in the field. The data presented in this white paper does not support this assumption. Once ESD failure is seen a supplier may ask the following questions:

- Could these failures be replicated and are they consistent?
- Was the root cause confidently identified?
- Will any changes impact the product performance by impacting the pin capacitance? (See Chapter 5, Figure 18)

Answering these questions involves costs to both the supplier and the customer. By "cost" this is not only the expense of the additional mask / silicon wafer production, but also an additional slowdown in the product delivery to the market, and degradation in the expected circuit performance due to the added ESD protection. Additionally, both supplier and customer must engage in a series of discussions to resolve these issues and agree on a path of resolution.

Questions that must now be answered include:

- What data was used to evaluate and resolve target ESD specifications?
- Will there be a delay in product delivery?
- How many phone/face-to-face meetings will be necessary for satisfactory resolution?
- What additional delay may be experienced by the customers for qualification of re-designs?
- Will the reliability improvement gained justify the efforts; is there real risk in doing nothing?
- What will be the total impact on time to market for both supplier and customer?

Table I summarizes real life examples collected from companies for a few products that originally met a 1 kV ESD target level to illustrate these issues. Although in some cases there were no disruptions to the product sales, the effort involved meant cost to both suppliers and customers. In one extreme case, the product release was delayed by two years. The added cost to the customers comes from the meetings and negotiations that have to take place before the issue is settled as well as impact to the product launch. Also, even if a re-design is completed, there is no guarantee that the failure rate will be improved and that no random false failures, or even a new failure mode might occur. For these reasons, the cost of meeting the current specs at 2 kV HBM is continuously going up, accelerated by the technology scaling effects and increased pin count.

Table I: Selected Product Example Cycles for Meeting 2 kV

Product	Disruptions	Impact	Intro Delay	Number of joint ESD Meetings
P1	**No**	**Redesign**	**None**	**1**
P2	**Yes**	**Redesign**	**2 Years**	**10**
P3	**No**	**De-rate ESD**	**None**	**4**
P4	**Somewhat**	**Had to do minor redesigns**	**3 Months**	**>5**
P5	**No**	**No**	**None**	**>5**
P6	**Yes**	**Some delay**	**6 Months**	**19**
P7	**No**	**No**	**None**	**2**
P8	**Yes**	**Redesign**	**1 Year**	**>5**

These examples in Table I represent a snapshot of what routinely and typically occurs for products at each supplier company. Note the number of customer/supplier meetings that had to take place during the efforts to improve the product ESD from 1 kV to 2 kV.
Both customer and supplier now must take a look back and try and address the following:

1 - Were these efforts meaningful or justified?
2 - What other design focus was affected while concentrating on component level ESD and how have new product innovations been affected?

The data included in this white paper supports the conclusion of the Industry Council in regards to Question 1 in that the efforts to reach 2 kV HBM level are not justified. In regards to Question 2, this is difficult to quantitatively answer but clearly pulling resources off to focus on a non-risk item deters efforts to improve product performance in other areas.

Another example, in Figure 7, shows the work-months involved for eight products manufactured at two different technology nodes. All eight products were passing 1 kV and required by the customer to be redesigned to meet 2 kV. It can be seen that the analysis effort can range from 2 to 15 work-months. Consolidated Industry Council data shows that the average ESD re-spin causes >7 work-month effort. Since qualification times add additional delay, the total product delay can be as much as 12 months time to market.

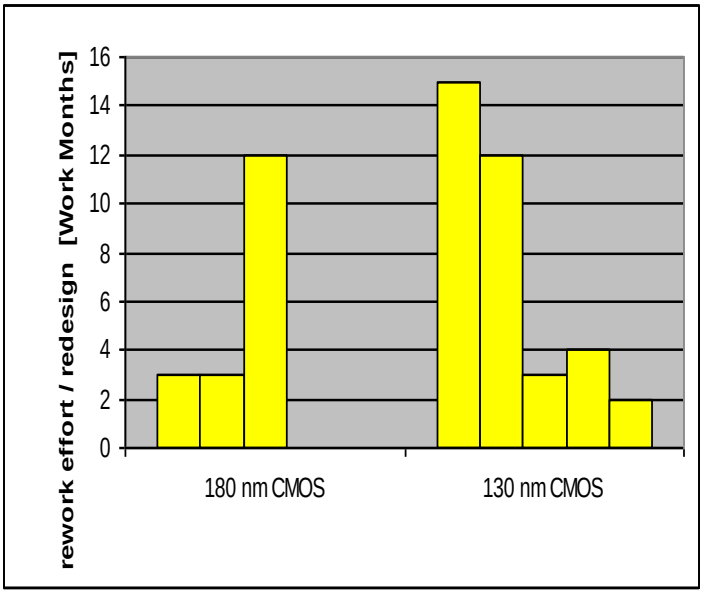

Figure 7: Actual example of ESD redesign efforts needed to meet 2 kV on devices meeting 1 kV.

4.3 Impact of a Revised ESD Target Level

Revision of the component HBM target level to a safe level of 1 kV would provide several benefits for both the customer and the supplier:

- Elimination of design re-spins for HBM performance between 1 kV and 2 kV and shorter time to market
  - For example, as much as 12 months can be saved as learned from case studies
- IO area savings to accommodate circuit requirements
  - For example, some calculations have shown as much as 43% reduction for advanced circuits with low leakage and high performance demands
  - Similar reductions would also apply to analog circuits
- Capacitance savings to help achieve faster circuits
  - For example, at 45 nm and 32 nm technologies 16-18 Gbit/sec cannot be met with 2 kV designs but can be accommodated with 1 kV or less requirement
- Short term gains would obviously be faster release of products for production and more focus on next generation technology ESD development and I/O performance
- Long term gains would be better customer relations and more opportunity for innovation of protection methods for the more relevant system level ESD

Chapter 5: IC Technology Scaling Effects on Component Level ESD

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Robert Gauthier, IBM

5.1 Scaling Effects on ESD Robustness

Advances in integrated circuit (IC) technologies which were achieved for circuit performance and overall reliability requirements have had a major impact on the intrinsic ESD design [1]. This is not surprising since the silicon scaling effects to increase circuit speed with shorter channel lengths or thinner gate oxides will lead to transistors that are much more sensitive to ESD and will result in lower failure current (It2). At each new technology node, new adverse effects are noted. Table II lists these technology trends and ESD impact starting in the early 80s to the present time period.

During the early technology applications, the transistor scaling involved increased current density (J) which led to higher dissipation J.E (where E is the electric field) and thus lower ESD levels. The next major change involved lowering E to improve channel hot carrier reliability which subsequently increased the power density (and decreased the bipolar efficiency) for NMOS NPN bipolar operation and thus again reduced ESD. This was rapidly followed by introduction of silicided source/drain diffusions that led to current crowding effects and even poorer bipolar efficiency. In addition to the silicide effects, the implementation of lower substrate resistance with epi to reduce latch-up effects caused another problem for the ESD design, especially using SCR type of clamps. However, when the epi was replaced by bulk substrates for cost effectiveness, this led to yet another unexpected problem – parasitic bipolar interactions at the IO areas and in the internal circuits.

TABLE II: Technology Scaling Impact on ESD

Feature Size	Process Advance	Impact on ESD	Factor(s) degrading intrinsic ESD performance
3 um	Junction Scaling	NPN Robustness	Current Density
2 um	Graded Junction	NPN Robustness	Power Dissipation
1 um	Silicides & Epi Substrates	NPN Robustness	Ballasting Effects and Avalanche Process
0.5 um	STI	SCR Trigger	Decreased Parasitic Bipolar Efficiency
0.35 um	Bulk Substrate	Parasitic Interactions	Increased Bipolar Effects
0.18 um	Shorter Channel Lengths	Lower It2	Localized Heating
0.090 um	Ultra-Thin Gate Oxides	Lower CDM	Ineffective Clamps
0.065 um	Thinner Metal Layers	Lower HBM, MM and CDM	Metal Heating
0.045 um	Insulating Substrates	Low Overall ESD	Increased Power Dissipation

As the technologies entered the nanometer range, the ESD sensitivity began to get much worse as much thinner gate oxides and thinner metal interconnects [1, 2] were both introduced to improve circuit speed. The thinner oxides result in lower CDM performance and the thinner metals cause heating effects with increased resistance in the ESD connections, making it difficult to keep the potentials at the IO pad low enough to meet both HBM and CDM protection requirements. Figure 8 shows that for technologies starting around 130 nm the failure current density of the ESD metal interconnect reduces with the effect becoming significantly worse as technologies shrink to 65 nm and below. The metal bus resistance per square is increasing which is also decreasing the electromigration reliability margin. This means that supply / ground bus routing will play an even more critical role in ESD design.

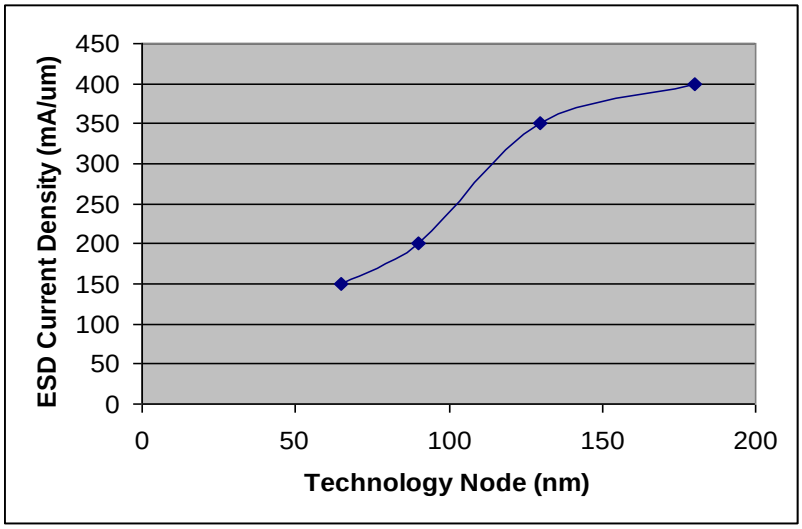

Figure 8: Metal ESD failure current density as a function of technology node.

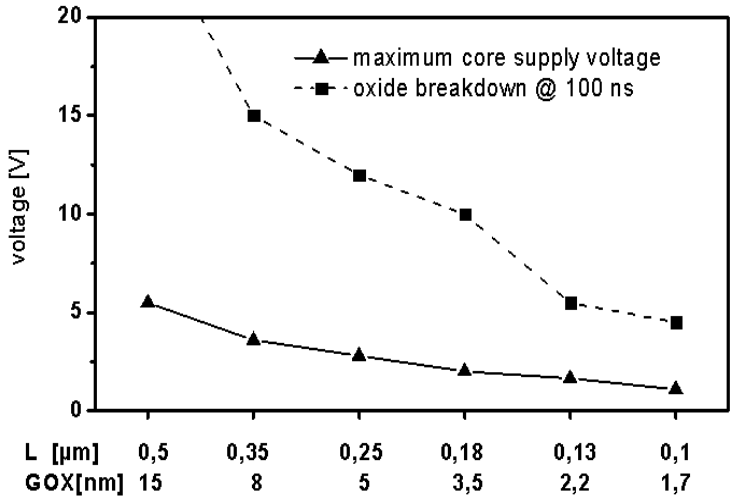

Figure 9: ESD regime oxide breakdown voltage and core supply voltage as a function of scaling

In Figure 9 the core Vdd supply voltage is shown as function of the technology node scaling for feature size transistor length and gate oxide thickness. Also shown in the figure is the simultaneous reduction of the gate oxide breakdown voltage under ESD like conditions. At the 100 nm node the gate oxide breakdown approaches 5 V for HBM stress. This means that any protection clamp at the IO has to keep below 5 V for 1.3 A or 2 kV HBM. With the metal resistance and current density limitations as discussed in Figure 8, the design to meet 2 kV becomes challenging and will even become impossible with further scaling.

Another new trend is the "Reverse Poly Effect" where the It2 values unexpectedly decrease with decreasing poly lengths [1]. Two different explanations are offered: 1) a decrease in the volume available for heating [3] and bipolar effect coming from merging of the pocket implants [4]. Combined with the local heating for reduced channel lengths, the introduction of SOI can lead to heating at the channel surface so much so that even gated diodes can have relatively lower failure current performance. In addition to SOI now the emerging technologies with multi gate (MuGFET) transistors, also called FinFET devices, have already indicated extremely low It2 and much more complexity to process effects [5]. A cross-section of the FinFET is shown in Figure 10.

Figure 10: Cross-section of an advanced FinFET.

The It2 data from [5] for the NMOS FinFET is shown in Figure 11. Note that although the device triggers as a parasitic NPN the failure current for the device (with an effective width of 50 um) is less than even 1 mA/um. This suggests that an understanding of the device heating under ESD conditions is required and that the methods to improve the It2 with layout and device structural changes need to be understood [6].

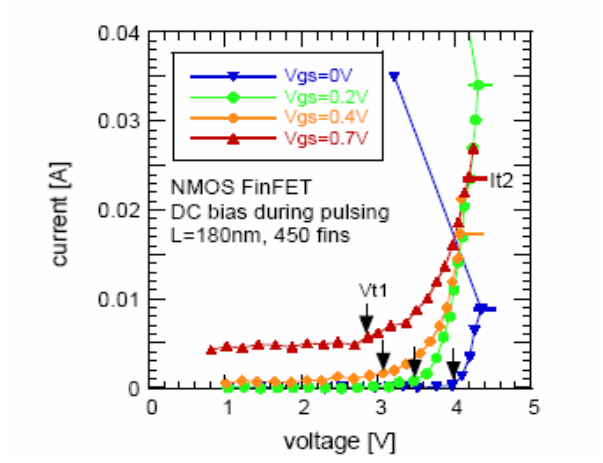

Figure 11: Ids-Vds curves for varying gate bias with trigger voltages (Vt1) and failure currents (It2) shown for a FinFET device structure [5].

The next major scaling effect on ESD is the use of ultra-thin oxides in the range of 20 Angstroms which were first introduced at the 130 nm/90 nm technology nodes. At such low oxide thickness the commonly used silicide blocking is not an option, since the increased on-resistance with contact to gate spacing itself will increase the drain potential during bipolar turn on to breakdown the oxide [7]. Even more severe is the oxide breakdown voltage which is in the 4-5 V range for thin oxides in 90 nm and below technology nodes making it very difficult to design for HBM let alone CDM protection. The statistical nature of the oxide breakdown mechanism is well known to be a very complex topic for time dependent dielectric reliability (TDDB), but the TDDB extension to the ESD regime is taking ESD design to the next level of challenges. As described recently in [8] the ESD regime oxide breakdown varies with process variations thus making it somewhat unpredictable to design for a given CDM spec. There are other issues with technology scaling that have not yet been investigated in detail for their impact on ESD. These include the upcoming strained silicon and the elevated source drain junctions and introduction of metal gates and high-K dielectrics. It is clear that the newer advances in transistor scaling will continue to have an impact on the ESD sensitivity up to a point that a completely new direction to the ESD protection strategy may have to be explored.

5.2 Protection Design Window

The ESD protection design has undergone several changes in strategy according to the technology scaling effects described in Section 5.1. Whereas the field oxide devices (FOD) in the early 80s, and the NMOS and breakdown SCR devices in the 90s have been extensively used, the current technologies make them difficult for practical implementation leaving only diode clamps and diode-triggered SCRs as mostly the available options.

A typical diode and rail clamp based protection concept is shown in Figure 12. Note that the entire protection performance critically depends on the on-resistance of the diodes, the VDD and VSS bus resistance values, and the efficiency of the Rail Clamp. This is indeed where the ESD Design Window is facing its constrictions [9]. The diodes sizes cannot be too large to minimize capacitance at the pad, while metal interconnects (which are becoming large component of the capacitive loading) at the diodes has to have minimum resistance to keep the pad voltage to a minimum for the ESD current flow in the range of 1-2 A HBM and 12-15 A CDM for very large package devices.

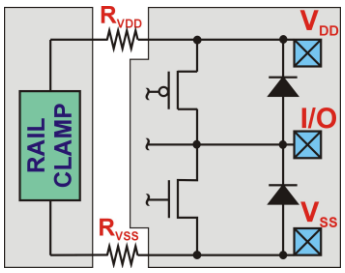

Figure 12: Common Diode with rail clamp based IO protection strategy.

Even for standard digital IO designs the voltage buildup at the pads during an ESD discharge can damage the input gate oxide or the output drain junction, especially if the output transistor has

low It2. This can lead to disappearance of the ESD Design Window as reported in [9]. It should be noted, however, that the relative margin for window is dependent on the choice of the protection clamp design. To illustrate the point, Figure 13 shows the design restriction for the common dual-diode protection device represented in Figure 12. As the technology is scaled the design for 2 A might vanish at the 65 nm node. Or, for 1.3 A (2 kV HBM), the window is reduced by 45%. No matter which clamp technique is employed, further technology scaling will further decrease the ESD protection window.

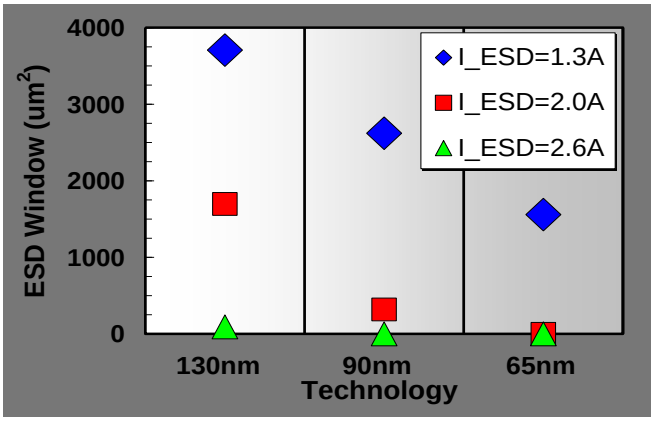

Figure 13: ESD Design Window Scaling [9].

These effects are even more severe for designs involving high speed SERDES (HSS) macros or RF low-noise amplifier (LNA) circuit applications. The design window severity comes from the constraints shown in Figure 14. Obviously the protection design must not only not interfere with the operating voltage, it must also have low enough on-resistance to protect the input gate oxide. The thermal failures from the top come mostly due to the metal heating in the advanced technology devices. As the window closes the challenge to meet 2 kV HBM or 500 V CDM becomes increasingly difficult.

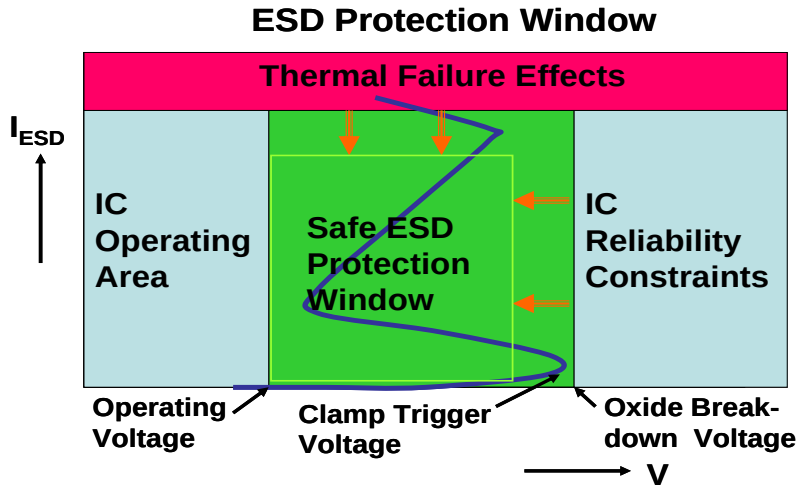

Figure 14: Technology Scaling Effect on ESD design.

To summarize, the severe restrictions on ESD design are coming from:

- ***Heating of the interconnect***
- ***Low breakdown of the gate oxides***
- ***Reduced failure currents of the advanced transistors***
- ***Lower operating voltages for the circuits***
- ***Very low tolerance to additional capacitance from ESD protection circuits***

5.3 ESD Capacitive Loading Requirements

As radio frequency (RF) application data rates and frequencies continue to increase in each new technology generation there is increased pressure to reduce the capacitive loading and improve the quality factor (Q-factor) of ESD devices. Quality factor is defined as the ratio of the reactance in Ohms divided by the resistance in Ohms. In a series RLC Circuit, $Q = 1/R * (L/C)^{0.5}$, where R, L and C are the resistance, inductance and capacitance of the tuned circuit, respectively. For example, in a parallel RLC circuit, Q is equal to the reciprocal of the above expression. Figure 15 shows a generic example of the general trend of ESD HBM levels vs. I/O operating frequencies. The operating frequency increase is due to the technology scaling and performance increasing as technologies continue to scale. In the labeled region 1 in Figure 15, the combination of chip level bussing resistance and power clamp resistance dominates the I/O signal pad clamping voltage thus the signal pad ESD protection as it is scaled larger (more capacitive loading) has a minimal effect on the overall signal pad voltage during an ESD event. In region 2 in Figure 15 the signal pad ESD protection network is scaled to reduce capacitive loading and in this region the ESD protection device itself dominates the signal pad voltage during an ESD event.

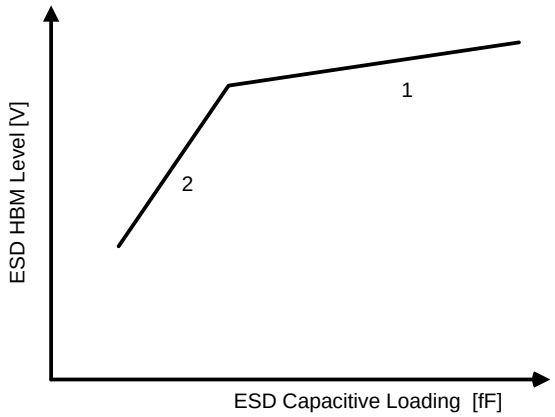

Figure 15: Generic plot of ESD HBM Level vs. ESD Capacitive Loading

Figure 16 shows a double diode based ESD protection strategy with the first and last stage of a bi-direction digital I/O receiver and driver respectively as a sample schematic for further discussion purposes. Included in the simplified schematic are the Vdd and Gnd bussing resistances, the power supply ESD clamp and the power supply effective decoupling capacitance. For a double diode based ESD protection strategy, one of the typically used power supply clamps is the RC-triggered MOSFET clamp. For calculating the IO pad voltage during an ESD event,

the power supply resistance of the discharge path and the voltage drop across the power supply clamp can be equally important as the voltage drop across the IO pad's ESD protection devices. In Figure 16, secondary CDM clamps using double diodes are shown but various types of CDM devices (SCRs, non-silicided NFETs for example) could be used rather than diodes. Figure 17 shows a similar simplified schematic as in Figure 16 except the HBM double diodes have been removed and a diode-string triggered SCR (DTSCR) is inserted [11].

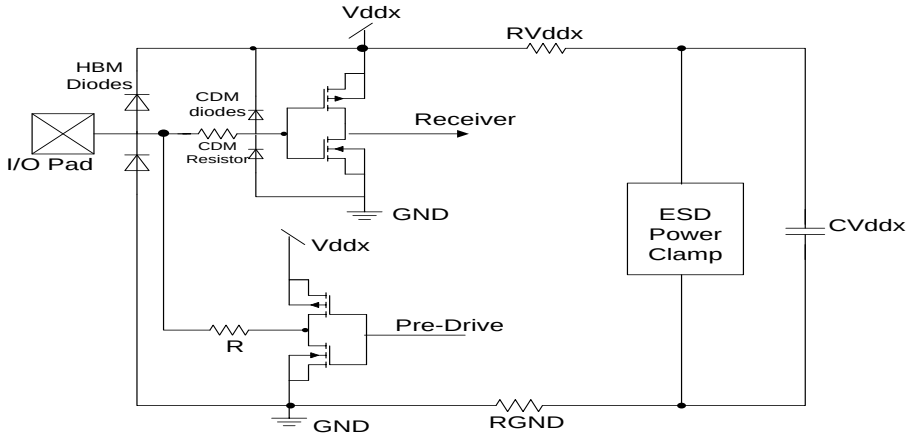

Figure 16: Double Diode based with RC-triggered Rail Clamp ESD Protection Strategy

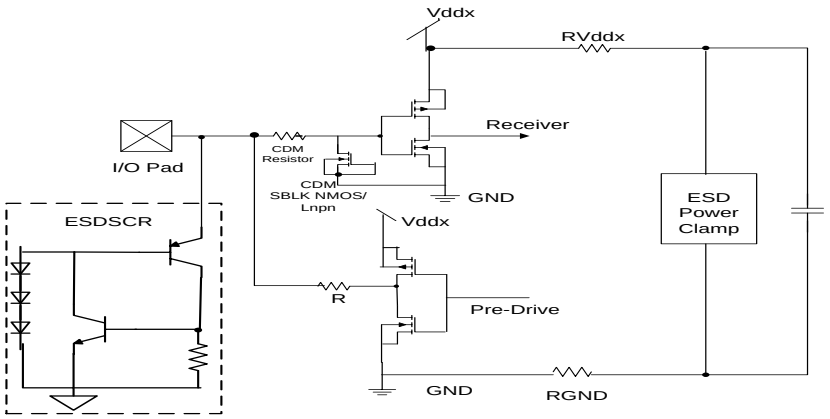

Figure 17: Diode String Triggered SCR (DTSR) with RC-triggered Rail Clamp ESD Protection Strategy

Figure 18 shows a specific example of the allocated capacitive loading budget for a high speed serial link (HSS, also referred to as a SERDES Core) where it is assumed in parallel to the ESD capacitive loading there are cancellation types of networks (such as t-coil) that cancel out approximately half the ESD capacitive loading. Figure 18 is just one sample showing the capacitive loading of the ESD device scaling; the specific results for a given technology may vary. However, the general trend is reduced capacitance loading budget for the high speed I/O.

Also in Figure 18, the calculated ESD results for diode and SCR based ESD protection (see Figure 17) concepts are added to the previous curve. As can be seen from the left hand y-axis in

Figure 18, as data rates go from 6 Gbits/sec to 12 Gbits/sec the ESD capacitive loading budget decreases from approximately 300 fF down to 150 fF. In the right hand y-axis in Figure 18 the calculated HBM ESD results are shown. The calculations use high current TLP (transmission line pulse, energy equivalent to HBM) data from a 65 nm technology and compare both diode based ESD protection with RC-triggered power supply rail clamps and diode string triggered SCRs (DTSCR) with RC-triggered power supply rail clamps. In the comparison the worst case HBM robustness is shown vs. capacitive loading requirements for both types of ESD protection. The diode-based and DTSCR-based ESD protection networks are two of the most commonly ESD protection networks used for RF applications. Machine model results exhibit similar trends to HBM.

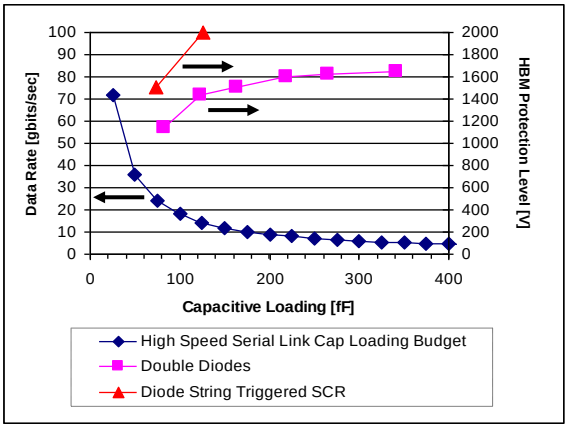

Figure 18: High Speed Serial Link Data Rates and HBM Protection levels vs. Capacitive Loading requirements

The ESD boundary conditions used to create Figure 18 are listed in Table III for reference. The capacitance values for the ESD devices include both FEOL and BEOL capacitances extracted using an extraction tool from actual ESD devices designed in a 65 nm technology node.

Table III: Assumptions used in calculations

Signal Pad ESD Protection Device	Signal Pad ESD device on-resistance	RC Clamp turn-on voltage [V]	RC Clamp on-resistance [ohms]	Decap on Vdd [fF]	Rvdd [ohms]	Rgnd [ohms]	Max Pad Voltage allowed [V]
Double Diode	**Varies with capacitive loading**	**0.5**	**0.5**	**0**	**1.0**	**0.5**	**4.0**
DTSCR	**“ “**	**0.5**	**0.5**	**0**	**1.0**	**0.5**	**4.0**

5.4 Package Effects

Package advances are based on requirements of the different market segments. Generally the packaging of a particular die in a package, given the same pins are bonded out for different packages, has little effect on HBM ESD performance. However, the variation of package size, bond wire inductance, etc., does cause a variation in CDM performance for the same die packaged in different packages. This development of package types from dual-in-line (DIP) to multi-chip modules (MCM) and from there to flip-chips and stacked die would surely determine the achievable ESD performance for CDM since during this stress mode the package capacitance plays a very dominant role. The original DIP packages have pins that are readily exposed to handling making them sensitive to HBM, but modern packages such as the ball grid array (BGA) have pins that are embedded as well as are closely spaced, making them much less vulnerable, and in fact may be impossible, to HBM stress. Thus, CDM plays the critical role for the overall ESD reliability. The critical issues for CDM and the relevant level for safe manufacturing will be addressed in a subsequent white paper.

5.5 ESD Technology Roadmap

The roadmaps for ESD [12] project severe restrictions on the achievable HBM ESD levels as shown in Figure 19. What should be noted from Figure 19 is how low HBM levels are and will project to. Constraints from circuit designs such as RF could eventually reduce the practical ESD HBM design levels into the 100 V range. Similarly, the CDM level (Figure 20) may get reduced to the 50 V range. Note that a MM roadmap does not make sense as this is reflected in the HBM roadmap.

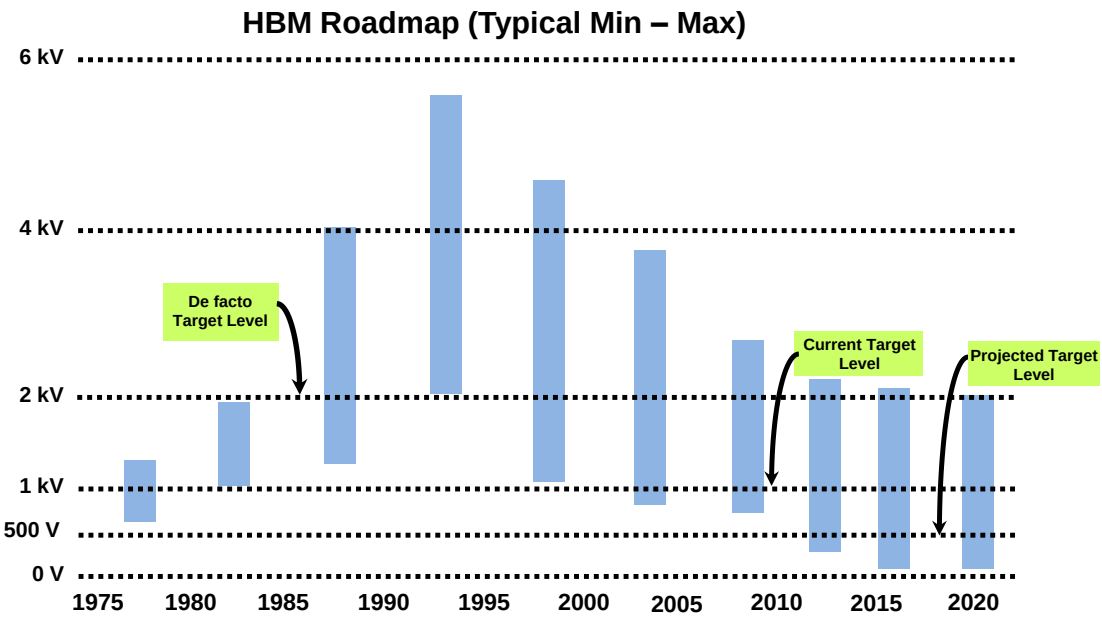

Figure 19 — ESD Roadmap for HBM [12]

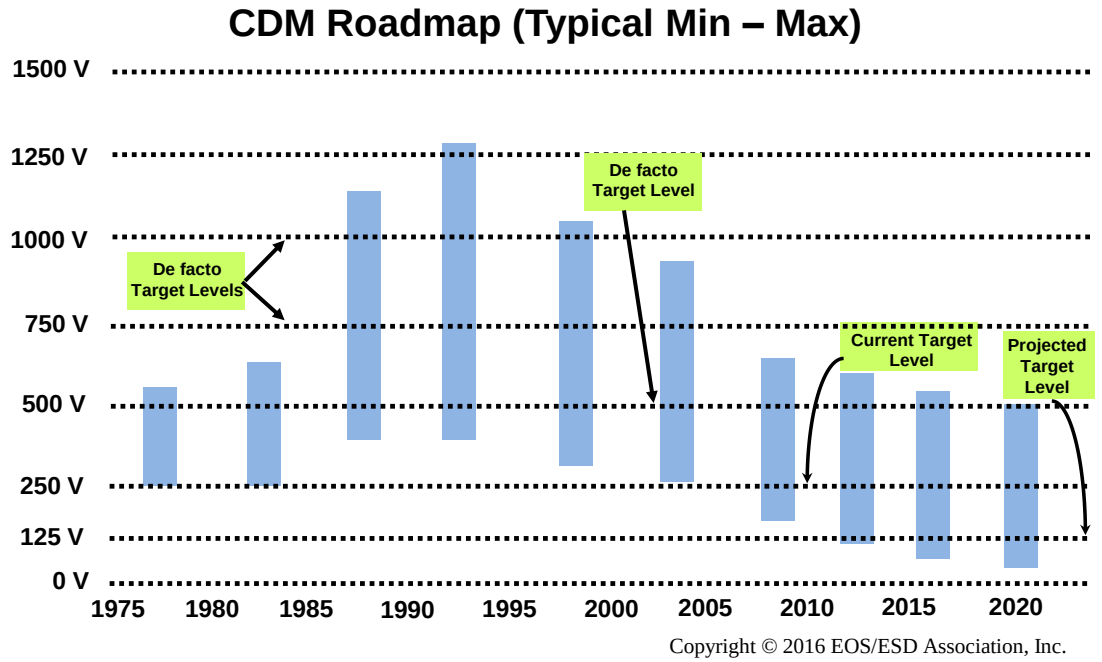

Figure 20 — ESD Roadmap for CDM [12]

These trends above will only mean that ESD control in the production areas will become absolutely necessary. Fortunately, the trends towards packages with very close pin spacings and

the much reduced incidences of human handling would certainly alleviate this threat for HBM. However, CDM ESD control, which is dependent on the package structure, needs to be carefully considered as the protection levels would drop with technology scaling. CDM control at the factory should be critically improved.

5.6 Discussion

This chapter addressed the scaling of IC technologies and the corresponding increased sensitivity of the IC chips to ESD. What has become clear is that the view and strategy of ESD has to be changed. Throughout the electronics industry there have been questions on the validity of the 2 kV HBM requirement given the much better factory controls combined with other factors. There are also questions on how the real world CDM discharge events can be more accurately represented with improved CDM tests, especially for large packages. ESD will continue to be a major reliability issue and some reasonable protection can be achieved as long as the nature of the threat is more realistically represented. An important objective should be to consider appropriate modification of the ESD target requirements enabling designs to meet the design performance objectives, while maintaining a safe HBM ESD target level that represent today's realistic component ESD environments. Meanwhile, more attention should be paid to the more obvious threats from System IEC, CDE, and TLU as outlined in the ESD Association White Paper [13].

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Chapter 6: Differences between Component ESD and System Level ESD

Harald Gossner, Infineon

6.1 The History of System Level ESD

System level ESD tests have their origins back in the 1960s. It was noticed that when people sitting in chairs with castors bumped into a mainframe computer system, the system would have to be reset or unexpected results would occur. As a precaution, mainframe designers developed ESD tools which would simulate this waveform and subjected operating machines to these events. As long as the machine was able to continue to operate, the test was considered successful.
This test was designed to generate noise on the signal line and power planes to ensure that the machine could continue to operate. It was not designed as a destructive test. How the machine handled the noise was resolved in many ways, from system packaging (from circuit board layout to cover design), system architecture (can a system recover from an unexpected signal) to signal to noise ratio tolerance.
As this standard has evolved into IEC 61000-4-2, it has also been extended to more than just mainframe systems. More equipment is now being subjected to this standard including notebook computers, gaming systems and mobile phones. While the standard does not require discharge to connector pins, there have been many system level designs that still allowed sensitive devices to exist without problems.

6.2 Differences in Component and System Level ESD Stress Models

Standardized **component level ESD stress test routines** are defined for the qualification of packaged ICs. The tests are designed to reproduce failure signatures observed in the IC component manufacturing environment. **All pins of an IC are stressed** in a large number of stress combinations during these tests. The IC is not powered when the ESD stress is applied. Passing these levels in the qualification is intended to ensure safe manufacturing of the IC in an ESD protected area of an IC manufacturing sites.

System level ESD strongly differs from component level ESD both in testing and resulting failure mechanisms. Both the stress model and the circuit ESD path environment are different between component and system level models. There is no strict correlation between IC level ESD robustness and system level ESD robustness. The procedure for system level ESD testing is described by the IEC 61000-4-2 standard [1].

The system level ESD stress event, which the system level protection has to be designed for, is an ESD discharge to an external interface pin of a complete electronic system which is touched or operated by the end-user or during the component replacement outside an ESD protected area. Electro-statically, the environment is uncontrolled and charging levels beyond 10 kV are possible. The waveform of the discharges varies over a wide range of pulse duration and currents. For testing complete systems a very flexible system-dependent set-up is required. This is realized,

for example, as a desk top placement of the system under test and application of the stress pulse by an ESD gun. This method simply cannot be extended to a stand-alone IC test. In general it is not clear which part of the discharge current applied to the system is reaching the IC. It is also known that EMI (radiated emissions) can result from the system level ESD tests which cause unique failures not captured by component level ESD tests.

Apart from this, the testing conditions of a system require the discharge both while the system is powered and without a connection to a supply. Due to this, both functional and destructive system ESD test failures have to be considered differently in comparison to IC component level ESD test failures. For example, in the case of triggering an IC latch-up event, functional fails might not lead to a physical failure signature and vanish as soon as the system is reset. Destructive fails often show a larger failure picture compared to component level ESD failures during testing due to higher pulse energy and possible subsequent dc stress in a powered system.

To determine the system level ESD robustness, an application board is required**, where only a few system relevant pins (e.g. pins attached to connectors) are connected to the discharge points and are stressed**. Currently a standardized set-up has been discussed which allows an evaluation of the system level related ESD robustness of an IC using appropriate application boards [2]. Typical target levels for system level ESD tests are 8 kV or 15 kV. The peak currents at these levels may range from 24 Amps to 45 Amps. A comparison of the test parameters is summarized in Table IV.

Table IV: Comparison of Component level ESD testing according to ANSI/ESDA/JEDEC JS-001 [3] (HBM) and system level ESD testing according to IEC 61000-4-2.

	Component level ESD test	**System level ESD Test**
Stressed pin group	Multitude of pin combinations	Few special pins
Supply	Non-powered	Powered & non-powered
Test methodology for 'HBM'	Standardized	Application specific using various discharge models
Test set-up	Commercial tester & sockets	Application specific board
Typical qualification goal	1 ...2 kV HBM	8 …15 kV
Corresponding peak current	0.65 … 1.3 A	> 20 A
Failure signature	Destructive	Functional or destructive

Obviously, pins exposed to system level ESD stress require quite a different protection concept than pins addressing component level ESD to sustain pulse energies orders of magnitude higher than component level ESD. The protection path is typically provided at the printed circuit board level (PCB) (e.g. by transient voltage suppression (TVS) diodes) as opposed to at the IC level. Both economic and technical reasons influence the choice of the approach and it usually differs

from application to application. If it is implemented on a PCB, it is required that the high current characteristic of the on-chip protection is compliant with the clamping behaviour of the PCB protection. The achievable system level stress fail level is related to the effective resistance of the on-chip current path. If resistance is too low in the voltage regime below the clamping voltage of the protection element on the PCB, the IC will inevitably be destroyed due to the extreme currents provided during the system level discharge. *It should be noted that replacing the RC network in a system level ESD test to match the component level HBM RC network does not make it equivalent to ANSI/ESDA/JEDEC JS-001*. Attempts to do this will not meet the requirements called out in ANSI/ESDA/JEDEC JS-001

6.3 Case Studies

To highlight the fact that there is no direct correlation between system level ESD (IEC) and HBM component level ESD, various case studies are presented. Both cases of products with low HBM ESD qualification levels, perfectly passing IEC tests and cases of products with 2 kV HBM and high CDM and MM qualification levels failing the IEC test are known. The examples show that the assumption that high component level HBM leads to high system level ESD is too simplistic. This does not mean that HBM robustness tests are useless for assessment of the system robustness. However, it has to be applied as pin-specific testing method and has to be accomplished by a high current IV characterization [4]. The standard HBM qualification testing addresses completely different failure mechanisms and can only lead to misinterpretation if compared to system level performance.

A DSP IC processed in a 90 nm technology had several pins passing only 500 V or 1 kV HBM. This IC also passed the IEC system level ESD tests conducted by the customer. The satisfactory IEC system ESD test has improved customer confidence that this DSP is production worthy even if the HBM level is lower.

One product designed in 130 nm technology had 35% of the pins passing below <500 V HBM. It had no handling issues and additionally it passed 8 kV IEC (contact method) test by the customer.

Two different IC designs, both with 2000 V component level HBM pass level, showed customer returns. Neither HBM, nor MM nor CDM could reproduce the failure signature. System level ESD testing showed the same failure signature as found in the customer returns. The device degradation already occurred at 50 V IEC pulse stress [5].

One IC processed in 0.35 µm technology passed 1.5 kV HBM at first silicon. The required IEC 61000-4-2 level was achieved at first silicon on the pins exhibiting 1.5 kV HBM. After a redesign, the same pins showed an improved 2 kV HBM level in the component level testing but failed the previously passed IEC level. As explained above, even when the ESD robustness of the modified on-chip ESD protection was improved, the I-V characteristics of the on chip ESD protection were no better at shunting additional current to the external, PCB protection element.

6.4 Conclusion

To achieve high system level ESD protection it is not sufficient to design for high component level HBM ESD values. In a number of cases, this assumption has been proven to be misleading and caused problems. Sufficient system level ESD protection requires a dedicated, pin specific protection development scheme. In many cases, joint design efforts between the IC and printed circuit board (PCB) protection circuitry or at least an adequate IV behaviour of the on-chip protection structure and modelling is required to enable optimization of the protection at the PCB level.

In general**,** system level ESD as well as similar pin specific system discharges like cable discharge (CDE) is considered as the more critical threat for electronic systems [6,7]. Recently, significant effort has been made to address this on the level of IC design and testing [8-12]. However, these are only the first steps done. It is recommended by the Council that IC suppliers and their customers focus on this topic in the future. System level ESD protection is the technical challenge in the field of ESD protection of electronic systems with proven relevance for application at the end customer.

References

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Chapter 7: Recommendations for a New ESD Target Level

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7.1 New Realistic Target Level for HBM

The preceding chapters have discussed the impact of a component level HBM withstand voltage on the capability to manufacture ICs without yield loss and reliability concerns. It has been shown that, for over 20 billion parts shipped by various Council companies, the field return rate was independent of the HBM qualification pass level of the ICs ranging from 500 V to 2 kV. This database includes more than 600 designs covering communication ICs, consumer ICs, discretes, memory products and automotive ICs that have been manufactured and placed onto PCBs at a large number of different sites worldwide over the last 5 years. Therefore the conclusion has been drawn that the overwhelming majority of today's manufacturing sites have ESD control measures in place that ensure safe handling of 500 V HBM parts. This includes the full manufacturing flow from wafer technology to testing, mounting and final placement on printed circuit boards when performed in an ESD protected area.

This experience of robust ESD control measures is seen by all companies contributing data to the Council and confirmed by ESD control companies represented on the Council involved in ESD manufacturing control for these components. As a wide variety of ESD protection circuits are used in these devices, this result can be considered to be independent of the detailed protection circuit concept.

The component level HBM qualification standard was created to ensure safe handling of ICs in ESD protected areas until assembled on a printed circuit board. During this phase of the manufacturing flow, a discharge between any combination of pins of an IC can occur. To guarantee a sufficient level of ESD robustness in later manufacturing steps outside an ESD protected area or even when the final system is handled by the end-user, system level ESD standards have to be applied to the endangered pins which are outside the scope of this white paper.

Based on the data collected and analyzed, **a revised HBM component level qualification target of 1000 V is unanimously recommended by the Council**. This target level includes an appropriate margin to the proven safe level of 500 V HBM.

The HBM target value is referring to the currently applicable test standards of ESDA, JEDEC and equivalents of several other standardization bodies. The HBM target is the recommended requirement for products and ensures MM performance for ESD protected areas.

Comparing a qualification level of 1000 V to a 2000 V HBM requirement, the industry will benefit from the following factors:

- No change in quality of ICs seen by the customer
- No change in process yield at the manufacturer
- Faster design cycles of ICs
- Elimination of many unnecessary design re-spins
- Gain in average time to market of electronic systems

7.2 Treatment of Special Pins

Pins which are prone to ESD discharge at the printed circuit board level or in the electronic system handled outside ESD protected areas have to obey system level ESD standards. These are system specific and are not covered by device level tests. Component level ESD tests do not correlate to system level tests. Weak system level ESD has been seen for pins with high HBM levels. The number of IC pins exposed to system level ESD is system specific. For a high pin count IC there are typically only a few pins that need system level requirements.

For a long time the ESD requirement for a subset of pins, e.g. RF pins, has been traded off with operating performance. To account for extreme performance requirements it is foreseen that this will continue in the future.

7.3 Timeframe for Applying New Recommendations

The data shown in this paper reflects data from ICs over a broad period of time. The analysis of the ESD handling capability of the manufacturing site is not limited to a special process technology or generation. As such, the recommendation is general and valid for any design developed now or in the future. However, the benefit of applying the new recommendation will be highest for ULSI technologies at 65 nm CMOS and below and complex SoC/SiP designs. In these cases the over-design is in average most expensive (in terms of design resources and die manufacturing / mask cost) and causes the largest delay.

7.4 Future Cost of ESD Design

While we have recommended a component HBM qualification shift from 2 kV to 1 kV, one should further consider the continued "Cost of ESD". As described in Chapter 4, this cost is going up exponentially, burdening the suppliers in delivering the products on time and inconveniencing the customers in receiving products that have the expected performance. These projected cost curves are shown in Figure 21.

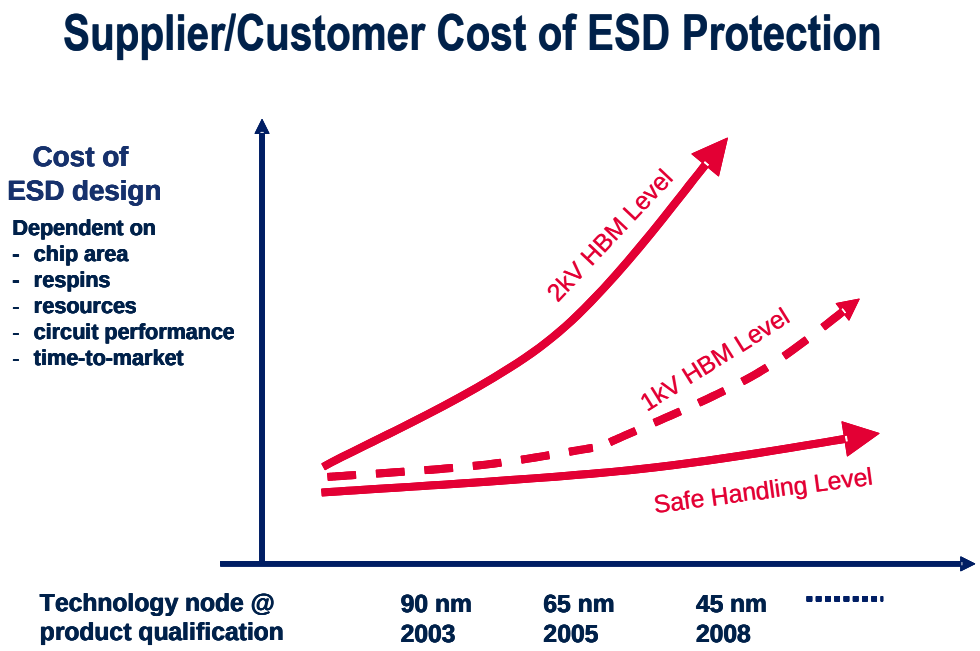

Figure 21: The projected cost of ESD requirements as a function of calendar year and the technology node, comparing current customer requirements versus lower recommended target and safe level requirements for handling in an ESD protected area with basic ESD control measures.

It is obvious that if safe handling only requires, for example 500 V HBM levels, there has been unnecessary cost for the last few years and this trend is expected to continually get much worse if we stay at the existing 2 kV HBM levels. What is also evident is that even if the ESD target level was to be further reduced to 500 V in the future, the cost of ESD design will still go up, albeit more slowly, because the technology impact will continue to play a significant role. This is one strong argument as to why the Industry Council recommends immediate lowering of the ESD levels independent of the technologies of the products that are in production now. Furthermore, this realistic shift will enable more focused R&D to develop effective ESD protection concepts that can be compatible with the very advanced 32 nm and 22 nm technologies in the near future. Equally important is the much-needed focus in understanding and developing protection for system level ESD tests such as transient latch-up (TLU) test and the cable discharge event (CDE) test. These very important tests for the IC products in their electronic applications are described in reference [1].

7.5 Product ESD Evaluation Criteria

Following the information given in this document, the Industry Council asks the IC suppliers, IC customers, and the OEM's to consider the true ESD HBM requirements as summarized Table V below.

7.5.1 Supplier to Customer

With this recommendation in place, the ESD negotiation between the customer and the supplier becomes much more realistic and flexible. As specified in the table when a product passes 2 kV it does exceed all the requirements, if it meets 1 kV instead the product is still very safe since it would have margin as stated in Section 7.1. According to this study even if it only passes 500 V HBM the product still meets the requirements adequately and is safe. Therefore, this should smooth out current misunderstanding between the supplier and the customer, and eliminate a lot of the unnecessary waivers. It should also pave the way for ESD requirements for the advanced technologies that are under development.

7.5.2 Catalogue Products

Catalogue products are often dealt with multiple customers and therefore a classification with a quantitative number may or may not have much meaning. As explained, products passing 1 kV or 4 kV are just as reliable. Therefore we propose future classification as suggested below to be adopted so that this dubious marketing competition for catalogue parts is eliminated. With this approach, Product X with 4 kV HBM exceeds requirements, Product Y with 2 kV HBM exceeds requirements, and Product Z with 1 kV meets requirements with available margin. Thus the marketability of all three products is equally appealing and mutually beneficial to both the customer and the supplier while the true circuit performance specifications remain as the only critical factors for consideration.

7.5.3 Realistic Rating of ESD Qualification Levels

Table V: Proposed component level ESD targets after testing according to ANSI/ESDA/JEDEC JS-001 (HBM).

HBM Level of IC	Impact on Manufacturing Environment
2 kV	Basic ESD Control methods allow safe manufacturing with proven margin
1 kV	
500 V	
100 V to <500 V	Detailed ESD Control methods are required

Basic ESD Control: Include wrist straps, grounded work surfaces, and safe packaging materials – and are safe with proven margin to 500 V
Detailed ESD Control: JESD625B has a scope of 200 V, but does not have a footwear-flooring system test for personnel grounding.

Processes compliant to ANSI/ESD S20.20 or IEC 61340-5-1 allow handling and manufacturing of ICs even as low as 100 V HBM

7.6 Looking Forward

As noted in Table V, products with HBM ESD levels <500 V can also be safely handled but do require detailed ESD control methods such as the ANSI/ESD S20.20 or the IEC 61340-5-1. The cost of such detailed control implementation would only be incremental. Factories and production areas must seriously consider moving towards these methods if they are not already doing so. As we further scale down technologies and develop even faster circuit applications 100 V or 200 V HBM requirement would not be unrealistic within the next 5 years.

Currently, the Industry Council on ESD Target Levels is conducting extensive studies on the required CDM ESD levels for ICs to arrive at a safe CDM target level for components. The results and Council recommendations will be reported as an update to this White Paper currently targeted within the next year.

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Appendix A: Machine Model – Correlation between HBM and MM ESD

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This section addresses the relationship between HBM and MM ESD robustness of products. It will be shown that typically the MM value is 1/30 of the HBM value, or higher, with a few exceptions. This implies that if a product passes 1 kV HBM the expected MM performance is > 30 V.

A.1 Correlation

The previous section explained the development of the MM standard. Historically an MM:HBM ratio of 1:10 was commonly used, as is e.g. clear from the classification in the respective standards [1, 2]. For example, a class 2 HBM product passes at least 2 kV, where as a class 2 MM product should pass at least 200 V. This commonly accepted ratio most likely arose from observations on products at the time of development of the standards. These observations are given in [3], yielding a 1:11.7 ratio.

In [4] a ratio between 1:10 and 1:20 is quoted. In [5] a paper was published that demonstrated ratios of 1:10 and 1:17 measured on test structures, using 2 different types of MM. In [6] a ratio varying from 1:13.5 to 1:18 was achieved for different variations of stacked NMOSTs in an advanced CMOS technology.

All results are given, while stressing that very similar failures were observed for HBM and MM.

Simply equating the available charge in the HBM and MM models it could be seen that a crude, but not realistic, ratio of 1:2 might be expected (not accounting for issues such as impedance in the discharge path):

$$C_{MM}*V_{MM}=C_{HBM}*V_{HBM} \rightarrow V_{HBM} = 2 * V_{MM}.$$

Most HBM and MM failures are related to thermal damage: due to overcurrent creating thermal melting / reflowing. Pierce [7] has shown that by equating the energy deposited in the IC during the stress and assuming that all ESD energy is used to create damage the following relation can be found:

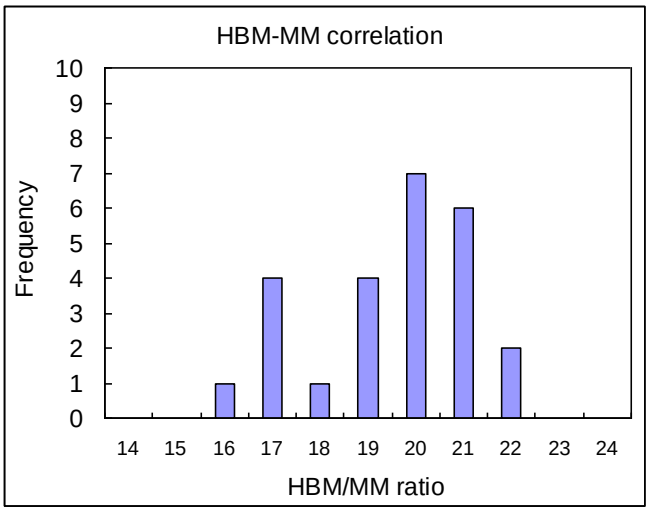
$$V_{MM}= \mathrm{sqrt}(R_{prot}*C_{HBM}/(C_{MM}*(R_{HBM}+R_{prot})))*V_{HBM}.$$

Using typical values this leads to an MM:HBM ratio of 1:25. This neglects the facts that power to failure depends on pulse width and that MM pulses are shorter than HBM pulses. From the above equation it is also clear that an increase of the Rprot leads to a lower ratio. By reducing the

HBM target the protection elements may have more impedance and thus the MM level will (relatively) be reduced less.

On the other hand, failures can also be induced if the protection does not clamp the voltage sufficiently. In this case, a small device or fragile oxide may become damaged with just a small fraction of the energy, because most energy is safely dissipated by the protection. For this reason it is good to compare peak currents for HBM and MM. According to the standards the peak current into a short is 1.3 A for a 2 kV HBM discharge and 3.8 A for a 200 V MM discharge. Equating peak currents thus leads to a 1:30 ratio of MM:HBM.

So on theoretical grounds a ratio between MM and HBM of 1:30 or lower is expected. This is confirmed on products and test structures by the publications quoted before. The council collected data both on test structures and products of several of the members. Figure A1 shows the results on the test structure. Clearly on average a ratio of 1:20 is found and factors larger than 30 are very unlikely.



average	19.1
median	20.0
3σ	5.0
median+3σ	25.0
max	21.9
min	15.7

Figure A1: HBM/MM correlation of test structures in an advanced CMOS process

A.1.1 Consequence of 1 kV HBM Target

Figure A2 shows data collected from several products from different suppliers and technologies. The figure shows the MM failure voltages vs. the HBM failure voltages. A best fit regression shows a ratio of 1:16. The whole population is bounded by 1:3 and 1:30 lines.

Figure A3 presents the HBM:MM ratio as a function of the HBM performance. It is clear that the ratio increases for increasing HBM level. This is mainly due to the fact that to achieve high HBM levels large, low impedance protections are needed. Since the protection impedance affects the MM peak current, this leads to a higher ratio for higher HBM performance. Conversely, as shown in Figure A3, as the HBM level is reduced the HBM:MM ratio is also reduced such that a minimum level for MM performance based on the HBM target level is still above 30 V. This is

mainly due to the fact that higher impedance is expected in lower HBM levels, indirectly "helping" MM performance. The above reasoning and data supports the conclusion that a 1 kV HBM target level will ensure an MM performance between 30 V and 200 V, with a typical expectation value of 60 V.

The above reasoning assumes that the MM bipolar stress case can be approximated by two unipolar HBM stresses. This means that the current and voltage rise times must be similar. It also means that the tester dynamics should be the same for both cases. Although these assumptions are correct for a large number of cases, MM and HBM can address different failure modes, in which case correlation is not possible. The next paragraphs will describe some of the cases in which MM and HBM do not correlate, detailed with measurements from different technologies and products.

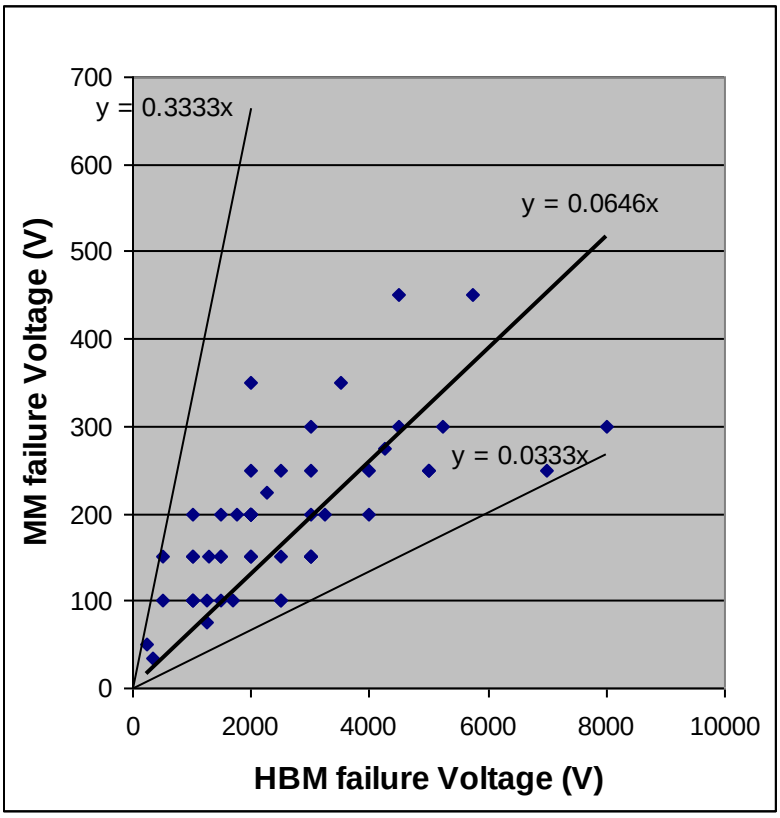


Figure A2: MM failure level vs. HBM failure level for several products of several companies.

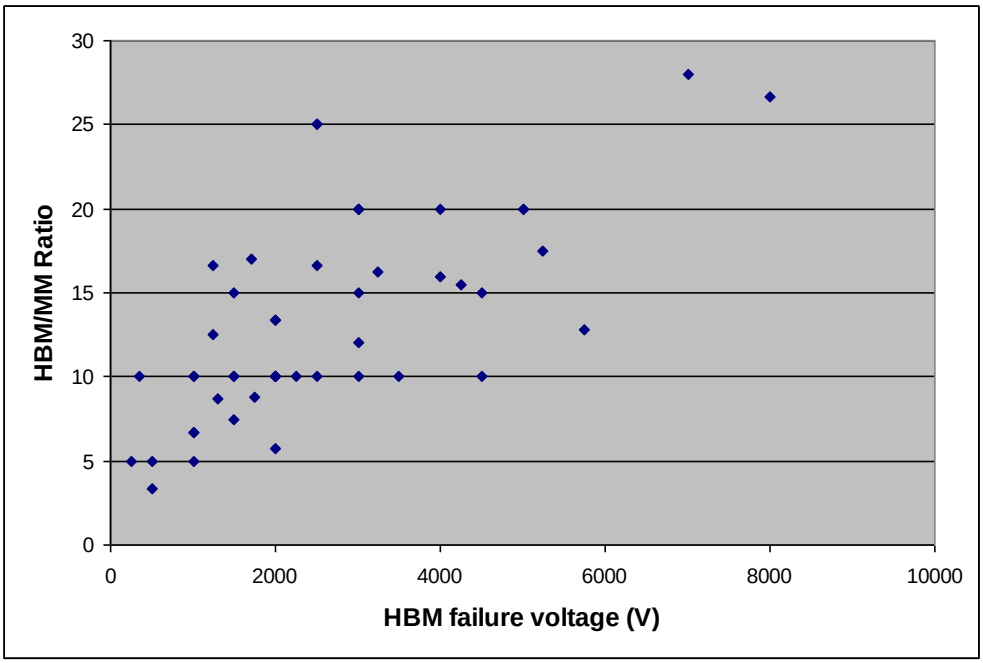


Figure A3: HBM/MM ratio vs. HBM level for several products of several companies.

A.2 Exceptions to HBM/MM Ratio

Bipolar vs. Unipolar Stress

The most obvious difference between MM and HBM is the bipolar nature of MM. Correlating the two models as shown in Figure A4 assumes that the device can be approximated in a quasi-static regime when the voltage crosses 0 during the MM pulse; only then can the MM level be extracted from a positive and a negative HBM level. In many cases this quasi-static approximation is reasonable, reducing the physics to the unipolar case.

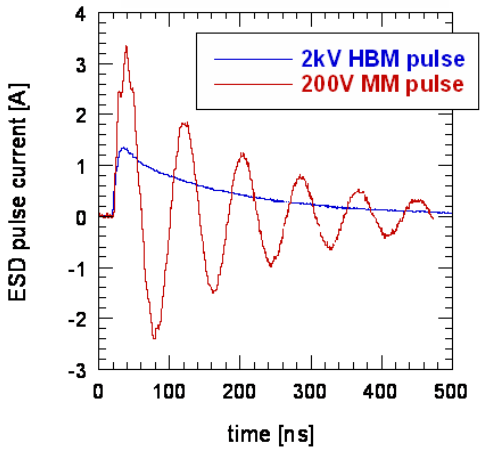


Figure A4: MM and HBM pulse, the main difference being the bipolar characteristic of the MM pulse

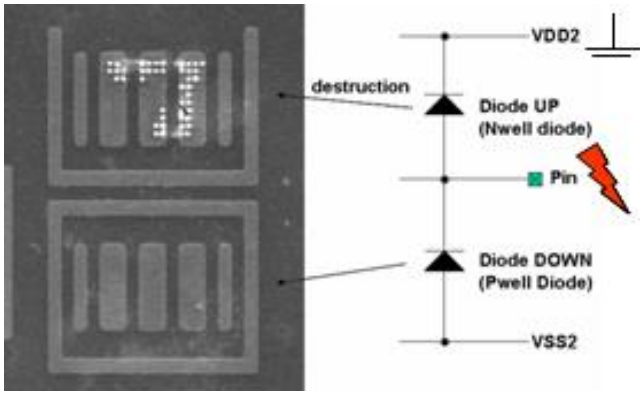


Figure A5: Diode up was destroyed by a positive MM stress between IO and VDD2.

This is however, not a general statement. One of the most notable physical effects for which this simplification is not valid is dynamic avalanching. In Figure A5 a case is shown in which MM stress damaged the diode from pin to supply VDD2, which cannot be explained by merely looking at the peak current or energy dissipated by the MM pulse. The well of the diode gets injected with charges during the first (positive) swing; when the stress reverses, these charges worsen the effect of avalanching at the Nwell/P+ junction. Dynamic Avalanching is one the most important effects where the pulse reversal has a dramatic influence on the ESD behavior of the device [8].

Advanced Technologies

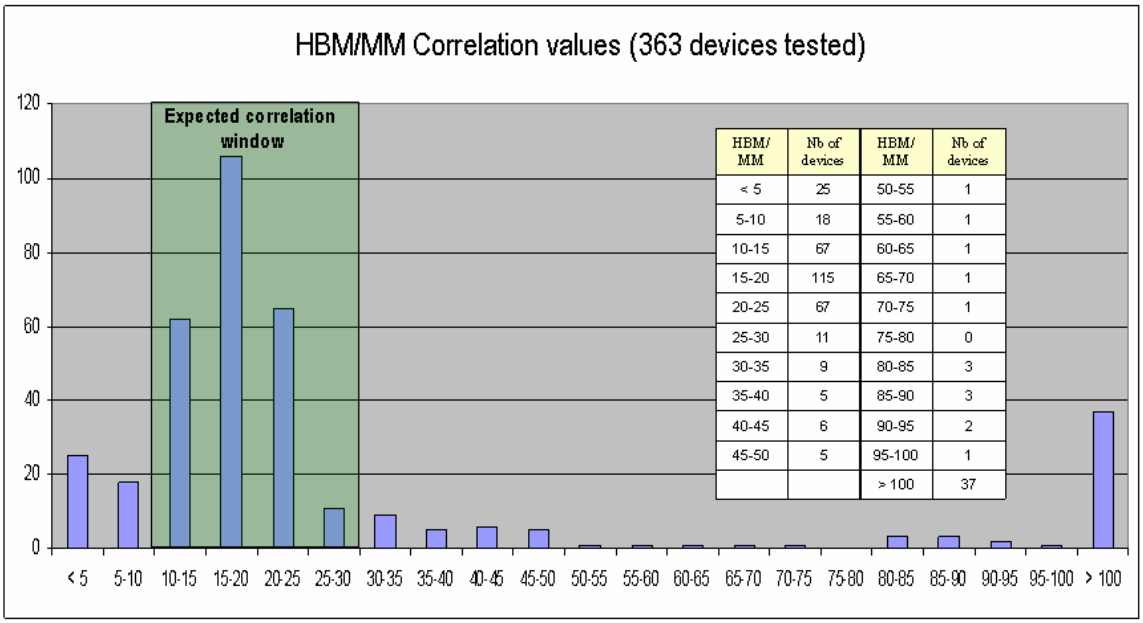
Figure A6 shows the results of HBM and MM testing on a wide variety of test structures in a 65 nm high performance technology. The majority (67%) of the test structures correlates well with the expected correlation (HBM/MM 10-30). A small portion (12%) has a lower correlation; some devices (21%) have higher correlation. All structures are either self-protective drivers or are measured with a sensitive node in parallel, such that the given numbers indicate their effectiveness as well as robustness.
Given the formula by Pierce:

$$V_{MM} = \mathrm{sqrt}(R_{prot} * C_{HBM} / (C_{MM} * (R_{HBM} + R_{prot}))) * V_{HBM}$$

higher correlation for lower resistive protection devices can be predicted. Care must be taken, however as this formula does not take into account the parasitic inductance of both testers (which is about 10 times worse for the HBM as for the MM tester), the test board capacitances and the parasitic resistance of the test board capacitances. The formula is plotted in Figure A7. Without the corrections for the tester parasitics, the correlation reaches infinity for zero Ohm protection devices, meaning the approximation is not correct for small Rprot. Note also that this correlation factor is closely related to the testers, and does not correlate with real life. As technology scales down, lower resistive protection devices are needed, meaning V_{HBM}/V_{MM} is expected to increase.

Also important to note is that the difference in parasitic inductance in both testers gives a very different rise time behavior. With poorly designed ESD protection, this might lead to large

variations in the correlation factor, and especially the MM value might vary from process (and lot to lot) variations.



HBM/ MM	Nb of devices	HBM/ MM	Nb of devices
< 5	25	50-55	1
5-10	18	55-60	1
10-15	67	60-65	1
15-20	115	65-70	1
20-25	67	70-75	1
25-30	11	75-80	0
30-35	9	80-85	3
35-40	5	85-90	3
40-45	6	90-95	2
45-50	5	95-100	1
		> 100	37

Figure A6: HBM and MM Results from a test chip in a 65 nm high performance technology

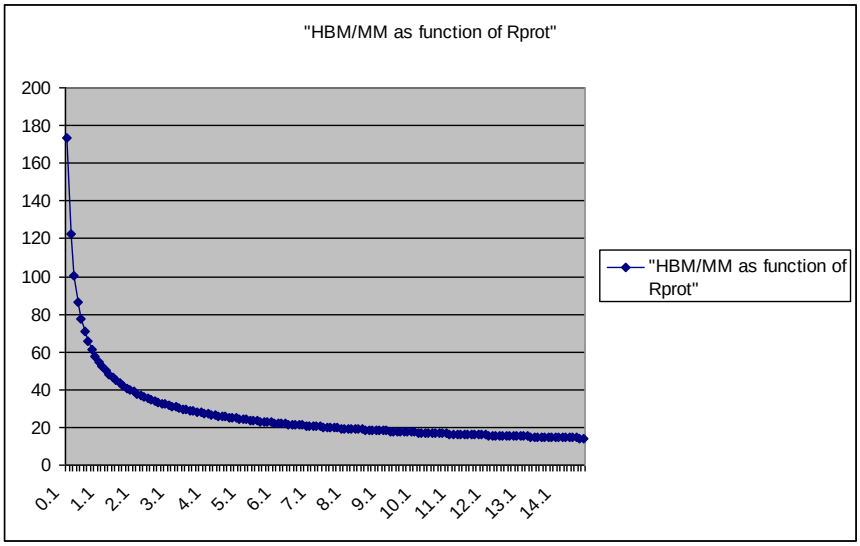


Figure A7: Pierce Formula for Different Rprot

An example of such apparent miscorrelation between HBM and MM qualification levels was reported for a product in a sub-micron Smart Power SOI technology. The product passed 8 kV HBM. Higher levels could not be tested due to tester limitations. The same product passed 1000 V CDM in a TSSOP32 package. During MM qualification a problem was observed. Whereas most pins were qualified without problems one specific pin combination failed at 75 V. This

same pin combination passed 50 V MM. The same pin types in other combinations also did not pose problems. The physical failure signature was a broken gate oxide on a transistor with its gate connected to the discharge path. Most likely the reverse recovery effect created a voltage overshoot due to the bipolar nature of MM. A rough calculation indeed shows that the voltage did rise high enough to damage gate oxide for that particular transistor. After a design fix the product passed 250 V MM (not stressed up to failure). No field returns related to this MM issue have been reported for both the initial and improved version.

A.3 Conclusions

It has been demonstrated that most of the observed HBM-MM relationships on products fall between the boundaries that are expected on theoretical grounds. Some rare exceptions to this general relation have been described. In most cases these are related to the use of relatively slow protection elements.

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Acknowledgement

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Revision History

Revision	Changes	Date of Release
1.0	Original release	August 2007
2.0	Table of contents updated, minor corrections throughout	October 2010
3.0	Updated Table in Exec summary, Table V in Section 8 and typo in Figure 11. Changed advanced ESD control to detailed ESD control. Fixed use of units throughout.	September 2011
4.0	Chapter 3 moved to Appendix A, all chapters adjusted to reflect this. Clarifications made on MM qualification testing to align with JEP172. Technology roadmap updated in Section 5.5. Abstract and Preface updated. A scope statement added. A Terms and Definitions section added. Clarifying statement added to Section 6.2. Minor formatting/grammar changes throughout.	June 2018