White Paper 3
System Level ESD
Part I: Common Misconceptions and Recommended Basic Approaches

Industry Council on ESD Target Levels

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Abstract

Over the last twenty years, an increasing misconception between system level designers (OEMs) and semiconductor component (IC) providers has become very apparent relating to three specific ESD issues:

- ESD test specification requirements of system vs. IC providers;
- Understanding of ESD failures in terms of physical failure and system upset and what causes these failures in terms of system level and IC level constraints;
- Lack of acknowledged responsibility between system designers and IC providers regarding proper system level ESD design.

In White Paper 1 from the Industry Council on ESD Target Levels, which presented a paradigm shift in the realistic and safe IC level ESD requirements, we introduced the importance of separately addressing the system specific and IC specific ESD issues. In White Paper 3 we present the first comprehensive analysis of system ESD understanding including ESD related system failures, and design for system robustness. The main purpose of the present document is to close the existing communication gap between the OEMs and IC providers by involving the expertise from OEMs and system design experts. This will be accomplished by what we describe in this document as "System-Efficient ESD Design" (SEED) which promotes a common IC / OEM understanding of the correct system level ESD needs. White paper 3 will be constructed of two parts. A key finding of Part I of the white paper is the development of a framework for sharing IC / system level circuit information so that best practice ESD protection and controls can be co-developed and properly shared.

Later, in Part II of White Paper 3, the Industry Council will use the information in Part I to establish recommendations for IC and system level manufacturers regarding proper protection, proper controls and best practice ESD tests, which can properly assess ESD and related EMI performance of system level tests. The purpose of White Paper 3, Part II will be to better define the ESD relationship between IC manufacturers and system level OEMs and their respective responsibilities.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies. *In terms of product shipped, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies, and over 70% of the total volume of product shipped by the top 20 companies, as reported in the EE Times issue of August 6, 2007*.

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Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system level ESD issues, the Council has now expanded its mission to directly address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system level ESD design. To ensure a broad range of perspectives the Council has expanded its roster of Members and Associates to include OEMs as well as experts in system level ESD design and test.

Preface

While IC level ESD design and the necessary protection levels are well understood, system ESD protection strategy and design efficiency have only been dealt with in an ad hoc manner. This is most obvious when we realize that a consolidated approach to system level ESD design between system manufacturers and chip suppliers has been rare. This White Paper discusses these issues in the open for the first time, and offers new and relevant insight for the development of efficient system level ESD design. This effort has been divided into two parts. In Part I, this document will identify and eliminate the misconceptions common in the understanding of system level ESD. This will be followed later by Part II where we will explore realistic system ESD protection requirements and strategies. We would also like to note that in Part I we address direct stress effects on external and internal pins of an IC while the more intricate effects of inter-chip pin coupling will be carefully considered in Part II. This document is intended to be useful for both chip suppliers and OEMs/ODMs. As a final note, we would like to clarify that this document addresses system level ESD issues only, but not Electrical Overstress (EOS) unless they manifest from a system failure.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing this information, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

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Glossary of Terms

AEC	Automotive Electronics Council
ANSI	American National Standards Institute
ASIP™	application specific integrated passive ™
bigFET	bipolar insulated gate field effect transistor
BiCMOS	bipolar complementary metal-oxide semiconductor
CAN	controller area network
CBE	charged board event
CCE	charged cable event
CDE	cable discharge event
CDM	charged-device model
CLK	clock
CM	contract manufacturer
CMOS	complementary metal-oxide semiconductor
DC	direct current
DUT	device under test
DSP	digital signal processor
ECU	electronic control unit
EM	electromagnetic
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EOS	electrical overstress
EPA	ESD protected area
ESD	electrostatic discharge
eSATA	external serial advanced technology attachment
ESDA	Electrostatic Discharge Association; ESD Association
EUT	equipment under test
FM	frequency modulation
ggNMOS	grounded gate N-channel metal-oxide semiconductor
GND	negative voltage supply
GRP	ground reference plane
HBM	human body model
HCP	horizontal coupling plane
HDMI	high definition multimedia interface
HMM	human metal model
HSS (HSSL)	high speed serial link
IC	integrated circuit
ID	identification
IDDQ	component quiescent supply current
IO	input/output
IP	intellectual property
IEC	International Electrotechnical Commission
ISO	International Organization of Standards
JEDEC	Joint Electronic Devices Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
LC	inductor/capacitor network
LIN	local interconnect network

LU	latch-up
MM	machine model
OEM	original equipment manufacturer
ODM	original design manufacturer
PCB	printed circuit board
PHY	physical layer
PICC	proximity IC cards
PUT	pin under test
RC	resistor capacitor network
RF	radio frequency
RLC	resistor inductor capacitor network
RP	residual pulse
RPS	residual pulse stress
RX	receiver
SAW	surface acoustic wave
SCR	silicon controlled rectifier
SMD	surface mount device
SOA	safe operating area
SPICE	simulation program with integrated circuit emphasis
TLP	transmission line pulse
TLU	transient latch-up
TVP	transient voltage pulse
TVS	transient voltage suppression
TX	transmitter
USB	universal serial bus
VBR	breakdown voltage
VCP	vertical coupling plane
VDD	positive voltage supply
VFTLP	very fast transmission line pulse
UTP	unshielded twisted pair

Crosstalk: Any phenomenon by which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel. This phenomenon is usually caused by undesired capacitive, inductive, or conductive coupling from one circuit, part of a circuit, or channel, to another.

ESD Design Window: The ESD protection design space for meeting a specific ESD target level while maintaining the required IO performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

External Pin (interface pin): An external pin is one which at the board/card level is exposed to potential ESD threats from the outside world.

Hard Failure: Failure of a system due to physical damage to a system component which can only be repaired by the physical repair or replacement of the damaged component.

IEC-Robustness: The capability of a product to withstand the required IEC ESD-specification tests and still be fully functional.

IEC ESD event: An ESD stress as defined in IEC 61000-4-2.

Internal Pin (non-interface pin): An internal pin is one which is exposed to ESD threats typically only during IC manufacturing.

It2: The current point where a transistor enters its second breakdown region under ESD pulse conditions and it is irreversibly damaged.

Residual Pulse: The resulting voltage/current (after system level ESD protection devices) seen by an IC component from an IEC stress waveform.

SEED: System-Efficient ESD Design - Co-design methodology of on-board and on-chip ESD protection to achieve system –level ESD robustness.

System level ESD Robustness: The capability of a product to withstand the required IEC ESD-specification tests and still be fully functional.

Soft Failure: Failure of a system not due to physical damage in which the system can be returned to a functional state without the repair or replacement of a component. Return to a functional state may or may not require operator intervention. Operator intervention may include rebooting or power cycling. Soft Failures can involve software issues and software fixes but in the context of this document they are primarily due ESD events injecting unwanted signals into the system which place the system into a state in which it does not function as intended.

Executive Summary

Our intention in this document is to work with the OEMs, and with their participation and feedback, eliminate misconceptions about system level ESD while jointly addressing the design of robust ESD systems. **Our aim is to bring suppliers and customers together for a common purpose towards the development of ESD robust systems.**

There is a growing awareness in the electronics OEM community that system level ESD robustness is an important requirement for reliable products. System level ESD testing is today applied to a wider range of products than ever before. Designing ESD robust systems can be very challenging, especially for systems which integrate advanced technology integrated circuit (IC) components. For most system designers, ESD protection strategy and design efficiency are only dealt with in an ad hoc manner. Many of the most severe system level ESD design problems can be traced to misconceptions between system designers (OEMs) and their IC providers. Adopting a consolidated approach to system level ESD design, which addresses these misconceptions, will be key to future success in building ESD robust systems.

This White Paper serves three important purposes. First it provides an overview of system level ESD test and design challenges in the industry today. Second, it identifies and characterizes the primary misconceptions mentioned above. Third, it introduces a new co-design approach called "System-Efficient ESD Design" (SEED) that promotes a common OEM/IC provider understanding of the correct system level ESD needs.

This white paper is the first part of a two part document. Part I will primarily address hard failures characterized by physical damage to a system. "Soft failures", in which the system's operation is upset but without physical damage, is also critical and predominant in many cases. The same soft failures can also refer to system upsets involving recoverable damage to system malfunction. However, these issues are out of the scope of the current document and will be dealt with in detail in Part II of this white paper. Although EOS failures can result from a system failure our focus here is not intended to cover other types of EOS failures that can come from mishandling, etc.

Background and Purpose (Chapter 1**)**

There is a critical need in the IC industry to directly address the growing division in the understanding of system level ESD between system/board designers and their IC providers. The true nature of system ESD reliability, especially in light of the rapid advances in the IC industry, requires a comprehensive examination. There are three aspects to this study.

1. Understanding of the nature of system failures which can be either "hard" or "soft." Hard failures are typically related to physical damage which is not recoverable, while soft failures describe a system upset or malfunction including recoverable damage.

2. Clarification of misconceptions that often lead to an inefficient approach to system level ESD design. For example, the commonly held belief that IC level ESD specifications (such as the HBM) can ensure robust system ESD design.

3. Definition of the whole system in the context of which portions of the IC components on a PCB are involved in the protection strategy. For instance, identifying the external (interface) pins that would be in the critical path of an ESD event and require careful

design strategy, versus internal (non-interface) pins which are not as affected and may not require special attention during system design. However, while differentiating internal versus external pins, it must be noted that issues associated with inter-chip pins are also important. Part I will address only direct stress issues while the indirect effects coming in from coupling will be dealt with in more detail in Part II of the white paper. OEM concerns about failures of products in manufacturing and in the field have often led system manufacturers to take their own initiatives, whether effective or not, or to make various demands from the IC suppliers, whether justified or not in each and every case.

Test Methods and Their Field of Application (Chapter 2)

The existing system level ESD test methods and their field of application are discussed in great detail. First, it is noted that IEC 61000-4 is a set of EMC test standards which includes the system level ESD test method, IEC 61000-4-2. It specifies calibration waveforms, procedures and stress points for executing ESD tests on systems. The standard clearly excludes several locations and situations. The standard also explicitly encourages committees, manufacturers and users to derive standards from IEC 61000-4-2 for specific applications. We discuss the IEC 61000-4-2 ESD procedure and present several examples of application specific interpretations. We also discuss examples where people have derived practices to stress locations or situations that were excluded in the IEC 61000-4-2. The most extreme example is the application of system level ESD stress directly to ICs. Several approaches for this application are discussed.

Proven System Level Fails (Chapter 3)

Here we address proven system level failures from actual case studies, examples of both field returns and failures generated during qualification testing. Field failures generated during a system operation are not easy to resolve as to whether they come from ESD or EOS types of events. If a failure is detected, a thorough root cause analysis would be necessary to establish the cause. The examples given try to ascertain whether the failures are related to the device HBM or CDM robustness as well as the type of external protection device implemented and their effectiveness in protecting against an IEC ESD event. By classifying the failure types and establishing the failure statistics a better insight into the system failure phenomena will be obtained. In this document we highlight how system problems are typically solved.

OEM System Level ESD Needs and Expectations (Chapter 4)

Next, we discuss the needs and expectations that OEMs have from their IC suppliers such that the OEM can design products that will not be physically damaged or have their operation upset by ESD stress. Three hypothetical design paths for ESD robust systems are outlined:

1. Design with ESD robust ICs in which ESD is not a concern.

2. Design with a combination of ESD robust and non-robust products, but with clear guidelines, procedures and tools available (i.e., the SEED approach).

3. Design with a combination of ESD robust and non-robust ICs, but without clear ESD guidelines, procedures and tools available to the system designer.

As desirable as path 1 may be, it is typically unrealistic. Instead we describe the information and tools needed to move from path 3 (which often describes ESD system design today) to path 2, which is a realistic goal for the future.

Lack of Correlation between HBM/CDM and IEC 61000-4-2 (Chapter 5)

There is a common assumption in the system design community that the IC level HBM has relevance to ESD performance at the system level. This assumption persists because of a lack of understanding of the differences between the models and a lack of actual data to make valid comparisons. Figure 1 contains data where some IC and system level information is available for a rough comparison. Details of the tests which were done to generate this data are not available as is often the case. However, this limited data serves to suggest that correlation is not likely (though not disproven by such a small data set). In this section, this lack of correlation and why this is expected is discussed. The relationship between IC ESD models (HBM and CDM) and the IEC 61000-4-2 is further explored. By comparing required waveform characteristics, equivalent circuit models and practical realization issues, it is demonstrated that these IC models cannot be expected to correlate to system level ESD. Actual test comparisons that have been reported in the literature are reviewed. While emphasis is placed on common HBM and CDM tests, comparisons to other emerging models are discussed. These include cable discharge events (CDE), human metal model (HMM), transient-induced latch-up, extended pulse length transmission line pulse (TLP) and charge-board events (CBE).

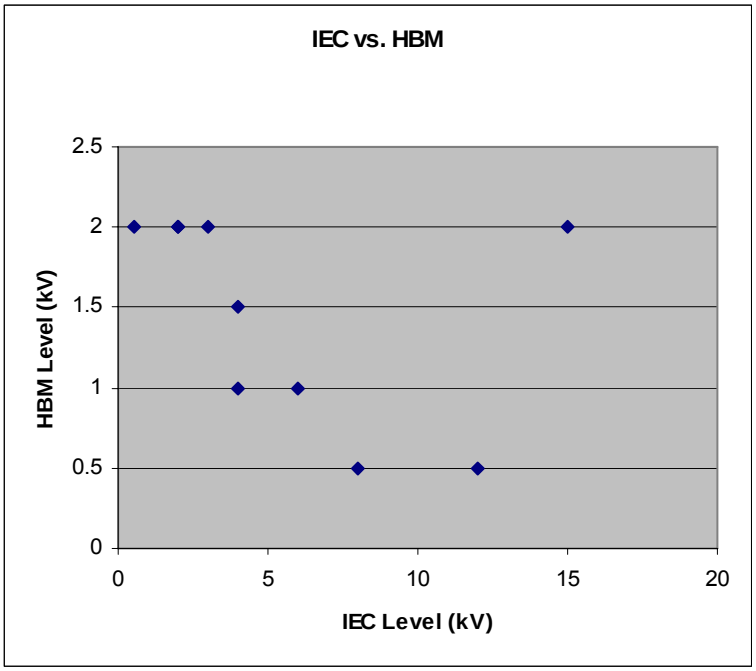

Figure 1: Comparison of IC ESD and System ESD

Relationship between IC Protection Design and System Robustness (Chapter 6)

Finally, we discuss the relation between IC protection design and system design robustness to avoid physical damage. Requirements and constraints of IC level ESD protection design are presented. Starting by highlighting misconceptions in equating IC ESD robustness, like HBM according to JEDEC with system level ESD robustness, a detailed discussion of various system level ESD protection concepts (both on-chip and on-board) is performed. On-board and on-chip protection circuits interact and can even compete. This requires a careful evaluation of the relevant parameters. Using analysis methods like transmission line pulsing, which reflect essential characteristics of IC pins and board protection elements, a systematic design of system level ESD protection can be developed. Essentially the comprehensive on-chip/ on-board protection co-design methodology, referred to as System-Efficient ESD Design (SEED), enables an optimum protection design from building blocks that provide a clear advantage to today's trial and error approach. The generic SEED concept is illustrated in Figure 2. The benefits are discussed for some examples like USB, CAN bus and antenna interfaces.

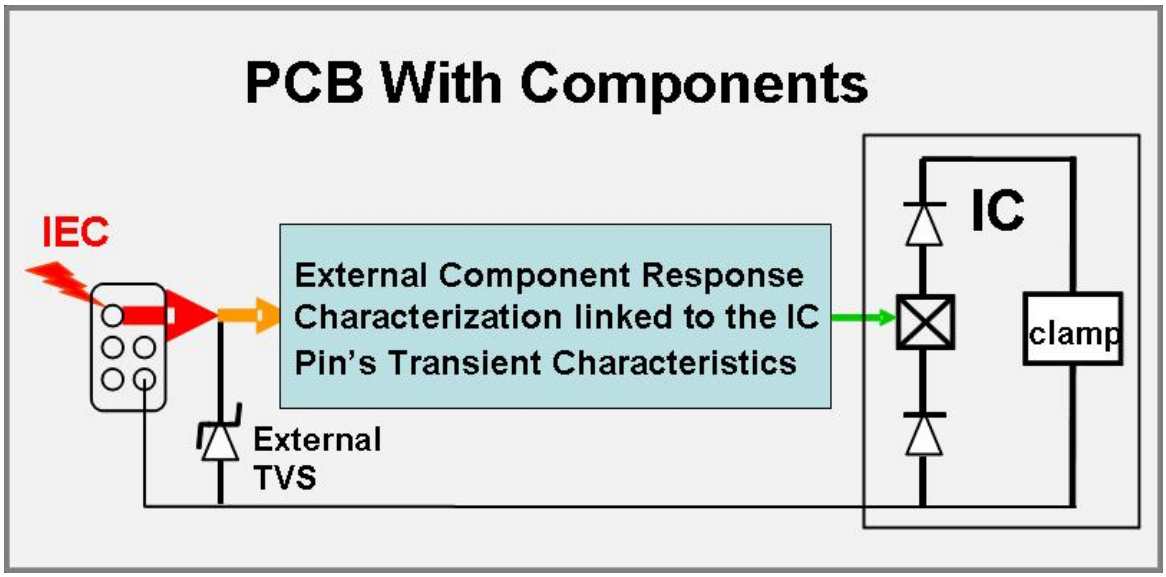

Figure 2: System-Efficient ESD Design concept requires careful consideration of interaction between the PCB protection and the IC pin transient characteristics.

Cost of System Protection

Assessing the cost of design, it becomes clear that a co-design approach is superior to design concepts relying on excessive ESD robustness requirements at the IC level. We show a path that illustrates how IC suppliers and system manufacturers can cooperate in the future, with both parties benefiting from this approach to achieving required system robustness without overly specified IC level ESD targets and performance restrictions.

Frequently Asked Questions

Q1: Why is the Industry Council addressing Non-Correlation issues between Device Level and System Level testing?
Answer: Some OEMs have been under the impression that higher levels of system robustness can be achieved by designing and measuring greater than necessary IC ESD levels. Our focus is to show that the system ESD measurement is relevant only when the IC is placed on the PCB and that stress data obtained at the IC level does not often correlate to system ESD capability when running the current IEC 61000-4-2 test procedure.

Q2: Is there a correlation between device failure thresholds and real world system level failures?
Answer: There is rarely correlation between device (IC level) failure thresholds and real world system level failure in the field. Device failure thresholds are based on a simulated ESD voltage and current directly injected into the device (IC) with the device in a powered down condition. Real world system level failures in the field occur in many different conditions, most of which are powered. In addition, there is no clear definition of soft failure robustness for ICs, and many real world errors are soft failures. First one needs to establish reliable methods for soft failure evaluation of ICs before one can attempt to compare IC level and real world failures.

Q3: Why wouldn't you expect to see correlation between IC level and system level testing?
Answer: Since the tests are done in different environments (unpowered versus powered or stand-alone versus on board) along with the different stress current wave shapes for the two tests, it is not surprising that they would be uncorrelated. In some instances external IC pins with higher IC level ESD robustness may result in less of a load on the on board ESD protection components. However, there are many examples where an improved HBM level for an IC resulted in lower system level ESD as discussed in Chapter 5 and Chapter 6. The approach of relying on IC level ESD for system level ESD protection is not only impractical and unpredictable, it also detracts from the need for an efficient system ESD design in which the on board and on chip protection work together.

Q4: Why are IC manufacturers now being asked to perform System Level testing at the IC level?
Answer: On the surface this seems like a very logical thing to do. If ICs and all other components can survive system level stress, it would appear that there should be no problems when it comes time to test the system for ESD robustness. There is also the desire to reduce component count for economic reasons. Unfortunately this approach may not be the most practical or economic approach and it also may not work. See Chapter 4.

Q5: Will there be a need for an IC ESD Target Level, to confirm System Level performance?
Answer: No. System level performance is a combination of on-chip ESD protection, on-board protection components and system mechanics design. The detailed properties of the IC's ESD protection such as turn on voltage, resistance, and maximum withstand current are much more important than the IC's HBM and CDM level measured in voltage. Automotive manufacturers do require some levels of IC ESD robustness for some bus transceivers but the specific test conditions are specified to be very close to use conditions.

Q6: Can devices really be designed to withstand real world system level events?
Answer: It is certainly possible to design ICs that can withstand system level ESD stress, but it is a complex and often unwise path. It is hard to know the exact details of the stress that will reach

an IC on a board due to circuit board parasitics, making the design difficult and prone to overdesign. Additionally, IC protection for IEC stress consumes considerable area and is likely not to be the most economical path.

Q7: Do all pins on a device need to be tested using system level events?
Answer: External pins (e.g. USB data lines, Vbus line, ID and other control lines; codec and battery pins, etc) need to be tested if the IC is not to be protected with on board components. But if the pin is to be protected by on board components, TLP characterization of the pin is more useful. Some internal ESD sensitive pins (e.g. control pins, reset pins, and high speed data lines, etc.) can be inductively coupled during a discharge to the case and/or to an adjacent trace of an external pin undergoing system testing. These pins need to be identified and may need to be tested using system level events.

Q8: JEDEC publication JEP155 recommended lowering IC ESD levels; will this have an impact on the overall system reliability?
Answer: Many systems, outside of the automotive industry, have been shipped with the IC ESD levels as recommended by JEP155 without a reduction in system level ESD robustness or an increase in other reliability issues (Data in the automotive industry is lacking because that industry has been very strict about maintaining the higher IC ESD levels. Although in the automotive industry ECUs containing devices with lower component ESD robustness are out in the field without known problems). First of all, most pins on an IC are signals that are internal to the system and will not be directly exposed to system ESD stress. Even for externally connected IC pins the relation between IC level ESD and system level ESD is not straight forward. Traditional levels of IC ESD robustness such as HBM 2000 V and CDM 500 V are not enough to protect against the much more severe system level ESD tests. In a system the IC's on chip ESD protection must work in harmony with the system level ESD protection. Increased levels of HBM and CDM can in fact lower system level ESD performance if the IC's ESD circuits begin to conduct at lower voltages than the board level ESD protection (see Section 6.7.1). This is an area that needs further work as stated in Clause 11 of JEP155.

Q9: If system level ESD testing at the IC level does not guarantee system level ESD performance, aren't higher target levels of IC HBM ESD better than nothing?
Answer: This would only give a false sense of security and could result in extensive cost of analysis, customer delays and a circuit performance impact. (Remember, higher HBM ICs may be harder to protect!). System ESD protection depends on the pin application and therefore requires a different strategy. System level ESD is clearly important, but targeting excessive IC level requirements could pull resources away from addressing and designing better system level ESD.

Q10: I often hear that the IEC 61000-4-2 pulse is a superposition of a CDM and a HBM pulse. Can IEC 61000-4-2 ESD testing replace CDM and HBM testing?
Answer: No. Looking at the two peaks in an IEC 61000-4-2 pulse the time duration is indeed comparable to a CDM and HBM pulse. However the required levels and discharge nature are completely different. This is because HBM and CDM is intended for IC level testing while IEC 61000-4-2 is intended for system level testing.

Q11: If CDM methodology and levels are modified would there be more fallout for EOS at the IC or System Level?
Answer: CDM and EOS event fails are completely different in total energy and time duration. Effective CDM protection does not guarantee EOS protection. EOS protection must be provided at the system level. There is no correlation between IC CDM failures and system EOS failures. Please refer to Annex D.1 and Annex D.1.3 for details in JEDEC publication JEP157. The fallout rate due to EOS would not change as a result of modifying CDM methodology and levels.

Q12: Since ICs are now designed for lower IC ESD levels, why would this not be reflected by a sudden change in the overall health of a systems for ESD capability?
Answer: The overall health of a system is dependent on a comprehensive approach to the protection methodology that includes a number of factors including on board protection components, optimized board signal routing, component packaging and, as a last line of defense, the IC level protection.

Q13: If all the recommended approaches listed in this document are followed would we then guarantee that a system will never fail for ESD?
Answer: One cannot guarantee that a system will never fail from ESD because there are many different discharge conditions and levels in the field. ESD sensitivity from one system (OEM product) to another system is always different because of differences in various product designs. Note; the recommended approaches in this document are intended to help produce more robust systems in a more efficient manner.

Q14: How will you reach all the different system designers for their inputs?
Answer: The current document has been reviewed by a number of OEM representatives and they are in agreement with the conclusions of the document. We expect that the publication of this document will result in further input from the system design community. This input will be especially important as the Industry Council works on Part II of this white paper.

Q15: If the system designers who are not involved in this document do not agree that it is a shared responsibility then what is next?
Answer: The system designers need to be educated in terms of system ESD versus IC protection design. Education with regard to these issues is a major focus of the Industry Council and we are convinced that as the benefits of the shared ESD responsibilities become evident more system designers will become convinced of their shared responsibility.

Q16: If an IC with the new lower ESD levels starts showing high levels of system failures how will the industry address this?
Answer: First, an investigation comparing ICs from provider A and provider B should look at the details of the IC level ESD designs, not just the IC failure levels in volts. Second, the OEM should share the system level ESD test results with the IC providers. For example, if IC provider A fails and IC provider B (2nd source) passes. IC provider A needs to investigate why their IC fails. Next, the OEM should review their ESD protection design for further improvement for both IC suppliers. This type of dialogue is important in the future.

Q17: What is the purpose of IEC 61000-4-2?
Answer: The purpose of the IEC 61000-4-2 test is to determine the immunity of systems to ESD events during operation. The document states that it relates to equipment, systems, subsystems

and peripherals, without further defining them. Its scope and description clearly indicate the purpose: to test electrical and electronic equipment that may be subjected to ESD from operators directly to the system under test or from indirect discharges from personnel to adjacent objects. See Section 2.0.1 of Chapter 2.

Q18: Which level does my system need to pass according to IEC 61000-4-2?
Answer: Like the international HBM and CDM standards, the IEC 61000-4-2 spec does not prescribe pass/fail levels. It describes the method and procedure on how to perform the tests. Related documents, such as IEC 61000-6-1, state that 4 kV contact discharge and 8 kV air discharge are suitable requirements. See Sections 2.0.2 and 2.0.3 of Chapter 2.

Q19: I cannot apply IEC 61000-4-2 as intended. What can I do?
Answer: Actually the IEC 61000-4-2 states that it serves as a basis to derive suitable standards for situations that are not covered by the document. For such cases, user committees should develop suitable procedures. Chapter 2 discusses several such standards.

Q20: What is HMM?
Answer: HMM stands for Human Metal Model. It is a method to assess the robustness of external IC pins against a system level ESD pulse. See Section 2.2.2 of Chapter 2 for details.

Q21: Is the Human Metal Model related to Machine Model? Should a device be required to have high MM levels to pass the HMM and this help the IEC performance?
Answer No. HMM has nothing to do with MM. Besides, MM is not a relevant IC level test and should not be used for any type of assessment.

Q22: After System Level ESD stress my application needs to be re-set. Is this a fail?
Answer: This is really application specific. Several system levels standards, including the IEC 61000-4-2 give several failure criteria. Which one is applicable depends on the application. E.g. for consumer electronics a manual re-set might be acceptable, but for safety-related applications this is strictly forbidden. See Section 2.0.2 of Chapter 2.

Q23: IEC 61000-4-2 refers to system upset. How do I evaluate this on my module or IC?
Answer: For a module this may be possible, if the module can be operated outside of the full system. Possible methods for modules are discussed in Section 2.0.4 of Chapter 2. For ICs the options are more limited. Latch-up tests such as JESD78B help to show immunity from upset but a standardized test method for transient latchup would provide a useful tool. For application to ICs typically permanent damage is the only failure criterion. See Section 2.2.2 of Chapter 2. Tests such as HMM could be performed on an operating IC but the required test setup would likely be very complicated.

Q24: Do all system level ESD standards use the same waveform?
Answer: In short: No. However, most use the waveform as defined in the IEC 61000-4-2, which is determined by a 330 Ω, 150 pF RC network. An example of a standard that uses a different waveform is ISO 10605, This standard uses the same type of ESD gun but the RC network is modified for some of the tests, using a 2 kΩ resistor and/or 330 pF capacitor instead of the values used in IEC 61000-4-2. See Section 2.1.1 of Chapter 2.

Q25: Is SEED considered to reproduce real, physical behavior of board and IC?
Answer: SEED is a concept to limit damaging current pulses reaching the internal IC pin. So in this sense it represents what the physical effect would be on the IC pin coming from an IEC stress at the external port of the PCB. What it represents for the board depends on how well the scenario is represented during the SEED analysis.

Q26: How can system/board designers get the required information about the IC IO behavior?
Answer: First, both the OEM and the IC supplier must define the 'external pins'. Following this, the IC supplier provides the TLP curve of the pin under interest with either bias applied or without bias which would depend on the pin application in the overall system board. The measured TLP at the pin will not only represent the pin's internal ESD clamp behavior but it will also include the IO design behavior to the transient pulse analysis.

Q27: What is the required degree of accuracy of the simulation models?
Answer: The simulation models can only be as accurate as the measured waveforms at the external clamp under IEC pulses along with the variations, and the internal IC clamp under the TLP conditions. Experience will teach us what level of accuracy is needed. Even if early attempts at simulation do not have the level of accuracy we may desire the simulations will still provide insight into the ESD properties of a design.

Q28: How can snapback devices be handled?
Answer: At first glance it would appear that snapback devices that are part of the on chip ESD protection would present a challenge in the design of an on board protection strategy. If, however, the on board clamp circuit maintains the voltage and current in the IC below the voltage and current failure levels of the snapback device there should be no problem.

Q29: Are different models needed for powered and unpowered conditions?
Answer: This depends on the pin application where the OEM would define whether the external pin would be facing powered conditions. It is generally good idea to provide TLP for both powered and unpowered conditions

Q30: Is it enough to simulate only an idealized IEC waveform or do we have to consider a wider range of discharge waveforms like CDE pulses etc?
Answer: This again depends on the application of the pin in the system board. For example, if it is an Ethernet pin a CDE pulse characterization may be important. It is generally a good idea to use waveforms that represent the expected system level stresses as best as possible.

Q31: What do you mean by hard and soft failures?
Answer: A hard failure is one in which a component of the system is physically damaged and the component must be repaired or replaced to return the system to a functioning state. A soft failure is one in which the system can be returned to a functional state without a physical repair to the system. A soft failure may or may not require operator intervention. Operator interventions may include the shutting down of a program on a computer or the power cycling of a system

Q32: HBM testing seems to be measured differently in different documents or discussions. This is confusing. Why is there a difference and what is it?

Answer: When the first ESD event measurements were made many years ago, the HBM term was used for any electrostatic discharge from a human. Both the discharge from the finger and the discharge from a metal object held in the hand were identified as HBM. Both these tests retained the HBM name for many years with widespread confusion. IC testers (i.e. two pin and multi-pin HBM testers) used the HBM name and hand held system level testers (ESD guns) sometimes also used the HBM name, even though these were two very different applications.

Just a few years ago the ESDA finally chose to differentiate them. The HBM (Human Body Model) definition remains for the current discharge through two pins of an IC provided by 2 pin or multi-pin "HBM" test system.

HMM (Human Metal Model) is a new term which defines the direct IC two pin device testing with the IEC 61000-4-2 waveform. Its lower spark resistance from a metal object held in the hand creates a higher current discharge than HBM testing at the same voltage. This is the threat provided by both ESD guns and the recently included IEC-50 ohm source HMM test systems.

Although the HBM term was originally used for both tests; you can help minimize this confusion by remembering these simple but important differences, and refraining from referring to either the HMM device test or the IEC 61000-4-2 system test as HBM!

Chapter 1: Purpose and Introduction

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1.0 Motivation and Purpose

There is a critical need in the IC industry to directly address the growing division in the understanding of system level ESD between system/board designers and their IC providers. The true nature of system ESD reliability, especially in light of the rapid advances in the IC industry, requires a comprehensive examination. There are three aspects to this study.

1. Understanding the nature of system failures which can be either "hard" or "soft." Hard failures are typically related to physical damage while soft failures describe a system upset. Soft failures on other hand refer to system upsets involving recoverable damage to system malfunction.
2. Clarification of misconceptions that often lead to an inefficient approach to system level ESD design. One such misconception is the commonly held belief that IC ESD specifications such as the HBM test can ensure robust system ESD design.
3. Definition of the whole system in the context of which portions of the IC components on a PCB are involved in the protection strategy. For instance, identifying the **external (interface)** pins that would be in the critical path of an ESD event and require careful design strategy, **internal (non-interface)** pins which are not affected and do not require special attention during system design and internal pins which are susceptible to stress via coupling.

The main purpose of this white paper is to address these issues from a variety of perspectives; including IC manufacturers, system board designers and OEMs/ODMs. The target audience spans the range from IC manufactures to board designers to OEMs/ODMs because the solution of system level ESD issues requires the effort and communication from all stages of system development.

As a special note, this document focuses on ESD protection designs, and is not intended to address the full scope of Electro-magnetic Interference immunity designs.

1.1 Scope

This white paper is the first part of a two part document. Part I will primarily address hard failures characterized by physical damage to a system (failure category d as classified by IEC 61000-4-2). Soft failures, in which the system's operation is upset but without physical damage, is also critical and predominant in many cases. We also note that some indirect coupling that might occur between interacting chips on a board are much more complex to describe but these will be considered in more detail in Part II. While preventing hard failures requires a carefully optimized approach, soft failures require an even deeper understanding of their nature before they can be

comprehensively addressed. For example, whereas hard failures involve direct current stress leading to damage, many soft failures are associated with the complex nature of EMC. Other types of failures can come from pure EOS events involving a shorted battery, inductively coupled surge from power supplies, or even lightning strikes. These specific issues are not in the scope of this document.

Although some soft failure issues and methods for designing systems against them will be covered in Part I, the issues associated with the numerous types of soft failures will be dealt with in more detail in Part II of this white paper.

1.2 Background

The ubiquity of electrical systems in modern life has led to their increasing deployment in hostile environments. It is well known that system components such as integrated circuits are susceptible to damage or data upset from externally generated electrical overstress, including electrostatic discharge events. Consider for example some common system level EOS/ESD events that may occur:

- A microprocessor IC on a laptop computer damaged when plugging in a charged USB cable

- A system built by cabling several large frames together fails during installation caused by damage on a device pin at the connecting point

- A communications IC on an operating cell phone suffers data state upset when a charged person touches the keypad

- A microcontroller IC on a washing machine is damaged due to inductive voltage spikes as the motor switches on

- A power management IC on an operating mobile phone suffering power loss that only happens in the winter when a user removes it from the holster

Even from the short list above, it is clear that system level EOS/ESD events can be caused by a wide range of application-dependent external stress sources. EOS/ESD test methods have been developed in an attempt to reproduce many of the most common system level EOS/ESD events (IEC 61000-4-2, ISO 10605, etc.). But one must note that while the ESD test methods have been designed to generate repeatable and reproducible results, they cannot address the full range of real world ESD events. Even with each of these stress tests there are still known issues with real world fidelity, test fixturing, etc. that need to be addressed. Therefore to obtain a better perspective we need to address the following issues.

1. What is the meaning of system level ESD robustness?
2. Do the system level tests adequately mimic the environment that a component on a board would encounter in the field?
3. What is the correlation between system requirements and returns from the field?

4. How are proper control methods implemented for the system?
5. Is the IEC 61000-4-2 stress method, which does not directly stress input and output pins, sufficient or do we also need to address the stress at the ports as done e.g. in ISO 10605?
6. How do we prove that the IC ESD design can protect a board?
7. What are the concerns for system level ESD vs. IC level ESD?
8. When is it better to place protection at the IC level? When is it better to place it at the board level?
9. What are the considerations for design speed versus cost effectiveness for the different design scenarios?
10. Under what conditions does crosstalk between signal lines which are directly stressed and other lines, either within a wiring harness or on a circuit board, become important?
11. Why are system level requirements increasing? What is the impact on IC ESD design capability?
12. How do we arrive at a safe and practical strategy that is useful for the electrical/electronics industry?

1.3 Problem

As cited below, concerns about failures of products in manufacturing and in the field have often led system manufacturers to take their own initiatives, whether effective or not:

- Implement increasingly more ESD robust system/board level design practices, perhaps partly because of more demanding RF functions. That is, RF signal integrity requirements are becoming more demanding, forcing OEMs to specify EMC functionality very strictly
- Require increased ESD tolerance from the suppliers of the ICs placed on the board (even if they only apply for the external pins one still needs to define and understand how these pins are categorized)
- Perform EOS/ESD testing using system level test methods
- Implement improved static charge controls in the manufacturing environment

These issues and strategies consequently have led to the following trends in system level EOS/ESD:

- Increased system level EOS/ESD performance targets which often leads to the same target for the component
- Continued requests for fewer on-board components: due to cost constraints driving the reduction of discrete ESD protection elements along with the drive to reduce parasitics in high speed lines
- Increasing competition as a result of expectations to provide more integration and higher performance in components
- Increasing expectations from board designers that IC components must self-protect once in a system

- Increasing difficulty for IC component designers to understand and target a customer's system level EOS/ESD requirements and then translate these requirements into actual pin by pin stress on the IC component
- Increased misunderstanding between system/board designers and IC providers

Based on the trends listed above, it is clear that improving the overall understanding of system ESD protection and establishing more productive dialogue between the IC supplier and the System Board Manufacturer has become crucial.

1.4 OEM Requirements

This "productive dialogue" of communication between the IC supplier and the System Board Manufacturer forms the first step towards improvement in the system level ESD design practice. The most important topic to address in this white paper is: "What do OEMs need?"

The obvious answer would be OEMs want solutions that work. The next question is then: "What are possible approaches to get working solutions?" This is where clear communication of expectations versus performance of the solutions becomes critical. These issues naturally become more confusing when multiple suppliers are involved in the same product. We realize the challenge for OEMs is always to supply solutions at a lower cost to their own customers. The question also arises on what the OEMs expect from their IC suppliers to assist in the design of ESD robust systems. There is inevitably a tangle of interests that need to be filled. To properly address these issues and arrive at a clear solution, a more efficient methodology is needed. One of the main objectives of this white paper is to explore a new approach beneficial to both suppliers and system board manufacturers.

1.5 System-Efficient ESD Design (SEED)

We introduce the concept of System-Efficient ESD Design or SEED. For the design of an efficient system many clarifications are first needed.

1. At best the IC ESD levels provide insufficient information for any system ESD design since IC level tests do not reflect what the pin experiences during the IEC ESD event.
2. An understanding of the stress event seen by the internal pin is paramount to design the system protection.
3. Thus, System-Efficient ESD Design (SEED) can only be achieved after a thorough understanding is obtained about an IC's pin interactions in the system along with the transient behavior of the pins during ESD stress.
4. For such an approach to be applied, efficient characterization methods like TLP data (ANSI/ESD STM5.5.1-2008 Electrostatic Discharge Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level) would be needed to analyze the IC pin and system interaction.

By demonstrating such a new concept it becomes apparent that:

- High levels of HBM protection are not necessary for system ESD design nor do they guarantee ESD-safe system design. Indeed, IO performance requirements may limit the ESD HBM levels that may be obtained.

- While the HBM ESD levels generally accepted for IC handling need to be reduced to a more realistic value, robust system ESD design targets can still be obtained as long as the interactions between the ESD stress and the full system design, including integrated circuits, are understood and addressed in a systematic manner.

1.6 System Definition (Internal Pins versus External Pins)

As mentioned earlier, an optimum system design would first involve defining which pins of an IC may be affected during the design for system protection. Consider first a simplistic representation of a part of a PCB as shown in Figure 3. More importantly, the pins attached to the signal buses connecting several PCBs would be critical since they would be exposed during repair. Obviously, pins attached to external connectors like a USB port are also critical for system ESD. It is worth noting here that although the inter-chip pin connecting one IC to the other IC may not see any coupling during unpowered conditions, there is always the possibility that during a powered condition there would be some coupling that may have to be taken into consideration.

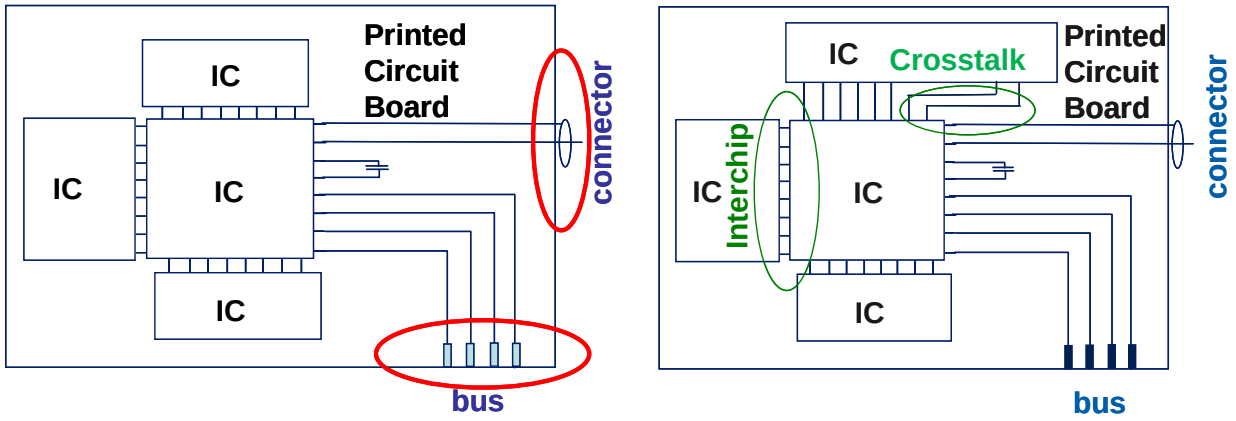

Figure 3: Classes of pins for specific system level ESD considerations including external and inter-chip coupling.

As a second example, consider a more detailed case as illustrated in Figure 4. Here the system design approach must consider the pins and ports where the ESD zaps are indicated. Even with these considerations there is also the uncertainty about the internal pins and if they do see any remnant energy pulses. Can they also get by with the minimum ESD levels that are required for IC handling? At best the IC ESD levels provide insufficient information for any system ESD design since IC level tests do not reflect what the pin experiences during the IEC ESD event. A more detailed analysis is still pending for Part II of the white paper.

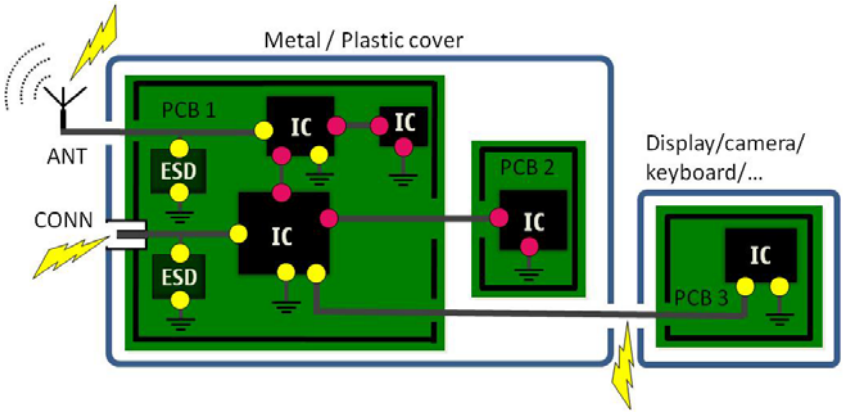

Figure 4: A wired system design with designation for external ESD threat.

In summary, the dialogue between the system builder and the IC supplier can only be improved through a thorough understanding of each type of system to know which types of pins would be susceptible to ESD events and therefore require close attention to system level design protection.

1.7 General Approach and Outline

In order to present the details of this white paper, we have formulated a strategic flow that will give the reader a solid understanding of the current state of knowledge of system level ESD robustness and define test steps that must be taken to develop and implement a highly successful design practice. We start by defining the current practices used for testing system protection performance (Chapter 2). This will be followed by a review of known system test failures (Chapter 3). Once this background is established we then present what the OEMs need and should expect from their IC suppliers (Chapter 4). This will then bring us to the review of common misconceptions that high levels of IC ESD performance will improve system robustness to ESD when tested to the known system level tests (Chapter 5). Dispelling this misconception will be the first step toward better insight into OEM requirements which will yield systems with good ESD immunity without overdesign of integrated circuit external pins. Based on this we will describe the methods of system ESD design that will be most compatible for customer needs and for the suppliers to be able to deliver these requirements (Chapter 6). Finally, we will summarize our findings (Chapter 7). Part II of this white paper will flesh out our proposed design strategy and focus on soft failures.

This document is only Part I. As mentioned above, a sequel to this white paper, Part II, will be documented at a later time. As a preview, the second part will deal with more details on EMC related system design. It will construct a framework of types of soft failures and root causes, followed by a reference methodology for the IC system design. The eventual goal will define the required design targets for system level ESD protection as a whole.

Chapter 2: Test Methods and Their Field of Application

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2.0 The Basic System Level Test: IEC 61000-4-2

The basic system level ESD test method is described in [1]. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. The document states that it relates to equipment, systems, subsystems and peripherals, without further defining them. Its scope and description clearly indicate the purpose: to test electrical and electronic equipment that may be subjected to ESD from operators directly or from indirect discharges from personnel to adjacent objects [2]. The scope further describes that the document is a basic reference method and that product committees, users and manufacturers are responsible for appropriate use and severity levels. The document explicitly recommends those groups to consider adopting the method where appropriate. This chapter will discuss several such initiatives, which resulted in formal procedures or standards. Also many companies, vendors and OEMs, have adopted their own internal qualification procedures, often inspired by the published standards and common practices.

The first ESD test method was identified as Human Body Model. It was originally generated in two different spark gap conditions, both of which were called HBM. One ESD discharge came from the bare finger of a charged human, while the other discharge was from a metal rod held in the hand of a charged human. The discharge current was measured with a sensor in the center of a large metal ground plane. The two discharge characteristics had significantly different electrical characteristics. The discharge between the finger and a metal is reflected in the IC level ESD test method Human Body Model. The discharge between two metal electrodes became the IEC 61000-4-2 test standard. It is a more severe current discharge than the HBM Test and is presently generated from a hand-held unit sometimes identified as an ESD gun. To avoid reproducibility issues a contact discharge method was added to the air discharge method. Note that this type of discharge does not reproduce the characteristic spark associated with ESD discharges. Concerning the current shape measurement for ESD generator calibration, contact discharge mode is recommended. No clear relationship between contact and air failure voltages is expected: "*It is not intended to imply that the test severity is equivalent between tests methods*" [1].

The original IEC specifications were chosen based on measurements made with 500 MHz – 1 GHz oscilloscopes and a current sensor of unknown time domain / frequency domain response. Although the methods and reproducibility have been improved over time, this does not imply that the method covers all ESD events that may happen in practice. Real ESD events may, for example, have much shorter rise times, especially at lower voltages.

Measured waveforms that meet the specifications are shown in Figure 5. The only IEC specifications for system level current are peak current, rise time and the ratio of current at 30 ns and 60 ns to the peak current. A historic concern in the IEC 61000-4-2 test simulator is that there are no specifications for electromagnetic radiation emitted from the gun. The latest revision of IEC 61000-4-2 contains a considerable Annex which describes the radiated phenomena and provides test engineers with guidance for recognizing and dealing with radiated effects. In order to perform contact mode testing, an internal switch is used in the ESD simulator. This switch is usually a relay designed to provide clean switching operation and a good current waveform with a smooth, fast rise time. Unless controlled, this rise time would be on the order of 600 ps or less. IEC 61000-4-2 calls for a rise time of 0.8 ns +/- 25% which means the rising current must be slowed down to be compliant, and this is typically done by controlling the parasitic inductance and capacitance to free space near the tip of the simulator. This fast rising current in conjunction with parasitic and real components produces a radiated field, the characteristics of which are highly dependent on a simulators' physical design.

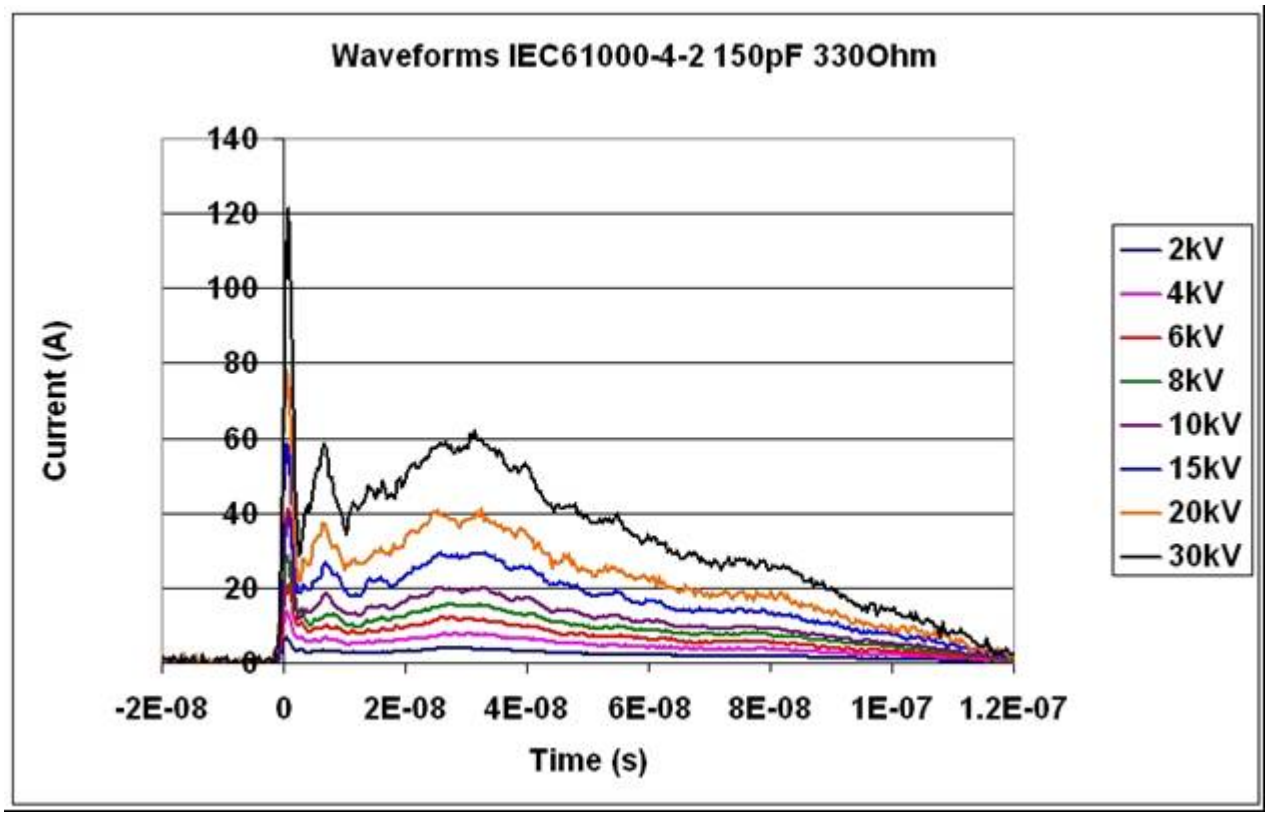

Figure 5: Measured waveforms of contact discharge from an IEC 61000-4-2 ESD gun on the prescribed calibration target

2.0.1 Rationale and Procedure

As mentioned above, the method targets direct and indirect ESD events between a person and a piece of equipment. The waveform described in the standard consists of 2 distinct regions; a sharp, short first current spike, followed by a slower, longer and smaller discharge current. The first peak supposedly represents the discharge through the tool that the person is using, while the slower part represents the discharge of the body through the length of the arm. From the same

reasoning the stress locations are also defined. Direct discharges are applied to metal locations accessible to persons during normal use of the equipment, but NOT to maintenance and service points (such as battery contacts) and the contacts of connectors with a metallic shell. For the latter the reasoning is that in any real life situation, the discharge will be to the grounded shell. Most of the above cases are stressed with contact discharge. Only insulated covers and connector pins with a plastic shell are stressed with air discharge. This is summarized in Table 1. Indirect discharges are always done by contact discharge to a coupling plane. Bleeder resistors (470 kΩ) are used to prevent charge built-up for multiple discharges.

Table 1: Stress location and mode for direct discharge

Case	Connector Shell	Cover Material	Air discharge to:	Contact discharge to:
1	Metallic	None	-	Shell
2	Metallic	Insulated	Cover	Shell when accessible
3	Metallic	Metallic	-	Shell and cover
4	Insulated	None	a)	-
5	Insulated	Insulated	Cover	-
6	Insulated	Metallic	-	Cover
Note: In case a cover is applied to provide (ESD) shielding to the connector pins, the cover or the equipment near to the connector to which the cover is applied should be labeled with an ESD warning.				
a) If the product (family) standard requires testing to individual pins of an insulated connector, air discharges shall apply.				

2.0.2 Failure Criteria

The recommended classification in [1] is as follows:

a) Normal performance within limits specified by the manufacturer
b) Temporary loss of function or degradation of performance which ceases after the disturbance ceases. Equipment under test recovers its normal performance without operator intervention
c) Temporary loss of function or degradation of performance. Recovery requires operator intervention
d) Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data

It is clear that several of those categories do not relate to physical damage, but rather to system upsets. High-speed energy that leaks (conducted or radiated) into a system can cause upsets in circuit operation with false or error information attached to digital signals. Thus, the test identifies the effectiveness of system shielding to prevent or minimize the amount of high-speed currents which get inside a system to develop errors on signal lines. Especially in the case of safety-related systems, those types of fails are much more relevant than the failure criterion normally associated with device level ESD testing.

2.0.3 Typical Requirements

IEC 61000-6-1 [3] and IEC 61000-6-2 [4] prescribe general requirements for products in a residential and industrial environment, respectively. With respect to ESD there is no difference between the two variants. The tests must be carried out in a well-defined and reproducible manner, and they must be carried out in the most susceptible operating mode expected during normal use. The standards prescribe 3 performance criteria:

a) **Performance criterion A**: The apparatus shall continue to operate as intended during and after the test. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer, when the apparatus is used as intended.

b) **Performance criterion B**: The apparatus shall continue to operate as intended after the test. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer, when the apparatus is used as intended. The performance level may be replaced by a permissible loss of performance. During the test, degradation of performance is however allowed. No change of actual operating state or stored data is allowed.

c) **Performance criterion C**: Temporary loss of function is allowed, provided the function is self-recoverable or can be restored by the operation of the controls.

These standards prescribe that equipment meets performance criterion B for 4 kV contact and 8 kV air discharge according to IEC 61000-4-2. Note that hard failure is not mentioned in these standards.

2.0.4 Exceptions

This section describes system level ESD situations which are often encountered in practice, but do not fit the standard as defined in [1].

I. Connector Pins

Although [1] clearly states not to stress connector pins with a direct contact discharge, it is common practice in many companies to do so. Therefore semiconductor suppliers receive requests to deliver components and ICs to let the system survive this kind of stress. Very often it is not well specified how exactly to arrange the connections. If not specified by the requester, an appropriate way to get repeatable results is to implement a configuration as described in [6]. In some cases, such as with (mini-) USB connectors, it is not possible to connect the ESD gun to the connector pin. In such cases it has been suggested to remove the connector and discharge directly to the signal wire or to insert a conducting wire in the connector and discharge to this wire. Obviously the connection to and the properties of the wire may influence the results.

II. Devices and Components

It is obvious that the system level ESD standards are NOT intended to be used for testing single components or ICs. This even holds for the dedicated components, the so-called ESD diodes, which are added on PCBs to let the system meet the requirements. Nevertheless the semiconductor industry has been confronted with request to prove that ICs are ‘IEC-compliant’. Approaches to accommodate such requests are addressed in Section 2.2.2.

III. Printed Circuit Boards

Most system level standards do not specify tests for PCBs. Practically speaking; they are often treated as modules or sub-assemblies, if ESD tests are performed.

IV. Sub-assemblies (modules)

This has always been a gray area in the European EMC Directive [7]. As originally written, the directive only applies to "apparatus", or finished complete products put on the market in the EU. The latest version modifies this by stating that certain components or sub-assemblies should also fall under the directive in certain circumstances. Specifically, it states that a component or sub-assembly intended for incorporation into an apparatus (finished product) by the end user which could either generate or be susceptible to EMC, ***does*** fall under the directive.

That means that items such as video cards, hard drives, or sound cards that a consumer could purchase, take home and install in his or her computer must be CE marked, which in turn means they must be tested for EMC, including ESD.

The basic standard, IEC 61000-4-2, does not give any guidance for testing such products and is open to interpretation. However, if one cannot perform ESD tests as specified in IEC 61000-4-2, the use of other methods is allowed as long as those methods and the reasoning behind using them are clearly documented.

Testing sub-assemblies has two basic problems – what points are tested, and how is the sub-assembly powered or should it be powered at all.

Test points:

From the standpoint of the manufacturer, making sure the product will survive normal handling by the consumer is probably the biggest concern. The consumer is likely not familiar with ESD control procedures, and probably doesn't have a wrist strap or any other means of ESD mitigation. As a result, any part of the sub-assembly is likely to be involved in a discharge in the un-powered state. A cautious manufacturer will probably perform tests to any point on the sub-assembly likely to be handled by untrained personnel. Test levels selected are likely to be in line with those established by product or generic standards for the final product.

Powering the sub-assembly:

In order to test to IEC standards, it is necessary to have the unit powered and operating in a normal manner. This presents some problems and raises a number of questions: If it is installed in an operating system for testing, test points may not be accessible; if installed on extender cards or via cables, is this a valid test since the proximity of the sub-assembly to other parts of the system, shielding and housing may affect the test results. Testing the sub-assembly on a jig will raise the same questions.

Equipment manufacturers are using the three basic methods mentioned in the above paragraph; depending on experience with the testing and the ability to access a sub-assembly installed in a system.

Testing an installed sub-assembly:
If testing can be done on an installed sub-assembly, it is likely the most realistic test possible. However, it only works if test points are still accessible after assembly. In a product like a desk top computer testing a video board or sound card for ESD may still be possible when the side covers of the main unit are removed. One must also make sure it's only the sub-assembly being tested and failures aren't due to radiated effects on other assemblies in the main unit. Some manufacturers use a "golden" unit, which has well understood ESD immunity characteristics so that a failure or upset in the sub-assembly being tested can be distinguished from any other possible failure or upset.

Testing using extenders or cables:
If test areas are not accessible when the sub-assembly to be tested is installed, other methods must be used to both power and exercise the sub-assembly. Extender cards and/or cables can be used to bring the sub-assembly outside the main unit and allow access to test points, but this introduces potential problem that the tester needs to be aware of:

-Cables and extenders add inductance in all lines to and from the sub-assembly, which for purposes of ESD add significant impedances between the sub-assembly and its mainframe.

-The additional impedance reduces any ESD currents that may flow from the affected sub-assembly into the mainframe and increases the susceptibility of the sub-assembly to the radiated effects from the ESD test.

Testing in a jig:
Problems similar to those found when testing with cables or extenders also exist when testing with a jig. Once the sub-assembly is removed from the main housing, the effects of an ESD event can be modified considerably for the reasons noted above.

Summary:
Several methods are commonly used for testing sub-assemblies for the effects of ESD. Although from the manufacturers' point of view handling is a big issue, IEC is **only** concerned with the effects of ESD during operation. Since testing sub-assemblies to IEC standards requires the unit to be operational, it is often necessary to test with unit covers removed which reduces shielding, or with the sub-assembly at the end of a cable or in a jig. In this case exposure to radiated fields and added inductances may significantly alter the ESD susceptibility characteristics of a product.

2.1 System Level Test Methods Based on IEC 61000-4-2

2.1.1 ISO 10605:2008 Road Vehicles [8]

The recent automotive ESD standard, ISO 10605 'Road Vehicles - Test methods for electrical disturbances from electrostatic discharge' [8] includes several test methods detailed in the IEC standard 61000-4-2:2008 with direct and indirect test discharges. It also includes the similar functional performance status (4 classes comparable to classes a-c of [1], while c is split into 2 distinct classes, neither of which allow permanent damage) after tests as well as the calibration test methods. However, several differences between both ESD standards remain. One particular application is the discharge on a coupling structure that provokes coupling to the cable harness. This test is intended to simulate the effect of an indirect ESD to a cable inside cable harness in a car and is detailed in Annex F of [8]

I. Differences Compared to IEC 61000-4-2

The automotive ESD standard ISO 10605 presents test methods for the electronic modules integrated in the vehicle. ESD tests are performed in two conditions: un-powered condition and powered condition, in which the battery is used.

As a consequence, this automotive ESD standard specifies connecting the ESD generator ground to the coupling plane, which acts as the battery ground or the chassis of vehicle. The IEC standard 61000-4-2 in contrast specifies connecting the ESD generator to the reference ground plane. The coupling plane is connected to the ground plane with 2 x 470 kΩ resistors (used to prevent charge built-up for multiple discharges). This is illustrated in Figures 6 and 7.

The automotive ESD standard uses both contact and air discharge modes, while the contact discharge mode is the preferred test method in the IEC standard 61000-4-2.

The ISO 10605:2008 does not specify an upper level of stress voltage. However, the ESD generator characteristics shall be in the range from 2 kV up to 15 kV for contact discharge mode and from 2 kV up to 25 kV for air discharge mode. This can confuse vehicle manufacturers, which sometimes require a 15 kV contact and/or 25 kV air discharge. The IEC standard 61000-4-2 details the preferred range of voltage levels from 2 kV up to 8 kV for contact discharge mode and up to 15 kV for air discharge mode.

A significant difference is that the automotive ESD standard has multiple RC discharge networks, whereas the IEC standard uses a single RC discharge network. The specified capacitance network for [8] depends on the location of the electronic modules in the vehicle. Obviously severity of testing depends on the RC network. Table 2 summarizes the test parameters detailed in both standards.

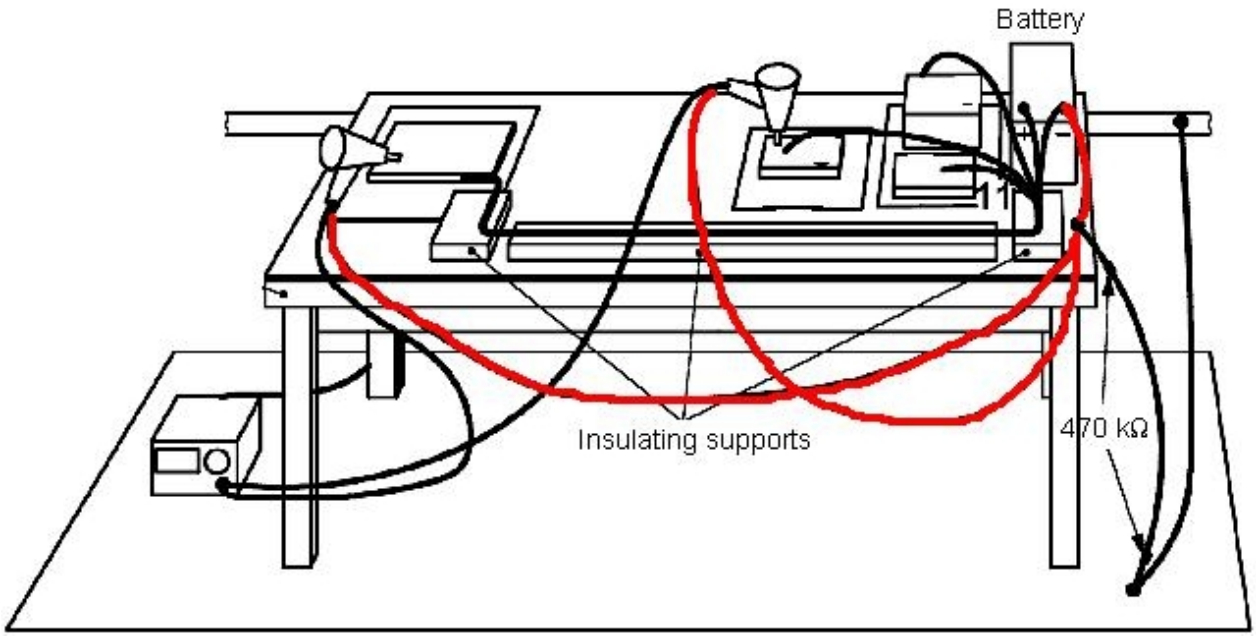

Figure 6: ESD test bench for powered condition from ISO 10605. The ground connections of the ESD gun are highlighted in red.

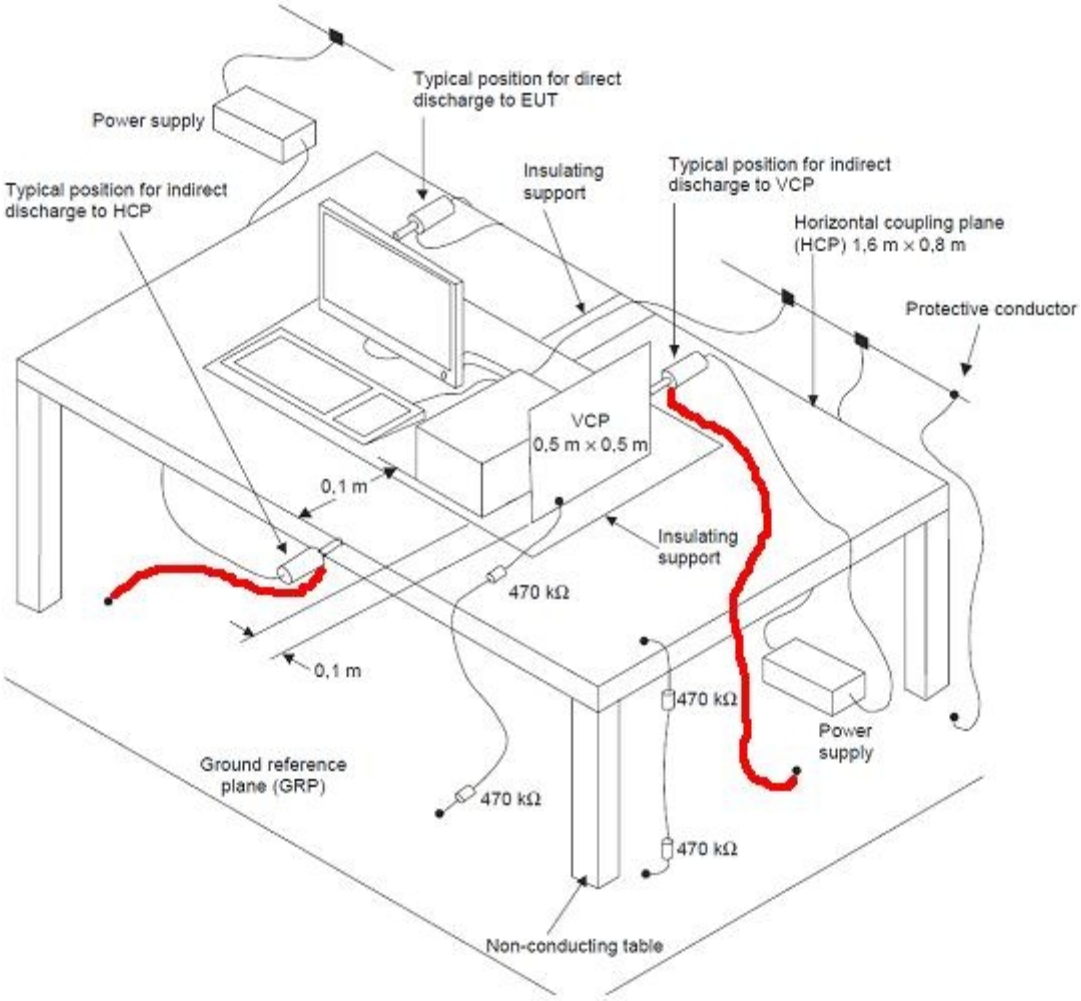

Figure 7: ESD test bench for powered condition from IEC 61000-4-2. The ground connections of the ESD gun are highlighted in red.

Table 2: Test parameters of ISO 10605 [8] and IEC 61000-4-2 [1]

Standards	***ISO 10605***		***IEC 61000-4-2***	
Parameter	Contact	Air	Contact	Air
Output Voltage	2-15 kV	2-25 kV	2-8 kV	2-15 kV
Interval Time	Minimum 1 s		Minimum 1 s	
Polarity at each stress voltage level	Positive and negative		Positive and negative	
Network Capacitance	150 pF/330 pF		150 pF	
Network Resistance	330 Ω/2000 Ω		330 Ω	
Number of Discharge pulses	Minimum 3		Minimum 10	
ESD Generator Ground reference	Battery ground		Earth	
Test conditions	Unpowered/Powered with battery		Powered	

II. Consequences

Using multiple RC networks with both un-powered and powered conditions implies a large quantity of samples for testing and it dramatically increases the test time. It has a significant impact on designers/producers for the costs of testing the electronic modules.

The severity of test depends on the RC module network used to create the direct discharge from any point to the ground of the ESD generator. Both peak current and total energy of the discharge can vary considerably compared to the standard IEC waveform. Since the network mainly affects the second peak of the pulse it is expected that test results for different networks relate to each other for hard failures, because of the Wunsch-Bell relation. For the system-upset type of failures this relation is less clear. The standard leaves room for interpretation as to which network needs to be used in which situation.

The automotive ESD standard has a low impact on the test equipment suppliers. They are able to propose an ESD generator with the entire RC discharge network.

2.1.2 DO-160 for Avionics [9]

DO-160, Environmental Conditions and Test Procedures for Airborne Equipment, is the basis for virtually all environmental testing done on non-military avionics equipment. For military avionics, a large part of DO-160 is being incorporated into a forthcoming revision of Mil STD. 461. DO-160 contains test procedures for a number of environmental conditions and Electrostatic Discharge (ESD).

The purpose of the ESD test is to determine the ability of avionics to withstand an air discharge electrostatic event. Because of the very low humidity experienced in high altitude aircraft, air discharge tests are done to 15 kV to any surface of a box that can be accessed by a person. At each location, 10 pulses of each polarity are done and the results recorded.

Although IEC 61000-4-2 includes testing to 15 kV air-discharge, most products don't need to be tested beyond 8 kV for compliance purposes. For avionics, however, 15 kV is the ONLY test level. The discharge network is the same as that used for IEC testing and the specified air discharge tip is identical to that described in IEC 61000-4-2, so in reality the differences are the test voltage (15 kV air discharge only) and the evaluation of the test results.

The compliance requirements appear vague on the surface:
"Following application of the pulses, DETERMINE COMPLIANCE WITH APPLICABLE EQUIPMENT PERFORMANCE STANDARDS, unless specified otherwise."

But the result is actually very similar to IEC failure criteria because the result of a 15 kV test might be acceptable for one box, but not for another. For example, an upset or re-set of critical flight controls during an ESD event is not acceptable; however, the need to re-set the entertainment system due to a 15 kV ESD event is perfectly acceptable. Hard failure of any box at 15 kV is unacceptable; as is any failure that poses a safety hazard. What is allowed is determined by the nature of the box being tested under DO-160, but specified by a product standard in the IEC world.

It should be noted that aircraft and equipment intended for use in aircraft are specifically excluded from the EMC Directive [7].

2.1.3 ISO/IEC FCD 10373-6 for PICC (Proximity IC Cards)

This standard [5] is an example of an interpretation of the generic standard [1] for a specific group of products. The standard is about credit card-like products that contain an IC, which may or may not have external contacts. Examples are banking-cards containing a chip with external contacts or contactless identification cards. The method prescribes the use of a normal ESD simulator as specified in [1].

The method prescribes that a standard sized card is divided in 4 by 5 equal test zones. Other sized cards (e.g. e-passports) are to be divided with a 1 cm x 1 cm grid. Direct air discharges are to be applied successively to each test zone, while the card is positioned on an insulating support on a horizontal coupling plane. If the card includes contacts, the contacts should face up and the zone which includes contacts should not be exposed to discharges. After the test the PICC should operate as intended. The standard does not mention required stress levels.

2.2 Device Level Tests Based on IEC 61000-4-2

2.2.1 Rationale

System manufacturers use the IEC 61000-4-2 discharge waveform to determine the failure level of pins on connector/cable ports. Although the IEC 61000-4-2 is intended only for systems, system manufacturers want assurance that the devices they implement will indeed pass this specification once in the completed system. Consequently, many of them have begun requesting IEC 61000-4-2 test results from devices they design into their systems.

I. Problems Associated with Applying the Stress

Requests for system level tests on devices are typically made for circuitry that is directly connected to external ports or connections. Thus, for devices or components that will be tested using the IEC 61000-4-2, only those pins coming to the exterior of the system are normally tested. These tests are typically performed using contact discharge although air discharge is sometimes used, usually at customer request. Air discharge is not recommended.

Air discharge test results usually add no additional information about the performance of the device in the final system. First, the air discharge test is not as reproducible as the contact discharge test. Second, air discharge testing of the completed system often highlights issues related to the overall shielding or grounding of the electronic system. Since these issues must be addressed at the system level, any air discharge results for individual devices are, in general, not applicable to the final system. Similar arguments also hold for contact mode discharges applied to parts that have a direct conduction path to ground.

Contact mode eliminates some of the problems with air discharge. An ESD pulse is a complex phenomenon that is dependent on environmental parameters. The contact method reduces the number of parameters (mainly the speed and angle of approach, air quality and geometry), ensuring more stable rise-time and peak current. Moreover, with the contact method, the ESD pulse can be reliably delivered to the aimed pin without random sparks to neighboring pins.

II. Problems Associated with Testing for Soft Failures

Product standards that specify ESD testing to IEC 61000-4-2 require that "*loss of function or degradation of performance*" be determined. When testing a device alone it is difficult to determine the operational state of a device, since often the complete system is needed to bring the device to a normal operational state. However, if testing a powered device one can measure voltage/current and determine if something has changed. This is useful as an indication that damage may have occurred, but "*degradation of performance*" may have occurred at a much lower stress level. Therefore, one must be careful ***not*** to assume that a device that passes a stress test, powered or not, will operate properly when tested in a system where "*loss of function and degradation of performance*" is the criteria for pass or fail.

2.2.2 Existing Device Level Test Methods

I. Zwickau

"Zwickau" ESD tests have been developed by the University Of Applied Sciences Of Zwickau in Germany in collaboration with an industrial consortium. The automotive ESD test for bus interfaces, sometimes referred to as the "Zwickau ESD Tests" are specific EMC/ESD tests applied to automotive applications, more specifically on transceivers such as LIN, CAN or Flexray.

A. Applications (LIN, CAN)

LIN and CAN are both communication systems used for vehicles. The LIN (Local Interconnect Network) is a single-wire serial communications system whereas the CAN (Controller Area Network) works in a differential mode at a higher speed. German car makers have described the OEM requirements in [10]. ESD requirements are defined in the EMC parts of the LIN / CAN conformance tests. Two test configurations exist for the CAN: only transceiver and transceiver with CM choke. For the LIN, three test configurations are described: test with transceiver only (no external devices), test with a bus capacitor (220 pF) and test with bus capacitor and indirect ESD coupling (derived for transceiver level from the ECU-test in [8], Annex F). For all cases the failure criterion is a physical (hard) failure (class D). More details are described in [11].

The Zwickau test set-up is similar to the HMM test set-up, which is detailed in Section III, Figure 8. Typical test parameters are as follows: The discharge level is from 1 kV to V_{ESD_DAMAGE}. The discharge voltage step is 1 kV until 15 kV is reached, then the discharge levels are 20 kV, 25 kV and 30 kV. Three positive polarity discharges are applied with 5sec delay, and before each stress a bleed-off resistor is used to discharge the tested Pad. The same sequence is used for the negative zaps. Tests are performed unpowered with a required minimum of three samples. The minimum accepted level is -/+6 kV.

B. Limitations

This test method can be used when results at the board level can replicate the results in the application. It is mainly driven by the European automotive industry. It is limited to transceivers such as LIN, CAN or Flexray. There is no shared document describing the "Zwickau" tests outside the LIN / CAN consortium. It could be replaced by the HMM tests described in Section III, as it is based on similar test procedures. Tests are performed in unpowered conditions; hence it cannot guarantee safe behavior of the system if an ESD zap occurs during normal operations.

II. IEC TS 62228 [6]

This Technical Specification is in fact a formalization of the Zwickau method discussed above. Formally it is restricted to CAN transceivers only. The procedure prescribes unpowered contact discharge, R and C according to [1], while the PCB is connected directly to the ground of the ESD simulator.

The stress levels are prescribed as: discharge voltage levels ranging from 1 kV to the fail level, with a maximum of 30 kV. 1 kV steps are required up to 15 kV, with 5 kV steps at higher levels. A required pass level is not mentioned, but the fail level must be reported. Failure is determined by measurements after the stress that indicates (physical) damage.

III. Human Metal Model (HMM)

Introduction

Workgroup 5.6 of the ESD Association has developed a standard practice for applying IEC 61000-4-2 stress [1] to ICs. This test is called Human Metal Model [11]. The HMM method is based on the Zwickau LIN test [12]. The test methodology is called the Human Metal Model to distinguish it from the well known IC-level ESD test according to the Human Body Model. Note that, unfortunately, some standards (e.g. [8]), refer to an IC-level gun test as an HBM test, although the gun test and IC-level HBM test have nothing in common.

HMM testing is a field under development, in which no single standard is accepted universally. When testing ICs by means of HMM, the test results need to be interpreted with considerable caution, since the IEC 61000-4-2 test was not designed for IC level testing. Test results at the IC level typically do not correlate with system level tests. Indeed, improvement of the IC level performance may even decrease total system performance [13].

When testing a single IC on a special test board, the grounding will typically be different from the grounding in the real application. Many systems have a worst case mode of operation if the IC has a fairly low-ohmic (e.g. capacitive) path to ground. The HMM test differs from the IEC 61000-4-2 test in that the coupling planes associated with the IEC 61000-4-2 have been eliminated. Thus none of the capacitive coupling between the ground plane and the IC under test is present. Redefining the HMM test configuration to be a test where the test PCB is hard grounded to the ground plane of the test setup and to the ESD gun ground to eliminate these capacitances is warranted since the configuration of the final system cannot be predicted. If the DUT is hard grounded to the external ground, the complete IEC 61000-4-2 setup (with ground plane, table and horizontal coupling plane) is not necessary. Instead a simplified configuration (see Figure 8) can be used.

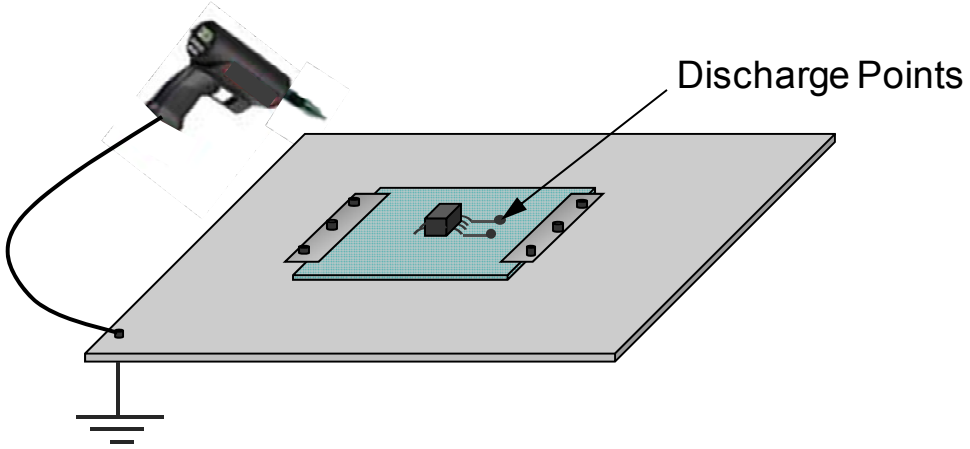

Figure 8: Simplified HMM test configuration

Like the IEC 61000-4-2 discharge, an HMM discharge has two peaks (see Figure 5). The first one is very fast and the second one is slower. The second peak stems from the discharge of the main RC network of the gun. The first peak is generated from the discharge of the tip-to-ground capacitance. Note that (parasitic) tip-to-ground capacitance of the gun tip depends on the orientation of the gun, the thickness of the test board (i.e. distance of the gun tip to the ground plane) etc. Therefore, the rise time and the peak of the initial current spike depend on poorly controlled parameters. The second peak, in contrast, hardly depends on parasitic components and is relatively well defined.

The parasitic tip-to-DUT capacitance produces ringing. The IEC 61000-4-2 waveform is defined to be measured with a 2 GHz oscilloscope or better to give a more accurate view of the ringing in the waveform.

The HMM Standard Practice allows three different configurations for testing. First, the gun tip can be touched to the DUT that is mounted on the test board as shown in Figure 8. The concern is that the electromagnetic field radiating from the gun tip may influence the test results. The second setup is where a hole is provided such that the gun tip can touch the discharge point through a hole in the test plate as shown in Figure 9. The test plate is then placed vertically to allow the gun to touch the discharge point from behind the ground plate. Thus the test plate serves as an EM shield for the DUT. The third setup involves replacing the gun with a 50 Ω pulser. The pulser is connected to the test point on the DUT through a 50 Ω cable. This eliminates the need for a test plate and removes any variability due to excess EM radiated fields from the gun.

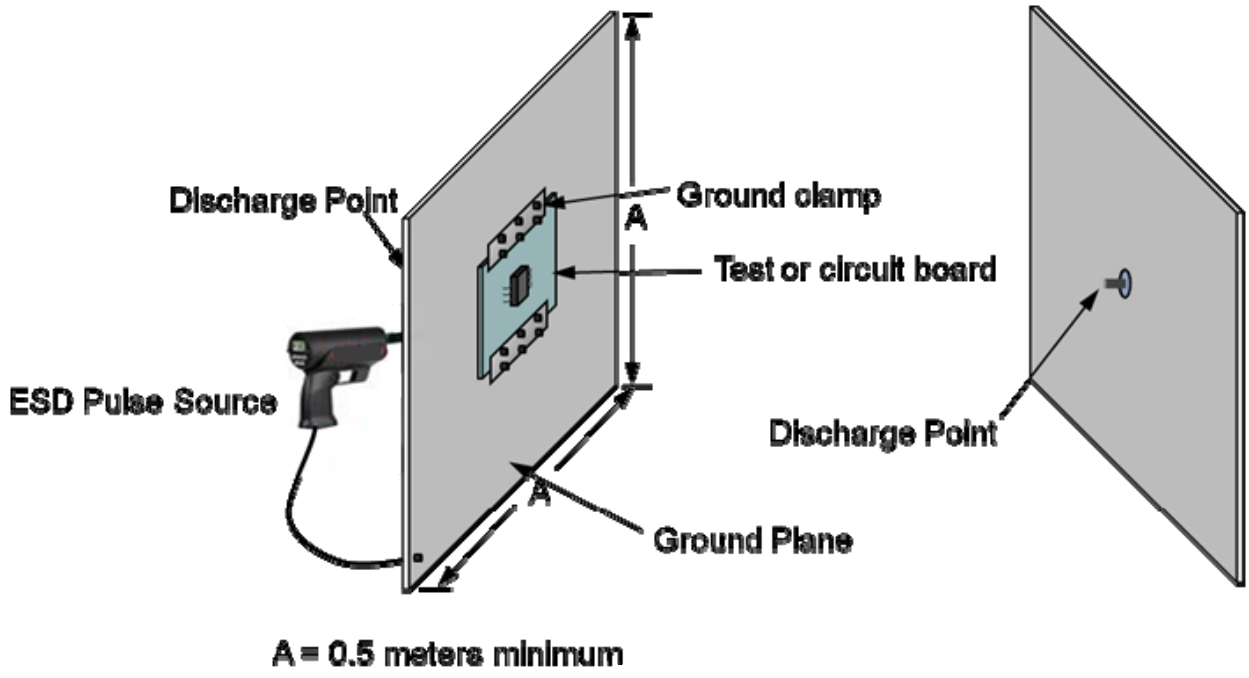

Figure 9: Vertical test plate HMM test configuration

HMM Test Parameters and its Development

As more external components are connected to electronics systems for external data or control, the connecting cables can become ESD charged. When a charged cable is connected to an external data port, the ESD into the external pins of the IC can result in damage. A test was needed to measure the system immunity to these cable discharge events. Since the IEC 61000-4-2 simulators are widely used for system level testing of the effects of ESD, it is a natural extension to use these simulators for testing individual pins on connectors. Although IEC 61000-4-2 specifically excludes the testing of connector pins for compliance purposes, many system manufacturers believe it is necessary to inject ESD events directly into connector pins to determine their level of immunity.

The HMM test injects the test pulse directly into connector pins to determine at what test pulse amplitude damage occurs to the external pins of the IC. The test pulse amplitude which causes external pin damage is an important parameter in HMM device testing. HMM calls for both powered and unpowered testing.

A note on nomenclature: There has been some confusion in the use of the term HBM in the electronics industry. For integrated circuit ESD testing HBM has been used to describe an ESD stress from a human finger. This is the familiar JEDEC/ESDA HBM standard now described by ANSI/ESDA/JEDEC JS-001-2010. HBM has also been used to describe an ESD event to a system in which a person holding a metal tool touches an electrical system, the IEC 61000-4-2 system level ESD test. ESDA Workgroup 5.6 adopted the name Human Metal Model to describe the use of the IEC 61000-4-2 waveform when stressing ICs to distinguish it from the traditional device level HBM test. The IEC 61000-4-2 system level discharge simulator became the HMM

tester as well. While these two tests use the same current waveform, they are applied to different samples, which can cause different electrical sensitivities.

4. Challenges in Achieving Repeatable Failure Levels

The IEC 61000-4-2 standard defines the current waveform when it is discharged into a 2 Ω target. However, the fast-changing gun current causes electric and magnetic fields around the injection point which are not defined. These fields are strongly dependent on the design of the gun and the gun tip. These and other factors cause considerable challenges to obtaining a reproducible HMM failure level.

Challenges between Gun Waveform Variations

An extensive characterization study [14] of nine brands of commercially available system level discharge generators (guns) established that all guns show strong high-frequency components in the radiated electric and magnetic fields. These high EM fields stem from unshielded currents in the generators. Depending on the sensitivity of the device-under-test for these fields, these unintended disturbances may severely impact the observed failure level of the DUT. For 'slow' CMOS circuits which react to frequencies below 1 GHz, a factor of 2 variability in observed ESD failure level may still occur depending on the type of gun used. For fast CMOS circuits which are able to react to 50 ps pulses, the observed variability may even amount to a factor of 5.

Challenges between 50 ohm HMM Pulse Sources and Guns

It has been found that IEC 61000-4-2 generators (guns) generate waveforms with generally poor repeatability and emit electromagnetic radiation around the tip. Alternatively, IEC pulses can be applied through a 50 Ω transmission line system which is adapted from a VFTLP pulser [15]. Since all components in the current delivery path can be made to maintain the 50 Ω impedance, the pulse quality is significantly improved. Furthermore, the increased distance between the DUT and the relays which generate the EM radiation virtually eliminates the EM received at the DUT. The transmission line can be operated at 50 Ω or 330 Ω. The 50 Ω transmission line source is identified at the equivalent IEC voltage to produce the same current waveform threat as the 330 Ω hand held ESD gun. When using the transmission line with 330 Ω impedance, there will be large reflections that need be de-convoluted from the signal.

The relays used in IEC guns inevitably generate small displacement currents prior to the main discharge, due to the increase in capacitance when the relay contacts approach. This very small current, which is not specified in the IEC 61000-4-2 spec, can cause considerable charging of an isolated device-under-test in a regular IEC test. Such a pre-pulse may disrupt the protection of the device against system level discharges, in particular if the protection is slew rate triggered (which is well-known from HBM testing of ICs).

In other cases the pre-pulse may lead to a delay in breakdown of a high-voltage p-n junction, which in turn may lead to a reduction of the safe-operating-area. It has been shown that the pre-pulse voltage varies strongly between different IEC generators, which are another source of irreproducible IEC test results.

The low source resistance of the 50 ohm system eliminates most of the pre-pulse threat in device testing. Using a 100 Ω transmission line (50 Ω both on the high voltage pin and ground) it is

possible to control the biasing of the DUT independently, which separates the effect of the biasing and results in more reproducible IEC test results.

In summary, using a transmission line to deliver the IEC pulse, potentially improves the reproducibility of the IEC test results. The ESDA HMM Standard Practice allows use of either an IEC 61000-4-2 compliant ESD gun or a 50 Ω source capable of supplying an IEC 61000-4-2 current waveform. However, the equivalence of the two pulse sources during device testing has not yet been verified.

Challenges between Testing Devices on a Test Board and in a System

There is always danger in expecting such tests as the HMM test to provide information about how a particular IC will perform once it is in the completed system. One type of testing where this is particularly problematic is air discharge testing. The IEC 61000-4-2 prescribes both contact discharge and air discharge testing to be done on systems. The HMM is only a contact discharge test. Occasionally customers will request air discharge test results from devices or components. However, the air discharge test is an attempt to find unprotected paths for ESD energy to get inside the completed system. When there are air discharge failures, typical solutions include improvement of the shielding within the system or improving the ground paths of the system. These can only be addressed at the system level, and any air discharge results of a particular component have no relevance once the component is placed on a board in the system.

Challenges from Radiation Conversion to I or V on PC Boards

Electromagnetic radiation directed at a conductor will induce currents into the conductor. This is the same result as was found with an antenna converting RF radiation into electrical signals. Radiation near unshielded leads or PCB traces connected to devices will produce currents and voltages on those conductors. Unspecified amounts of radiation with uncontrolled amplitude and time variations can create similar currents in conductors connected to devices leads. The uncontrolled amount and type of radiation can create unknown effects on devices being HMM tested. An additional concern is that the radiation from the gun reaches the test area before the current test pulse arrives. In the real event the current threat and radiation from the discharge begin at the same time. High speed voltages of a few volts can be high enough to turn the external pins of the IC on before the main current pulse arrives. This unusual turn-on condition, which would not occur in a system because of shielding, can cause it to operate in a manner different from what the ESD protection is built to protect against.

The high speed radiation begins to be emitted as soon as the high speed currents begin to pass through the complex shaped conductors used to prevent their passage. The amount of effect that excessive radiation has on HMM device testing remains to be determined. ESDA Working Group 5.6 is presently working on details of the HMM device test to help identify these effects. Round robin device testing will be made on typical devices which can be subjected to the HMM threat. Some answers to these questions are expected in 2010.

2.3 System Level ESD Tests under Development

2.3.1 Cable Discharge Event (CDE)

Low voltage ESD generated during hot plugging can produce Cable Discharge Events which are randomly spaced electrical pulses leading to data, or soft failures. The electrical signal produced by connecting charged cables to a system connector can also damage external pins of ICs, so it is included in this section. Experiments have determined that the amount of voltage which can build up on cables during flexing can be hundreds of volts. Physically long cables however can produce long discharge pulses. This alone can be sufficient energy to damage external pins of ICs which are identified as hard failures.

The discharge which forms between the system and cable metal connector pins forms a low resistance spark. ESD protection clamps typically have low resistance I-V characteristics. When the charged cable impedance is greater than the spark and protection clamp resistance, the discharge pulse will circulate back and forth between the system and an open ended cable. The "ring down" or damped current waveform will dissipate most of its energy charge in the silicon clamp and spark resistances. The mismatch between the source and load for CDEs increases the ringing and adds to the possibility of IC damage. There is a distinct difference between the effects in unshielded vs. shielded cables. In the latter case the location of the discharge – shield or conductor- plays an essential role [16].

The ESDA is preparing a standardized test method to determine failure levels from CDE threats at different amplitudes. Experiments by the members of this working group have identified many different discharge waveforms. Some example waveforms are shown in Figure 10. The test pulse rise time must be identified by a high speed measurement chain. Because the discharge occurs between metal electrodes in cable and system connector pins, the test pulse speed can be very fast at the typical charging voltages found in this threat. Determining the test simulation waveforms will require more experiments with sufficient bandwidth sensors and oscilloscopes to capture the real world event. These highly variable CDE waveforms include multiple waveforms. This standard has been in discussion for over one year, with concerns focusing on providing a test specification which can be used in commercial testers. Because of limitations on participant's time to develop and define a reasonable and effective test method, this information may not be available for many months.

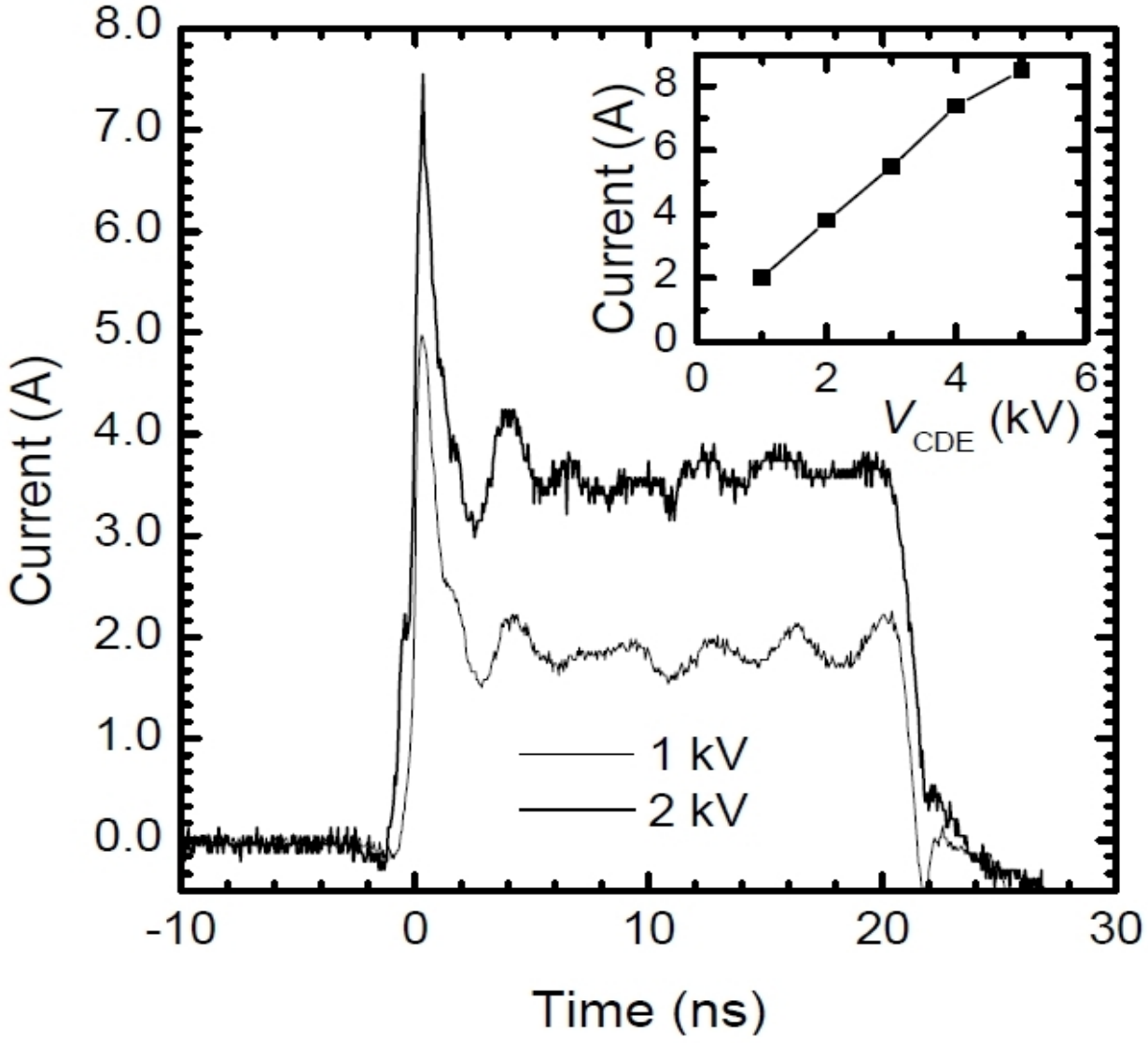

Figure 10: Measured CDE currents for a USB cable with V_{CDE} = 1 kV and 2 kV, respectively. Inset: Current amplitude of the rectangular part of the waveform as function of the pre-charge voltage V_{CDE}.

2.4 Discussion and Conclusions

2.4.1 Failure Mechanisms

The four levels of system response during IEC 61000-4-2 ESD testing, with only one of the levels related to physical damage, indicates that upset rather than hard failure may be the likely outcome. This is also related to the original specification of air discharge only, where the most likely effect would be a disturbance in the ground system; either via a direct arc or through electromagnetic coupling. Note that air discharges were supposed to be done to non-conducting surfaces or metallic (connector) shields. Such a disturbance of the ground potential can easily result in unwanted behavior of the system. However since the disturbance is already at the ground

connection not much energy will be able to flow into internal devices, therefore actual damage is less likely.

When contact discharges are applied to any other location than ground-related points, the energy will be conducted to the ground via a, best-case intended, internal path. This path must be robust enough to sink the current. If this is not the case, fatal damage is likely. If the path is robust enough, the risk of a system upset is still present if the voltage excursions put the system in an unwanted state. This will depend heavily on the complete system design.

In all situations that deviate from the generic description in the IEC 61000-4-2, the dominant failure mechanism depends very much on the test method and type of application. Several example cases are discussed in Chapter 3.

2.4.2 Conclusions

The goal of the IEC 61000-4-2 is to assess, for final applications, the immunity to electrostatic discharges of locations which people have access to in normal use. The second goal is to serve as a basis to derive standards for situations where the IEC 61000-4-2 is not applicable. Several examples have been discussed, the most deviating case being the HMM, where system level pulses are applied to individual ICs. Whereas originally the focus was on 'system upset' as a failure mechanism, the changes to contact discharge and the use of system level ESD on modules, PCBs and ICs have increased the significance of physical damage as a failure mode. Requirements are typically set by users or committees and are inherently very application dependent

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Chapter 3: Proven System Level Fails

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3.0 Introduction

There are many discussions going on in the industry between suppliers and customers about ESD problems which occur in the final system ESD test or in the field at the end-user. Why did the failure happen? Is it due to a HBM-weak device or maybe pre-damage during production and transport of the device or PCB? The root cause for field failures generated during system use (handling or operation) is not easily proven and the confirmation whether it is coming from an ESD or an EOS event is very difficult to establish.

In White Paper 1 [1], regarding HBM, the Industry Council collected extensive data on field failures with a root cause of ESD or EOS and demonstrated little relation to the HBM qualification value of the devices. This evaluation was based on approximately 21 billion devices. A similar study was done for CDM [2]. In both studies the number of field failures has been compared with the number of sold devices and correlated to the HBM/CDM qualification voltage. System level failures are due to various root causes, such as ESD generated noise (to be reproduced by an ESD gun stress), Cable Discharge Events (CDE) during installation of systems or exchange of boards, Charged Board Events (CBE) during installation or exchange of boards, or simply EOS events, that can be generated by spikes on the power supplies, wrong polarity of power and so on. For most of these root causes a test method does not exist, therefore there are no qualification target values.

On the other hand, problems in the field are not only due to damage to devices/systems but also to so-called soft failures like system lockups, where the system is not damaged but its functionality is interrupted temporarily. These problems happen more often than damage but most of them are not reported back to the board and IC manufacturer. Most of these problems are resolved by resetting the device by rebooting or repowering and may often be blamed incorrectly as software bugs.

In the following sections, case studies of actual system problems in the field or during system qualification tests have been collected. The root cause for the failures was evaluated as well as the type of failure. A very interesting point was the question of how system problems are typically solved.

3.1 How to Prove a System Level ESD Fail?

Verifying that a failure coming back from the field is a system level ESD fail can be difficult. Normally when a failure occurs in the field, the end user will send the failing equipment back to the manufacturer for analysis, especially when the failure mechanism occurs often, when the

equipment is large or has safety problems or data integrity failures. The system manufacturer then tries to reproduce the failure in the lab using one of the methods described later in this document. The reaction of the equipment under test (EUT) to ESD or ESD-like pulses can be categorized in four classes:

A. EUT continues to function normally
B. EUT has an upset condition but recovers automatically
C. EUT has an upset condition and needs manual interference to recover
D. EUT is damaged

If case D happens with the same failure mode, the device can be analyzed and the results of the physical failure analysis can be compared with failures found in the field returns. If it is the same, a system level ESD failure can be confirmed.

However, it is not always that straight forward, especially taking into account that soft failures (case B and C) are often difficult to analyze. When the system (or subsystem) comes back from the field, the system manufacturer checks the system and the result is often: “No Trouble Found”. These soft failures are also difficult to reproduce by ESD system stress, since the occurence often depends on the complete test setup. In such cases it is difficult to clearly identify a system level ESD event as the root cause for the field problem. This must be kept in mind when drawing the right conclusions from the case studies analyzed later on.

3.2 System Level Fails – Case Studies

The Industry Council has collected 58 system level case studies. Some studies have completed a deeper evaluation where the failure was duplicated with existing or new engineering test methods in the lab. Others have been reported but never resolved as they only occurred once or twice and did not result in physical failures.

Figure 11 shows the type of failure, for example whether physical damage (blue bars) or a soft failure (red bars) were reported from the field. As can be seen in Figure 11, more physical damage was reported than soft failures, although system manufacturers report that usually soft failures are the dominant failure mode. The reason for this could be that soft failures, while they happen more often, are in general not reported back to the manufacturer. Typically these soft failures are resolved during system development by the system design engineer prior to product launch. This is consistent with the results that EMC engineers from OEMs and EMC test houses obtained while doing qualification tests on systems to IEC 61000-4-2. If soft failures occur in the field (at the end user), they are often not reported back to the system manufacturer. This may be another reason why we tend to see more returns for physical damage than soft failures.

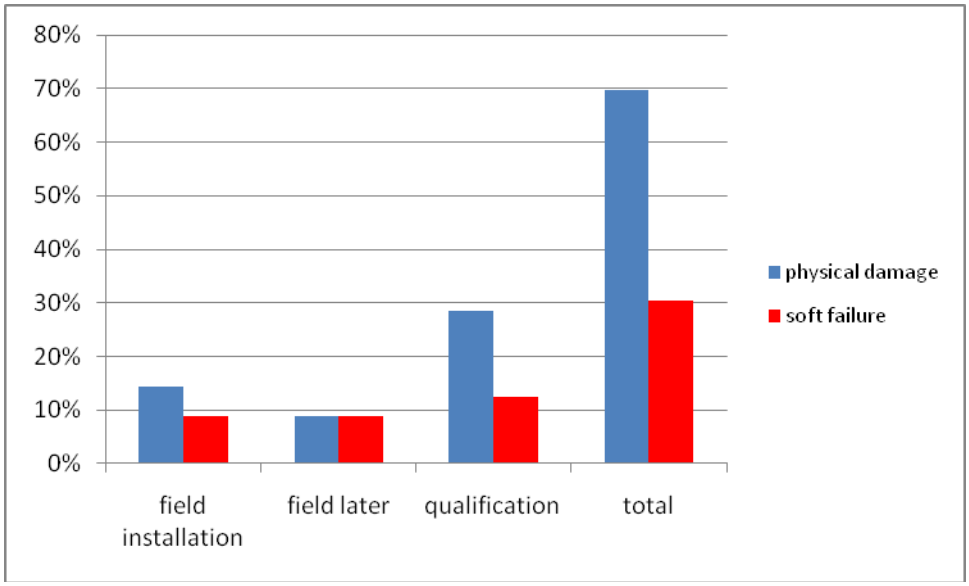

Figure 11: Type of failure with failure location (percentage of cases with given information)

When system qualification tests are performed according to IEC 61000-4-2, discharges are done only to the housing of external connectors as the standard states and not to the product or the pins of the connector. By following the requirements of the standard, hard failures resulting in device damage are very, very rare if they appear at all. However, many system manufacturers not only want to discharge to the housing but to the stress connector pins. Failures during this type of stress are definitely reported back to the IC manufacturer, another reason why we have more hard failures than soft failures in the graph.

Also, the automotive industry does stress the connector pins and therefore has reported more hard failures during qualification than in the non-automotive industry. Nevertheless they experience more soft failure issues but they have difficulty quantifying (and reporting) it. In addition, Figure 11 highlights in which situations failures occurred. Most physical damage was reported during qualification, while in the field, damage occurred mainly during installation. For example, when different parts of a system are connected to each other or when any upgrades are installed. Out in the field, after the system has run a while, the main failure mechanism is a soft failure.

Figure 12 shows the details of the failures; whether the damage or the soft failure had its origin in a CBE, which can happen when two sub-assemblies of a system are mounted together, or in a CDE, which can happen when a system is mounted in the field or when new components are attached. Other root causes can be any Electrical Overstresses (EOS), that can have various causes or true system level ESD events (mainly reproduced by an ESD gun test). Figure 12 shows that soft failures happen mainly during system ESD events with a low chance of occurrence during CDE and CBE and not at all during an EOS event (too much energy). Physical damage is mainly due to EOS and system ESD events even though CBE and CDE may contribute.

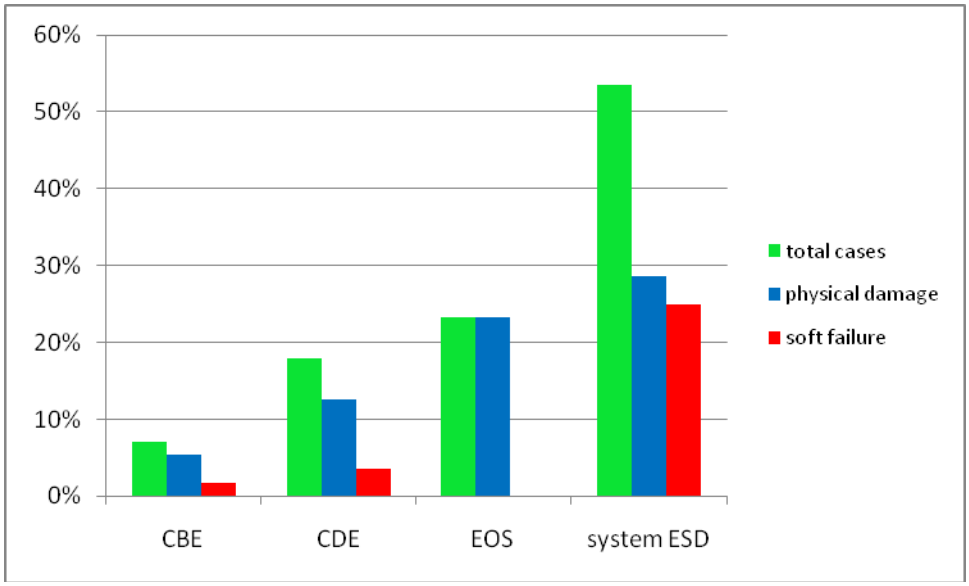

Figure 12: Type of failure – details; physical damage and soft failure included (percentage of cases with given information)

In Figures 13 and 14, the previously shown failures are depicted in relation to the affected pin. Physical damage appears at the external pin or power pin with few exceptions (Figure 14). Only one internal pin was damaged during a CBE event and one internal pin was damaged by an ESD event in the field, where the pin was rather robust with respect to HBM (see below).

For soft failures, more problems are seen on internal pins; but since only two cases have been reported with information about the affected pin, statistics might be too low to draw a conclusion.

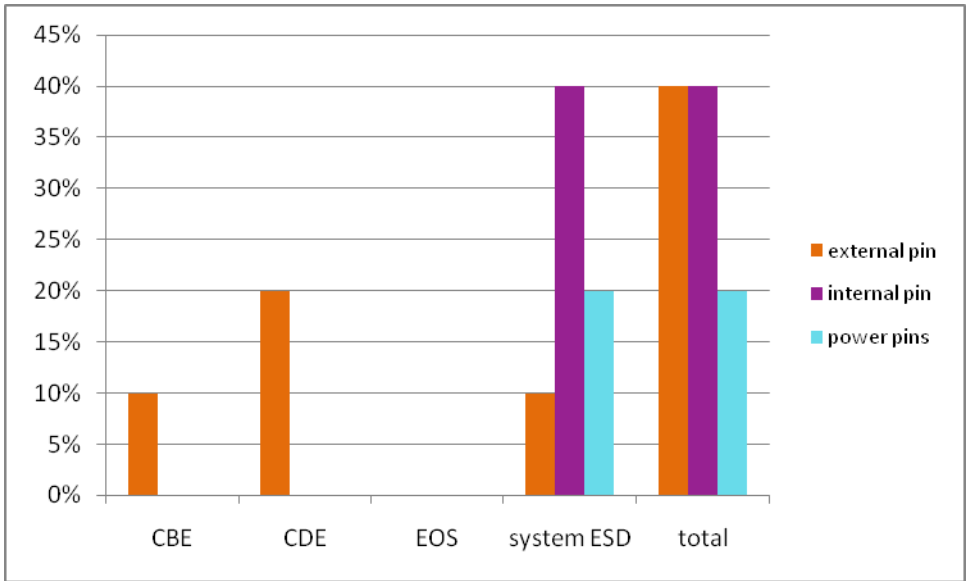

Figure 13: Root cause for soft failures; affected pin included (percentage of cases with given information)

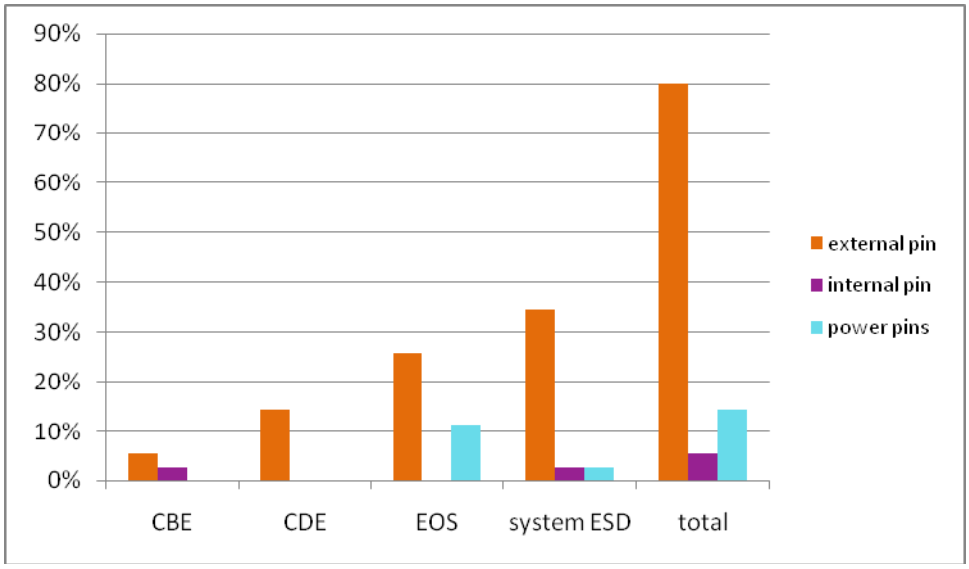

Figure 14: Root cause for physical damage; affected pin included (percentage of cases with given information)

Figure 15 shows how the reported case studies have been solved. Most of the problems have been solved by improving the process in the field, by improving the board layout or the board protection. Only four cases reported that the problem was solved by improving on-chip ESD-protection. All these pins had an HBM robustness of 2 kV before the failures occurred, but since these were pins connected directly to external connectors, this was not enough as one might expect. In one case, improving the HBM robustness on the IC level from 1500 V to 2 kV even reduced the system level robustness from 4 kV to 3 kV. It is also important to note that when failures occur a quick solution is often extremely important, making chip redesign a last resort.

The fourth category of solving the problem, through a software change, was only reported for two case studies, but is a very helpful tool for soft failures. It is especially used in the early test phase of a product.

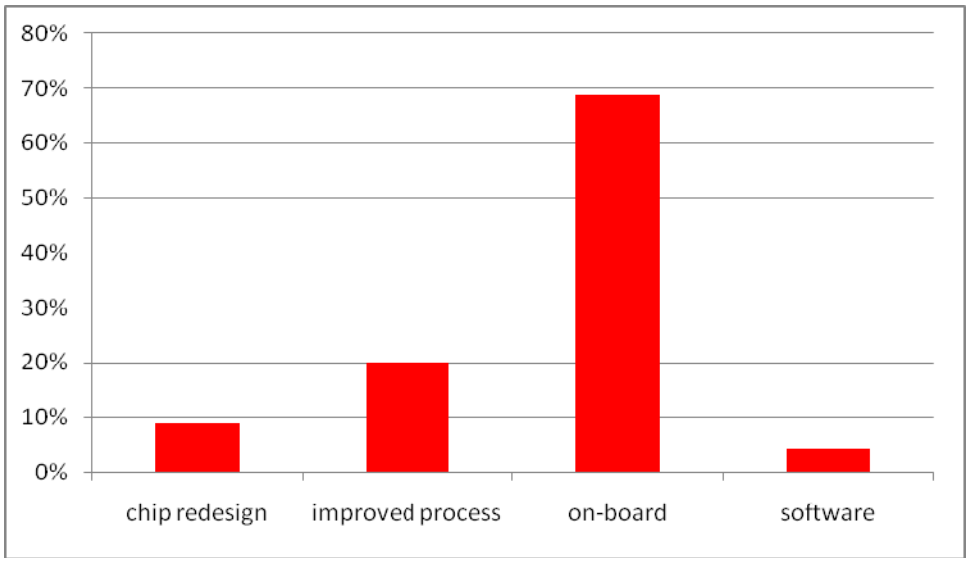

Figure 15: Solution of problem (percentage of cases with given information)

3.3 Detailed Case Study

System Level Damage – Cable

A large server during installation was experiencing failures when the machine was powered on. Parts were replaced and upon receipt back at the factory, the failure was duplicated at the system level. The parts were operational upon leaving the factory.

The installation consisted of several large frames that had to be cabled together to form a system. Investigation indicated that the part that failed and the device on the part that failed had a direct connection to the cable pin. If fact, the cable pin was in the top corner of a multi-connection cable. At this point, ESD was not suspected as a problem as the HBM sensitivity was in excess of 5,000 V.

Further failure investigation showed that all of the failures occurred during the cold time of the year. The data centers where these machines were installed had a very low relative humidity level at the time of the installation. While duplicating the installation, it was found that the outside of the cable could retain a significant charge and thus induce a large charge on the cables inside.

To verify that the cable could cause the problem, a direct discharge was applied to the connector pin at the frame. The failure was duplicated in the experiment. The conclusion was that the cable could charge to a level such that if the corner pin made first contact, there would be enough energy to cause the part to fail.

The fix for this problem was quite simple. These cables had a ground shield that would typically be connected after the cable was connected to the frames. The sequence was changed so the shield was connected first and then the cable was plugged into the system. In this case, the discharge from the cable occurred on the shield and the signal pins did not experience a damaging discharge.

After this change of sequence, there were no additional installation failures due to ESD discharges from the cables.

System Level Upset – Cables

Large mainframe servers have the ability to be upgraded in customer locations. In fact, some of the upgrades doubled the size and capacity of the original machine. One of the features of this upgrade was the ability to complete the mechanical upgrade and verify the upgrade while the customer continued running applications on the installed machine. Only when the machine upgrade was confirmed would the customer have to interrupt his machine to merge the two systems together into one large system.

This was accomplished by a process known as logical fencing in this machine. While the upgrade was being installed and tested, the existing machine would ignore all signals from the upgrade, effectively “fencing” them off. As long as those signals met the expectations, the machines upgrades occurred without a problem.

It was found in a few systems that during the upgrade, the machine that was running had an upset condition that caused it to go off line. The machine had to be restarted and lost the jobs that were

currently running on the system. In addition, it took 45 minutes to 1 hour for everything to go back on-line. There was no damage and no parts had to be replaced; just a restart of the machine.

It was found that the errors occurred during a particular operation where cables were connected from one side of the machine to the other. These were relatively short cables that routed from one system board to another. The cables were Teflon™ coated, a charge was measured on them but the energy level was quite low.

Measuring the discharge showed that the energy level would not be sufficient to damage the parts as the part had a sensitivity level in excess of 5,000 V Human Body Model. However, there was enough charge to send a signal on the line when connected. It was thought that the logical fencing would be enough for the signal to be ignored but the noise that was generated got past the logical fencing and caused the system to be upset.

The solution was quite easy. The Teflon™ coating on the cables was changed to be in the static dissipative range. Since the installation team would be wearing wrist straps, the exterior of the cables would discharge by handling. After this change was made in the cables, upgrades were made without any machine upset.

3.4 Summary

- Failures that result in physical damage are reported more often to IC suppliers than soft failures. Typically, soft failures are resolved after a reset (reboot or repower) and are considered an annoyance and are therefore not analyzed in detail.
- Physical damage failures were found during qualification tests or initial installation while soft fails were found during qualification and post installation.
- Most of the reported fails could be reproduced by an ESD gun test, but CDE and CBE are also systematic problems.
- Most of the problems have been solved on the system side by improving board layout/protection, system level packaging, software or the handling process.
- On-chip improvement was only reported for system pins and typically these failures only occurred during qualification testing or initial system installation.
- Pins affected by system fails are mainly external pins.
- Fails of internal pins are mainly soft failures. Only two occurrences of physical damage of internal pins are reported in the survey. One of them involved a pin with more than 2 kV HBM robustness.

3.5 Conclusion

Different types of system failures due to different types of root causes can be found during ESD system testing as well as in the field. Due to the variety of root causes, there are also a variety of solutions or protection strategies. These problems can normally not be resolved by increasing the device level ESD robustness but rather by improving the handling process, changing the housing of the system (system level package) or the on-board layout. Other ways to solve the problem are to improve the signal to noise ratios, the ability to reject random signals in the device, design recovery methods in the system operating system or machine controlled software (microcode).

Another way of solving the problem in the future may be to develop a systematic and efficient co-design method where the IC manufacturer and the system manufacturer would cooperate at an early stage. This method will be explained later in this document.

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Chapter 4: OEM System Level ESD Needs and Expectations

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4.0 Introduction

Component suppliers must comply with an OEM's needs in terms of functionality, performance, form factor and reliability. The OEM's needs may be supplied by formal specifications or from the component manufacturer's knowledge of the component's end use. In addition, OEMs have another set of implicit requirements for system level ESD: OEMs want ESD solutions that work, minimally affect the functional performance of the system and cost as little as possible to implement. These explicit and implicit requirements are often in contention. A successful solution requires that the OEMs not only understand each component's characteristics, but also how different components work together in the system. This last requirement, particularly in the context of the overall system, is the focus of this chapter. First we describe three hypothetical paths for ESD design. This is followed by a descriptive list of OEM system level ESD needs and a discussion of the realities of current ESD solutions, their physical limitations, and how they measure up against those requirements described in the list.

> Note: The majority of this chapter is written assuming a simple OEM to component supplier relationship which would be expected to exist for a consumer product such as a mobile phone or a laptop computer manufacturer. This has been done to more easily contrast different design approaches without going into the details of an individual industry. Section 4.4 addresses the concern that may exist in other industries such as the automotive industry.

4.1 Paths to ESD Robust Systems

It is worthwhile to repeat the first implicit requirement from Section 4.0; OEMs want system level ESD solutions that work. The ESD needs must, however, fit within the general needs of the system. Due to construction of the system chassis or the physical ports into the system, different parts of the system may be exposed to different levels of stress during a system level test as described in the IEC 61000-4-2 specification. Even in a system where all the individual ICs have robust HBM and CDM levels, the system can fail system level ESD stress.

There are three general paths that can define the way to a robust ESD solution:

1. The components, including integrated circuits, chosen for the system are all inherently robust to system level ESD and the OEM does not need to think about system level ESD at all. (A component is considered to be robust to system level ESD if it is able to survive stress with an IEC 61000-4-2 current waveform to a specified level without physical

damage. Since component robustness to ESD stress is generally only tested for physical failure this path can only be expected to work for hard failures.)

2. Not all components, including integrated circuits, chosen for the system are inherently robust to system level ESD, but component suppliers provide clear rules and procedures for using a set of system level ESD robust and non system level ESD robust components that will produce an ESD robust system.
3. Not all components chosen for the system are inherently robust to system level ESD, and the OEM has to find a solution on their own to design an ESD robust system.

At first glance, path 1 looks quite attractive for an OEMs' system design. However, as discussed below, cost and performance reasons might prevent this approach, which inevitably results in significant overdesign of the ESD measures. Additionally, even a "robust" IC may suffer from soft errors when it is integrated into a full system. Most OEMs would probably find path 2 an acceptable alternative. It is certainly more desirable than path 3. Unfortunately most OEMs would probably consider their current situation somewhere between paths 2 and 3. Board designers are faced with the trial and error approach of path 3, while some experienced designers have developed tools and experience that bring them closer to path 2. Today there are many system level ESD robust components that promise to make systems robust to ESD, but there is certainly no guarantee of first pass success. The development of design tools to use these components and the proper characterization of components will make path 2 a reality. This is what we refer to as System-Efficient ESD Design, SEED, introduced in Chapter 1 and further detailed in Chapter 6.

While path 1 may seem desirable, economic and technical constraints will move the industry to the SEED approach because of its distinct advantages to path 3. This will be illustrated in the following two examples.

First, a high level example - a mobile phone OEM and a IC supplier that provides a hypothetical single chip mobile phone solution. The single chip includes all of the electrical functionality of the phone and is robust to system level ESD stress. The OEM only needs to supply an attractive case, keyboard, display, microphone, speaker, antenna, battery and charging connector. Still a bit of work, but seemingly not a hard design challenge. This may not be the best path for a variety of reasons. The single IC may have grown too large to fit easily into the phone's desired form factor. The single IC may also be too expensive because high cost, state of the art, silicon area may not be used efficiently. There are many reasons for this.

- Filter ICs built on chip use large areas of silicon
  - Off chip filtering may be more economical
- Driver circuits for USB and speakers may not be economical in advanced technologies.
  - Separate driver chips may be more economical
- System level ESD structures are not ideal in state of the art integrated circuits
  - It may be hard to produce low C, highly robust protection in advanced silicon technologies with high doping levels
  - System level ESD structures are large and expensive in advanced silicon technologies
  - Dedicated ESD protection structures placed on the board may be more effective and lower cost than including the protection within a state of the art IC.

These points suggest that multi component solutions may be more economical than a single IC design. Path 1 also assumes that it is possible to provide a single IC that can guarantee a passing ESD testing result. Most system level ESD failures are in fact due to system upset rather than physical damage. Even with a very robust system on a chip solution, the OEM must still design a system's case, connectors and circuit boards to defend against system upset and damage during an ESD event. Even in a single chip solution the SEED approach becomes valuable. The value of the SEED approach increases when multiple components are used.

The next example will deal specifically with high speed integrated circuit IOs. As discussed in Chapter 1 the first priority in system level ESD protection is for IC pins which connect directly with system level IOs. This includes high speed serial interfaces such as HDMI, eSATA and USB 2.0/3.0. Protecting these IOs is a particular challenge. Capacitance budgets for protection components on high speed lines are very low and often very little impedance can be tolerated between the physical cable port on the chassis and the transceiver without degrading the port's performance. Simply adding a stand-alone ESD clamp between the physical port and the transceiver IC might appear to be an obvious solution as shown on the left side of Figure 16 below. However, care must be used in the selection of the component. In addition to selecting a protection component with capacitance low enough that it will not distort signals, the turn on voltage of the protection component is critical. If the turn on voltage of the protection is not lower than the turn on of the transceiver, the protection will not be able to perform its function. This is illustrated on the right side of the Figure 16.

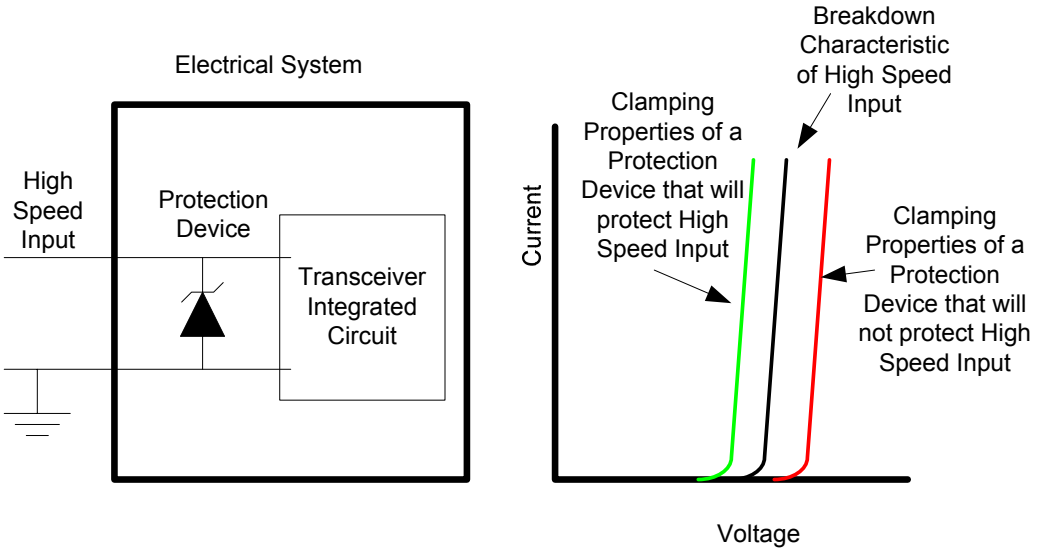

Figure 16: Example of high speed interface system level ESD protection clamping requirements.

This high speed interface example illustrates the three paths to ESD design. In path 1 the transceiver would need to be system level ESD robust, but as we have seen this may not be possible or economically the best solution. In path 3 a protection element can be added, but without knowledge of both the protection component's capabilities and the transceiver's properties there is no guarantee that the combination will produce an ESD robust system. Only path 2, the SEED approach, will guarantee a successful design, since both the properties of the protection and the properties of the transceiver are understood and can be shown to work effectively together.

4.2 An OEM's ESD Needs and Expectations

The challenge for OEMs is to drive down costs and speed up design time while providing current and relevant solutions to their customers. As discussed in the previous section, unless the OEM is happy using a single source vendor and that vendor's components are designed to work in the configuration needed by the OEM, there is no guaranteed single solution. Often, the OEM and its component vendors have to work in an environment where not all the details of the design are available, either because the design is still a work in progress or due to confidentiality concerns. However, there are a common set of requirements that OEMs tend to have that are described below:

Requirement	**Defense of requirement [why it is necessary]**
Components well characterized for their ESD performance	Without knowledge of how a component will perform during an ESD stress it is impossible to predict the component's or the system's behavior during an ESD stress
Good app notes with respect to ESD.	These instructions tell the OEM's engineers how the component's creators envisioned it being protected in a system. This gives color to the standard data sheet table of values such as those discussed in the next section and can define component specific improvements that can be incorporated into the system design.
Software for simulating ESD current flow and voltage levels in a system during an ESD event.	This software will provide the ability to highlight trouble spots and implement fixes during the design phase.
ICs integrated with error detection indicators for reset, latch-up and other soft failures.	Different products use different system designs. The failure modes and levels are different. More robust error detection indicators must be used to allow the processor to refresh the failure functions and locations by software and/or hardware. Software which detects and notifies of upsets during ESD testing can be very helpful.

In the characterization of ICs for ESD it is desirable that OEMs refer to international standards when requesting certain IC properties. For example TLP validation, which is able to provide more detailed information of the IC behavior during stress, is not yet commonly in use [1]. More detailed standards are needed before OEMs can request and suppliers provide information that fully enables "SEED" operation mode.

An OEM cannot, however, always use a single source supplier. A major challenge is when an IC from supplier A will pass the system level ESD test while supplier B's IC will fail. The OEM will often require an improved IC ESD level from supplier B in an effort not to disrupt the product launch schedule. Care must still be used here, since an improved ESD level for supplier B's

product may not solve the problem if the root cause was really supplier B's IC ESD protection triggering at a lower voltage than an off chip protection product.

4.3 ESD Characteristics of ICs and Systems

If it is accepted that system designs will typically be a combination of system level ESD robust and non ESD robust products, what can an OEM reasonably expect from their IC suppliers? The answer depends on how the ICs behave during an ESD event. This may be a more complex situation than it first appears. Today, many OEMs may ask for the IEC 61000-4-2 level of the IC. Moving beyond the fact that IEC 61000-4-2 does not describe how to test ICs, a single survival voltage is a very incomplete description of the system level ESD properties of an IC. Survival of an IC to a particular level of IEC 61000-4-2 stress is usually interpreted as lack of physical damage. This ignores the fact that most system level ESD failures involve a system upset. Even if the system level ESD failure criteria is restricted to physical failure, an IEC 61000-4-2 level sheds very little light on how the product will perform in conjunction with other ICs. For example a system level ESD protection component may be able to survive a large IEC 61000-4-2 stress but may not have a low enough turn-on voltage or on-resistance to protect sensitive circuits. The list below outlines some of the component properties that may be needed to design ESD robust systems.

- Properties for system upset
  - Active components
    - Susceptibility to ground voltage disturbance (possibly on a per ground pin group level)
    - Susceptibility to supply voltage disturbance (also possibly on a per supply pin group level)
    - Susceptibility of IOs to state change due to transients
    - Susceptibility of internal circuits to EM fields
    - Integrated circuits with built in self recovery and resets for lock-up
    - Susceptibility to electric and magnetic field coupling into the IC's leadframe / heatsink etc.
  - Passive (including protection) components
    - Capacitance
    - Inductance
    - Resistance
    - Spark Gap
    - Turn-on voltage and on-resistance
      - TLP I-V curves provide basic knowledge
      - TLP I-V curves with multiple pulse lengths provide additional information
      - Ideally a high current Spice model
- Properties for physical damage to system
  - HMM (IEC 61000-4-2) passing level for ESD stressed pins
    - Full TLP characterization may make this unimportant or it may help define the passing level
  - Turn on voltage and on resistance for ESD stressed pins
    - TLP I-V curves provide basic knowledge
    - TLP I-V curves with multiple pulse lengths provide additional information
    - Ideally a high current SPICE model is also available

The above component properties appear to be enough to give an OEM a good start at predicting system level ESD behavior. However, there is another issue; what is the actual system level ESD stress, and how does it propagate through a system? At this point OEMs, and the electronics industry as a whole, need to take some responsibility. Interfaces need to be developed for communicating the ESD withstand capabilities of ICs to OEMs. How a system level ESD pulse propagates through a system cannot be a IC supplier's responsibility, although use guidelines may be given, especially for suppliers of protection components. The OEM should have the best understanding of how signals travel within a system. 3D ESD simulations are now available but only the largest companies are able to use them due to complexity and cost.

A particular concern is the issue of EM fields causing upset. It is only recently that measurement techniques have been developed to determine the susceptibility of ICs to EM fields [2]. Standardized measurement procedures would be helpful in evaluating susceptibility to EM fields. At present, the level of EM fields that a product or component should be immune to is not well understood. IEC 61000-4-2 compliant ESD guns emit considerable EM fields but the intensity of those fields is not controlled by the IEC 61000-4-2 standard and the intensity of the EM fields emitted by the guns varies considerably from manufacturer to manufacturer. This issue must be addressed by the industry by updating existing test standards and/or creating new test standards.

4.4 Industry Specific Concerns

Specific industries have more complex business models than has been assumed in this chapter. For example in the automobile industry the automotive OEM does not typically deal directly with suppliers of integrated circuits. The OEM typically obtains electrical subassemblies such as radios or engine control modules from a subsystem manufacturer, often referred to as a Tier 1 supplier. It is the Tier 1 supplier that designs the subsystem to the OEM's specifications and obtains electrical components from integrated circuit manufacturers. A main difference compared to OEMs of stand alone devices is that the subsystems are spread all over the vehicle and are connected via a cable harness with around 1000 single wires with a total length of 2 km. Therefore one emphasis is indirect ESD pulsing. Another difference in the automotive business is that automobile assembly and repair is not normally done in an ESD controlled environment. A main concern of the automotive OEMs is the risk of field fails (damage while assembling/repairing, malfunction during customer-use) and the cost impact for the modules. Subassemblies such as engine control modules must be robust to ESD and cannot rely on the automobile to provide physical and electrical protection. Subassemblies and subsystems must therefore be robust to ESD. For this reason, as discussed in Chapter 2, the automotive industry has developed a separate set of ESD test methods which include the stressing of subassemblies and subsystems in both the powered and unpowered states.

This does not mean, however, that the approaches outlined in this chapter and the White Paper do not apply in the automotive industry. The SEED approach has simply moved from an interface and design strategy involving OEMs and electronic IC suppliers to an interface and design strategy that involves Tier 1 suppliers and electronic IC suppliers.

4.5 Summary of Realizable Needs and Expectations

The needs and expectations of OEMs in terms of the ESD properties of ICs is a complex subject. ESD solutions should be designed within the complex constraints of technical needs and

economic necessity. OEMs need detailed information on the properties of ICs when they are stressed with ESD in order to determine how they will perform within a system. OEMs also need to have tools that allow them to predict the system's behavior when exposed to an ESD stress. It is not realistic in most cases to rely totally on IC suppliers to provide a full ESD solution in their ICs. The SEED approach will provide a disciplined and effective tool for designing systems which are robust to hard failures from ESD. The improved understanding of ESD events within systems that SEED encourages will also be important to the understanding and elimination of soft failures as well.

References

[1] ANSI/ESD STM5.5.1-2008 Electrostatic Discharge Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level

[2] Impact of ESD Generator Parameters on Failure Level in Fast CMOS System, Aug 18-22, 2003 IEEE EMC Symposium

Chapter 5: Lack of Correlation between HBM/CDM and IEC 61000-4-2

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5.0 Introduction

System level designers have legitimate concerns about the vulnerability of their systems to ESD malfunction or damage. Design organizations are always searching for the most efficient design techniques for avoiding these problems. In particular, they often try to identify a design platform that can be used across many products, thus minimizing design time and cost. Over the last two decades of EMC design, there has been a significant movement towards pushing design decisions further upstream and to embed re-usable platforms in the design. It was natural that this trend resulted in system designers looking for solutions at the chip level. The idea that at least some portion of ESD "immunity" could be "built-in" at the device level was an attractive option to be pursued. In many cases this meant that the responsibility for finding these solutions was transferred, at least in part, from the EMC engineer or designer to supply chain or component engineering. This transfer was also enabled by the fact that the discussion of ESD effects often blurs the distinction between reversible system level malfunction and actual irreversible hardware (device) damage. In any case, the first impulse then was to target IC ESD ratings as the first step towards "better system level performance", even though there was no evidence for making this connection.

In this chapter we discuss the current limited data on correlation and why using IC ESD ratings cannot be expected to work. We also discuss the relationships among other ESD and similar stress tests and where correlation might or might not be expected. Many references of comparison studies and studies of other "system"-like stress models are included.

5.1 Correlation between ESD Models

It is important to understand what is meant by "correlation". One approach is to look for statistical correlation. To address the statistical definition of correlation one needs to perform testing using the two models in question over a range of products to establish whether there is any useful mathematical relationship between the two models. As of the writing of this document, little data was available to firmly establish the question of correlation on empirical grounds alone. However, the data available can be used to get a sense of whether the position made here - that the models will not correlate – is likely to be true.

In Figure 17, IEC 61000-4-2 system rating [1] and HBM device rating (withstand threshold) (JEDEC A114) [2] are plotted for the cases where they have been reported on the same system. These data points were taken from the larger data collection discussed in Chapter 3. This scatter plot of these nine data points shows no indication of correlation between the IEC and HBM data sets. More data is of course needed to firmly make this point. We can say at this point that the

likelihood of good *statistical* correlation between the IEC ratings and the HBM thresholds of a device is small.

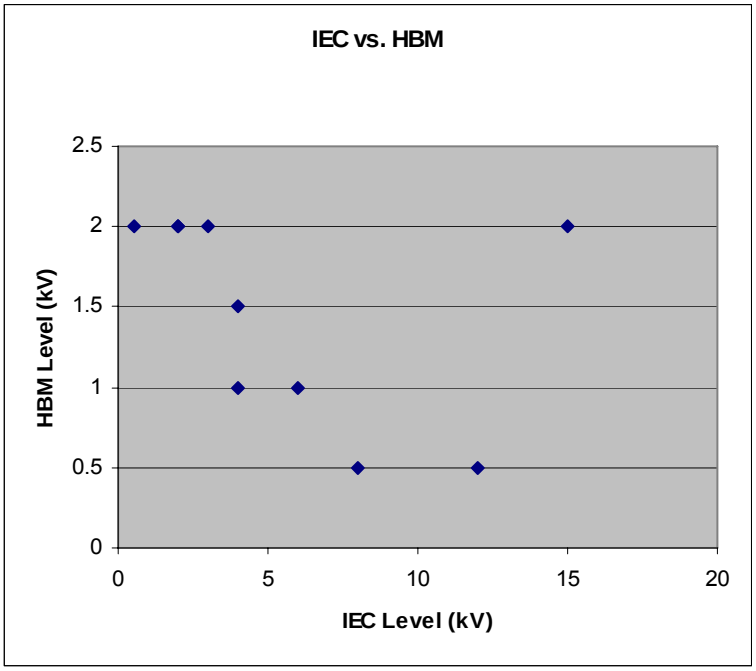

Figure 17: IEC 61000-4-2 System Ratings vs. HBM Device Withstand Thresholds for systems where both have been reported (In some cases only passing levels were available. However, when lower passing levels are reported, it usually means that the failing level was only a few hundred volts higher. This is sufficient for this rough analysis).

These results suggest that the standard HBM rating of a device is not likely to be a useful predictor of system level robustness. This may seem to be a trivial point. However, much of the reluctance to adopt the 1000 volt HBM target proposed in White Paper 1 has been based on the assumption that lowering these targets will result, statistically, in the erosion of system level ESD performance. There are of course other dimensions of correlation that could be explored. There are two device models (HBM and CDM) and there are two main categories of failure or malfunction at the system level (irreversible hardware damage and reversible upset or data transmission errors). It is clear that, in attempting to correlate HBM or CDM to the second category of system failure, one is trying to correlate two entirely different mechanisms. This alone suggests that any "correlation" should be very weak. A slightly stronger case can be made for trying to relate the IC level HBM and CDM thresholds to the relative "immunity" of a system to hardware damage *of that particular device*. However as we shall see even this correlation is likely to be minimal. The following experience is illustrative: the first version of a device passed 1.5 kV HBM, and passed 4 kV in an automotive customer's system. A single pin of the device was redesigned and the part then passed 2 kV HBM, but the part in the system only passed 3 kV IEC and failed 4 kV IEC, and failed on the fixed pin. This pin was protected at the system level by a varistor that had a higher trigger voltage than the IC protection, and the IC protection improvement meant more IEC current could be carried by it and it failed. Experiences such as these demonstrate how counter productive it can be to depend on device-level HBM for system level improvement.

Most attempts to use device level information for system level purposes are based on the HBM. This is due to its similar scope and name and the fact that the HBM thresholds are available for almost all integrated circuits. Even though CDM is responsible for virtually all production-related ESD failures, CDM threshold data is still not universally available. Thus most of the discussion about correlation is centered on the relationship or lack thereof between HBM and the IEC method.

5.2 Differences among Device Level Tests (HBM/CDM) and IEC 61000-4-2

The idea that device level ESD thresholds could provide information about a system level test such as IEC 61000-4-2 probably comes from incomplete understanding and knowledge of how either or both of the methods are actually defined and implemented. In this section we explore the apparent similarities and the fundamental differences.

The impression that the HBM device level test should be similar to the ESD gun based test may be widespread simply because the descriptions of the two stresses in the standards themselves are similar. The original intention of the device level HBM test was to simulate handling (touching) of a device by a charged person while the scope of IEC 61000-4-2 refers to the "electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects" and that it represents "… a [charged] human body holding a metallic object such as a key or tool". The high level schematic descriptions of each model as they are commonly shown are very similar as shown in Figure 18. These representations leave the impression that the two models might only differ in the choices of the RC-network chosen (device HBM: R=1500 Ω, C=100 pF; IEC 61000-4-2: R=330 Ω, C=150 pF) and thus one might conclude that the results of the two tests would be similar. However, a more careful look at the details of the methods shows that this is not the case.

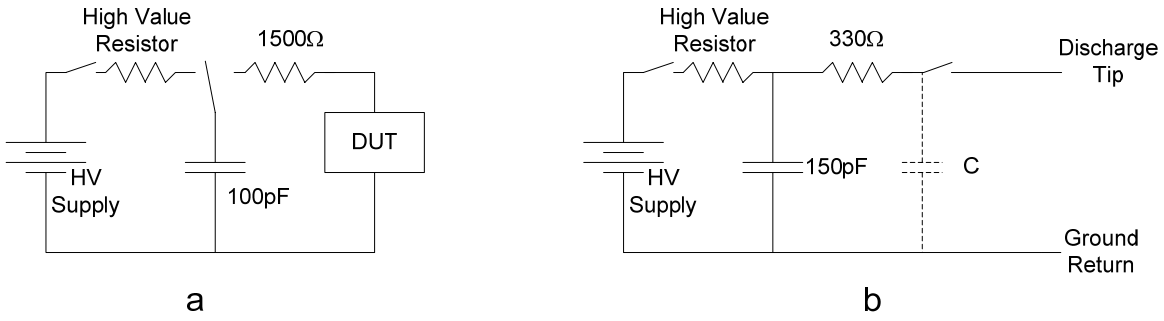

Figure 18: Common simple circuit representations of the a) device level and b) system level methods

5.2.1 Differences in Test Procedure and Threshold Definition

Standardized HBM testing of devices specifies stressing each pin of a device in several configurations where other groups of pins are grounded. This is summarized in Table 3, which is the pin combination table from ANSI ESDA/JEDEC JS-001-2010 [3]. For a typical device there may be hundreds or thousands of different pin / grounded group configurations stressed, each would in general have its own failure level. The device level HBM ESD threshold that is assigned is the minimum of all these failure levels. In practice, devices often are step-stressed and testing is

terminated when the first failure is obtained. Thus, to make a relevant comparison between the device level HBM and the IEC method, one would have to select a pin combination which closely resembles the stressing of the device at the system level. Even if this connection can be made, there are still distinct differences between the stresses as described in the next section. A summary of the differences between the system level and HBM methods is given in Table 4 (originally published in White Paper 1 [4A])

Table 3: HBM Pin Combinations for Integrated Circuits (ANSI ESDA/JEDEC JS-001-2010)

Pin Combination Set	**Connect Individually to Terminal A**	**Connect to Terminal B (Ground)**	***Floating Pins (unconnected) (Must include no-connect pins)***
1	All pins one at a time, except the pin(s) connected to Terminal B	First supply pin group	*All pins except PUT* and first supply pin group*
2	All pins one at a time, except the pin(s) connected to Terminal B	Second supply pin group	*All pins except PUT and second supply pin group*
N	All pins one at a time, except the pin(s) connected to Terminal B	Nth supply pin group	*All pins except PUT and Nth supply pin group*
N+1	Each Non-supply pin one at a time	All other Non-supply pins collectively except PUT	*All supply pins*
* PUT = Pin under test.			

Some other distinctions are important to mention here. The dotted-line capacitance in Figure 18b represents the unspecified capacitance of the ESD gun to its environment. It leads to the initial peak in the IEC standard waveform. This capacitance is not important in the device-level HBM model as the relay position leaves this capacitance uncharged before the stress. The initial current pulse has been shown to produce CDM-like (gate oxide) failures [5, 6, 7]. However, there is no indication that the device-level CDM would be a good predictor of behavior in the system level test. The rise time of this initial peak can have a dramatic effect on the propensity of a system to experience soft errors during the IEC stress. However, since the device level CDM is done on an unpowered isolated device (as is the HBM), correlation to system soft error susceptibility is not expected.

Table 4: Comparison of IC Level HBM (ANSI ESDA/JEDEC JS-001-2010) and System Level ESD (e.g., IEC 61000-4-2, ISO 10605)

	IC level ESD test	**System level ESD Test**
Stressed pin group	Multitude of pin combinations	Few special pins
Supply	Non-powered	Powered & non-powered
Test methodology for 'HBM'	Standardized	Application specific using various discharge models
Test set-up	Commercial tester & sockets	Application specific board
Typical qualification goal	1 ...2 kV HBM	8 …15 kV
Corresponding peak current	0.65 … 1.3 A	> 20 A
Failure signature	Destructive	Functional or destructive

5.2.2 Differences in Pulse Characteristics (Hardware Failure View)

One way to investigate the lack of correlation in failure mechanisms between System Level ESD and the other ESD models is to consider differences in the electrical signature of the model stimulus, namely the rise time, peak current, energy and power parameters of the different models.

The total power and energy of stresses in the total event times of ESD levels was initially described by Wunsch and Bell [8] and extended to the very short (adiabatic) and very long (equilibrium) timeframes by Tasca [9]. The resulting plot of failure power density versus log (time) and the different ESD event representations are shown in Figure 19. Figure 19 represents the entire time spectrum of EOS. ESD is a subclass of EOS events which results from triboelectric charging and is generally characterized by short pulses. However, some ESD events have a very high power density, and can result in EOS-like events even for short duration time scales. Examples of these ESD events (Charged Cable Events, Human Metal Model and Charged Board Events) are discussed in Section 5.3.

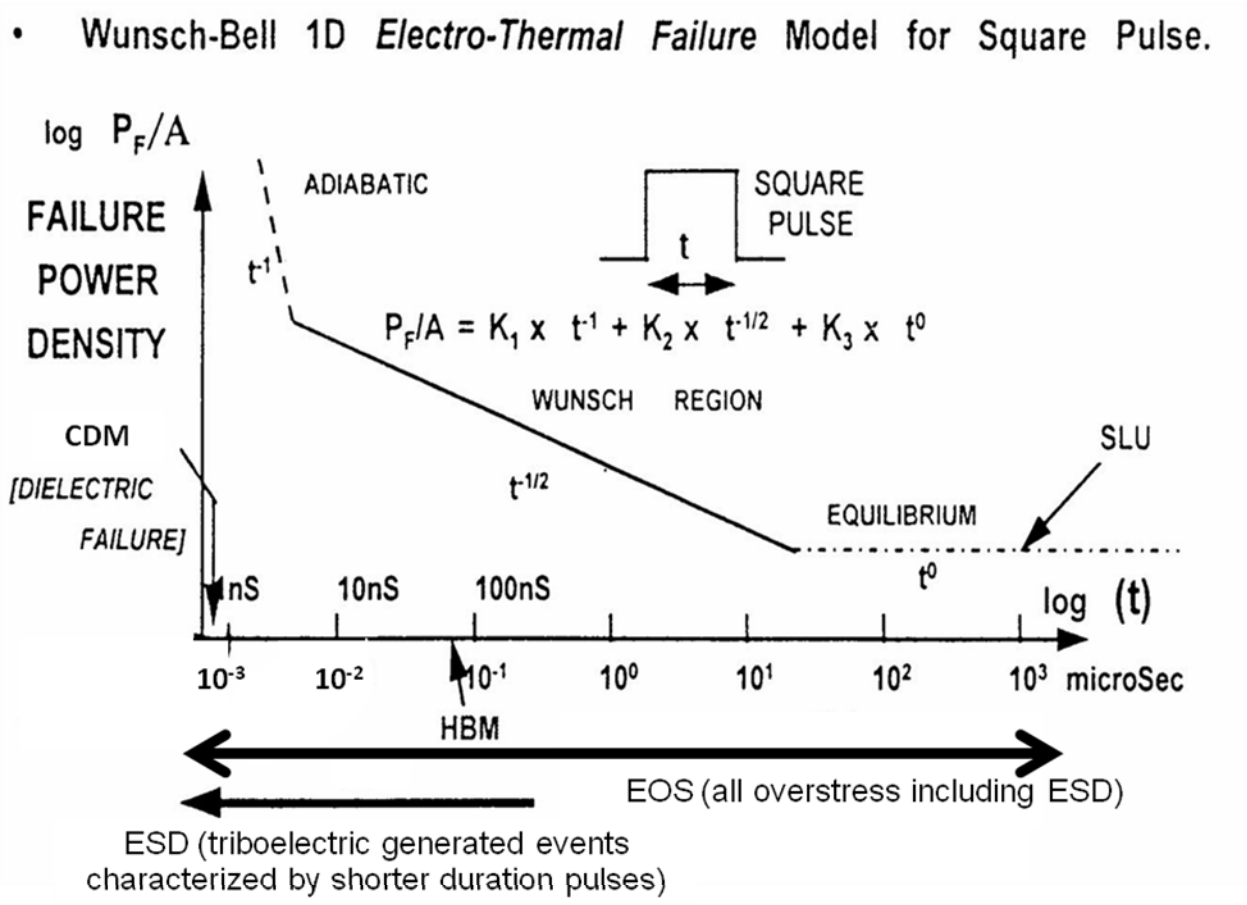

Figure 19: Wunsch-Bell Power Density / Time plot for ESD / EOS level pulses.

The Industry Council on ESD Target Levels authored White Paper 2 on CDM which gives relevant information considering a 1 kV event from each model [4B]. Comparison values for HBM, CDM and IEC pulses from White Paper 2 for a 1 kV ESD event from each model are shown below in Table 5. Total peak current values for HBM and IEC ESD events of this magnitude are 0.67 and 3 A, based on the fixed circuit models for these methods. However, for CDM, which is dependent on the total device size / capacitance, the peak current can range between approximately 1 and 25 A. It should be noted however that the values in this table represent the event through the circuit model itself, and the actual event parasitics below are dependent on the stressed system circuit under test.

Table 5: Comparison of some typical network values and electrical quantities for a 1 kV stress

	C (pF)	R (Ω)	τ (ns)	Q (nC)	E (μJ)	Pavg (kW)	Ip (A)
HBM	100	1500	150	100	50	0.33	0.67
CDM	1-100		1-2	1-100	0.5-50	0.25-25	1-25
System	150	330	50	150	75	1.5	3

One major difference among the models which is not included in the Wunsch-Bell plot is the initial rise time of the measured pulse. The standard HBM circuit model has a specified rise time

between 2 and 10 ns, while the CDM rise time is typically in the range 50 – 500 ps, depending again on the effective device size / capacitance. However, the IEC initial pulse has a rise time of between 0.6 and 1 ns while the secondary larger total energy pulse has a rise time between 10 and 20 ns. These differences are critical to the effectiveness of on-chip protection structures. Most ESD on-chip circuits are dependent on the rise time of the initial pulse for turn on response, in addition to the total power / peak current handling capability. Thus they can be expected to perform differently for different model stresses. Thus when one attempts to use the HBM (or CDM) threshold, even if one has identified the external pin in the system, one is making the incorrect assumption that the protection structures will operate the same over a wide range of rise times. It may be necessary to define a set of waveforms that an IC may be exposed to in a system during an ESD event in order to fully evaluate how the IC will behave and design countermeasures at the board level to prevent failure.

The concept of simulation fidelity has been described by Pierce [10]. Particular ESD events which occur in the field can only be well-simulated if the particular ESD model is precisely described. Thus, when conducting failure-mode analysis and investigating root causes of failure, it is often necessary to adjust the model parameters to produce the exact physical and electrical signatures.

Average power during the ESD pulse through the circuit is difficult to calculate without knowing the effective resistance and peak internal voltage of the circuit ESD path. But a few general comparisons can be made for the IC case from assumptions of ESD path resistance and breakdown voltage.

The HBM circuit model consists of a 100 pF capacitor and a 1500 ohm series resistor. The HBM current results from the resistive divider between the 1500 ohm resistor and the path resistance of the device under test. Path resistances within a device under test may be on the order of 1-10 ohms and device breakdown voltages are on the order of 10V, sometimes more, sometimes less. A peak circuit voltage in this case for a 2 kV HBM ESD event could be in the 10-12V range. For CDM, the resistance varies depending on the circuit area and connectivity to supply and ground. Also, due to the ns-time scale of the CDM event, the dv/dt of the CDM voltage is much higher than HBM, well under a nanosecond, which is very close to the turn-on time of the ESD protection, and the fast ramp results in a peak voltage that is higher for the short CDM time compared to HBM. An approximate in-circuit voltage value / path resistance could be 20 V and 5 Ω for a 500 V CDM discharge. An IEC pulse could take a similar path (in the unpowered state) to that of an HBM pulse, as its stressed and grounded points (IO and system ground respectively) may be similar to that for the IC itself. Assuming this is true, the path resistance would be similar, but the peak voltage would be much greater. The resistive divider from the IEC circuit results in a higher peak voltage (by 4.7X) compared to the HBM pulse at an equivalent voltage (the peak current is greater as well). So peak voltages for the IEC case for the same protection would be much higher (40-50 V) for a 2 kV pulse compared to a 2 kV HBM pulse. This means that a typical IEC pulse, if applied directly to a device, will produce stress far in excess of the level for which the protection circuitry is designed.

However, actual system level testing is even more complicated. To discuss the energy of an applied pulse, distinction must be made between air and direct discharge. In the latter case, a high portion of the energy is injected directly into the *system*. If the pulse is applied to the outer casing, the energy arriving at the board can be greatly diminished by proper shielding and current

diversion techniques, and the energy delivered to the IC will be lower by an unknown amount. For air discharge, the fraction of the energy coming in to the system directly is significantly lower, again by an uncontrolled amount. This is counteracted somewhat by the fact that the specification for air discharge immunity is typically set higher (15 kV vs. 8 kV for direct discharge). However because much of the energy is radiated, there is more chance of stray fields entering the system and reaching board components through other paths. Thus designing robust system inputs, even if focusing only on hardware failure, requires a system approach as is described in Chapter 6.

5.2.3 Differences in Pulse Characteristics (System Upset View)

It is clear that the current waveforms associated with the IEC requirement and the IC specifications differ significantly. The amount of energy in an IEC pulse is much higher than in an IC level HBM or CDM pulse, as is the peak current. In addition, the frequency spectrum is very different. It includes high frequencies comparable to CDM, lower frequencies comparable to HBM and everything in between. But even if the exact applied IEC waveform could be well defined, the waveform reaching the IC in a particular system is usually unknown. Furthermore, the system level test is much more complex than a pin-to-pin case; due to EMC radiation and other coupling effects, both capacitive and inductive, such as “crosstalk”. This means that multiple IC pins can receive spurious stresses more or less simultaneously during an IEC test. This can complicate understanding the system and IC responses greatly.

Frequency Domain and the IC. The frequencies of the applied pulse tend to be lower when reaching the IC because of interaction with the parasitic impedances of the system. In general, the high frequency first peak will be lowered and stretched in time. Likewise, the more energetic second pulse tends to extend in time. These trends are not universally true however, and dependent on board and application.

Switching states in an IC can create sudden redistribution of the system level energy, causing secondary high frequency pulses to arise. One such example is the discharging of a stabilizing capacitance in response to the triggering of a snapback-based clamp. In this case, the fast rise time of the superimposed pulse will not cause any additional issue for the ESD protection, as it happens after triggering. Therefore, the main issue concerning the pulse frequency modulation is the unknown time duration of the pulse arriving at the IC. For high speed pins which can be touched directly that have much less parasitic impedance between the connector and the IC, the high frequency part of the IEC pulse can reach the IC. A closer look at the details of the two peak IEC waveform is discussed in the next section.

5.2.4 IEC Two Peak Waveform as Applied to Chassis Metal

The IEC 61000-4-2 system ESD test method describes a current waveform into a standard target load. This waveform has been described by mathematical expressions and circuit models in professional literature. K. Wang et al [11] have developed a mathematical reference discharge waveform given by

$$i(t) = \frac{i_1}{k_1} \cdot \frac{\left(\frac{t}{\tau_1}\right)^n}{1+\left(\frac{t}{\tau_1}\right)^n} \cdot \exp\left(\frac{-t}{\tau_2}\right) + \frac{i_2}{k_2} \cdot \frac{\left(\frac{t}{\tau_3}\right)^n}{1+\left(\frac{t}{\tau_3}\right)^n} \cdot \exp\left(\frac{-t}{\tau_4}\right)$$

with the following constants

$$k_1 = \exp\left(-\frac{\tau_1}{\tau_2}\left(\frac{n\,\tau_2}{\tau_1}\right)^{1/n}\right)$$

$$k2 = \exp\left(-\frac{\tau_3}{\tau_4}\left(\frac{n\,\tau_4}{\tau_3}\right)^{1/n}\right)$$

and the following parameter values for a 5 kV pulse

i_1 = 21.9 A	τ1 = 1.3 ns	τ3 = 6 ns	n = 3
i_2 = 10.1 A	τ2 = 1.7 ns	τ4 = 58 ns	

References 11-13 also present comparable circuit models for simulating the IEC pulse. Cannigia and Maradei [13] present a circuit comparing results to field simulations and having a distributed model of the strap as in Figure 20 below. The construction of models such as these shows the level of detail that is left out of the superficial description of the models in the standards.

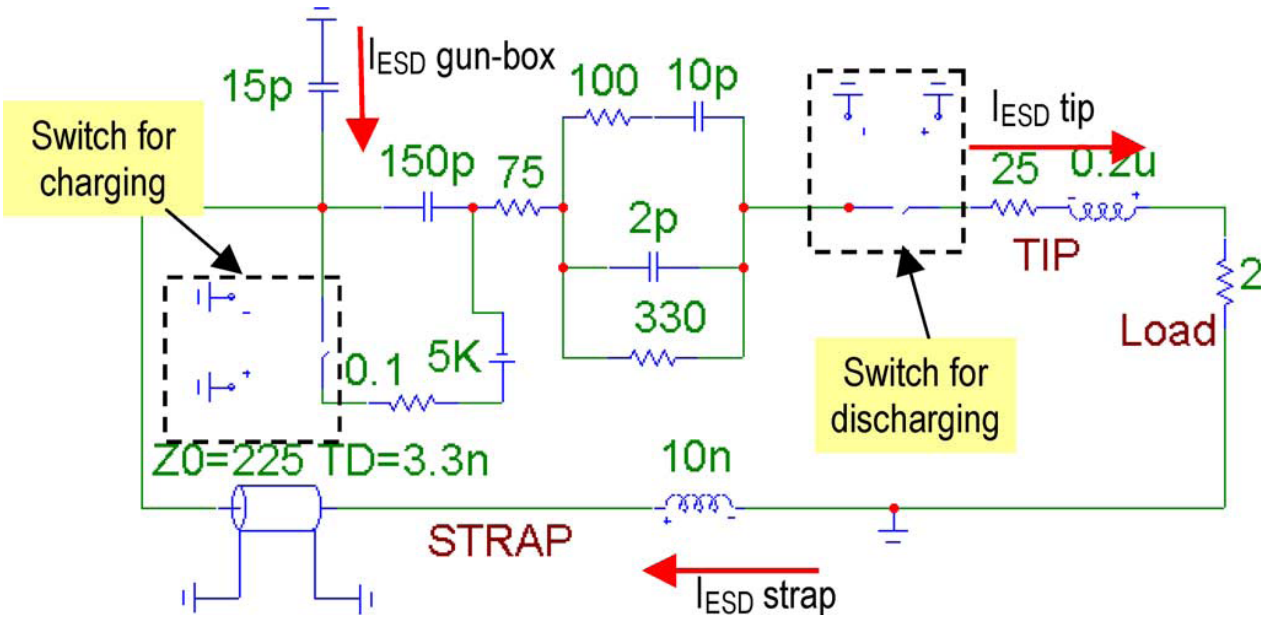

Figure 20: SPICE model of the IEC generator, from Reference 11

5.3 Relationships among Different Possible Realizations of System-Type Stresses

In order to address concerns about the failures of devices in higher levels of assembly and in systems, considerable effort has been applied to create stress models (tests) which simulate specific situations. The intent of these approaches is to simulate real-world environments that the existing models do not. In this section we briefly review the models and methods that are of current interest and where possible indicate how they may relate to each other.

5.3.1 Cable Discharge Event (CDE)

A cable discharge event often originates from a cable being charged triboelectrically. The discharge occurs when the cable is connected to a system and the charge stored by the cable is discharged through a connector pin into the system. Early literature on cable discharge events are included in references [14-16]. Mitigation techniques include ensuring the ground part of a connector is connected into the system first to avoid discharging of the cable onto boards/components inside the system that are electrically connected back to pins on the connector of the system. Other mitigation techniques can involve board-level solutions or chip/integrated circuit solutions. Some details of attempts to standardize a CDE test were introduced in Chapter 2. The rise/fall and pulse width of CDE pulses are very different than IEC 61000-4-2 or Human Metal Model (see Section 5.3.3) type pulses. The CDE pulse width is dependent upon the cable length. The rise/fall times of the CDE pulse are usually highly dependent on the parasitics of the cable and connectors. There has been no correlation to date shown between CDE system level results that can occur from cable plugging and the IEC 61000-4-2 system level results. In addition, there has been no correlation found between CDE results with powered systems and unpowered ESD HBM, MM or CDM levels for ICs. However, there has been some effort to correlate CDE to long pulse TLP (Section 5.3.4). Some insights into CDE and the resultant stresses for shielded and unshielded cables are provided in a recent study [17]. For example, the strong pulse that can occur on the shield of a plugged-in cable, when charged objects are neutralized, is found to produce a fast bipolar induced pulse on the interior lines of the cable. This will have much reduced magnitude but can still be hazardous.

5.3.2 Transient Latch-Up

Transient latch-up can occur when a transient signal is applied to the power supply and/or signal line pins on an IC. The transient stimulus distinguishes this approach from the standard JEDEC JESD78 [18], in which the signal pads see static (DC-like) signals for the current injection test and power supply voltage ramp testing on the supply pins. While the focus of both of these tests is to stimulate CMOS latch-up, almost all reported latch-up problems in the field are likely to be caused by the transient events. Transient latch-up trigger currents/voltages are a function of the pulse characteristics such as pulse width and rise/fall times [19]. Figure 21 shows the typical cross sections of test structures utilized for characterizing external latchup using static or transient triggering sources where both injectors of holes (positive mode external latchup) and injectors of electrons (negative mode external latchup) structures are shown [20].

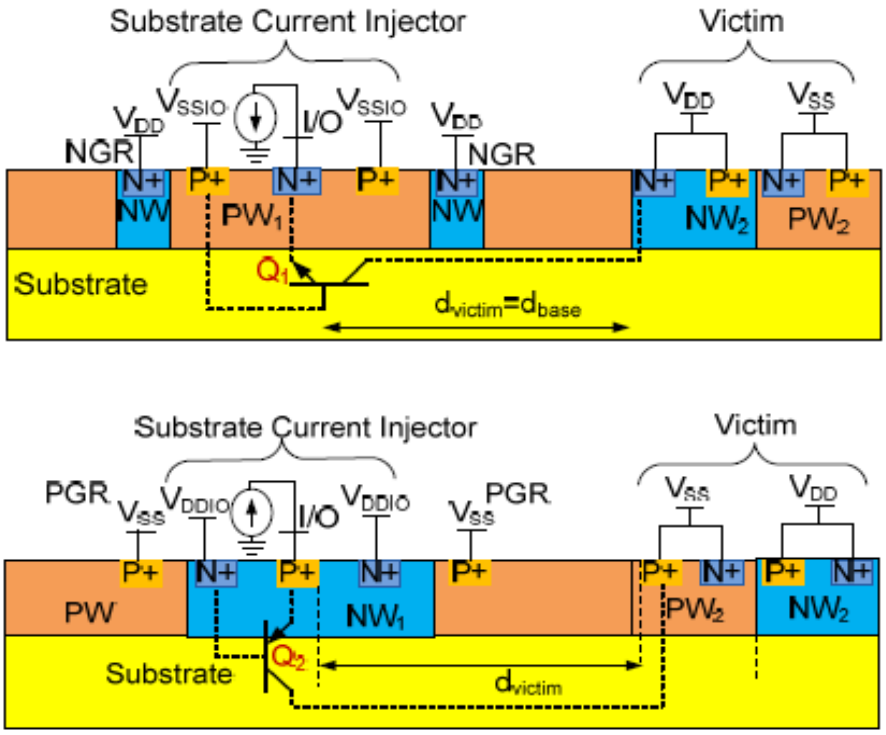

Figure 21: External latchup test structure cross sections

Figure 22 shows the results from negative external latchup testing acquired in a 180 nm bulk CMOS technology node using p-type starting wafers. The data shows the strong trigger current dependence on the applied pulse width for 1us and below pulse widths [19].

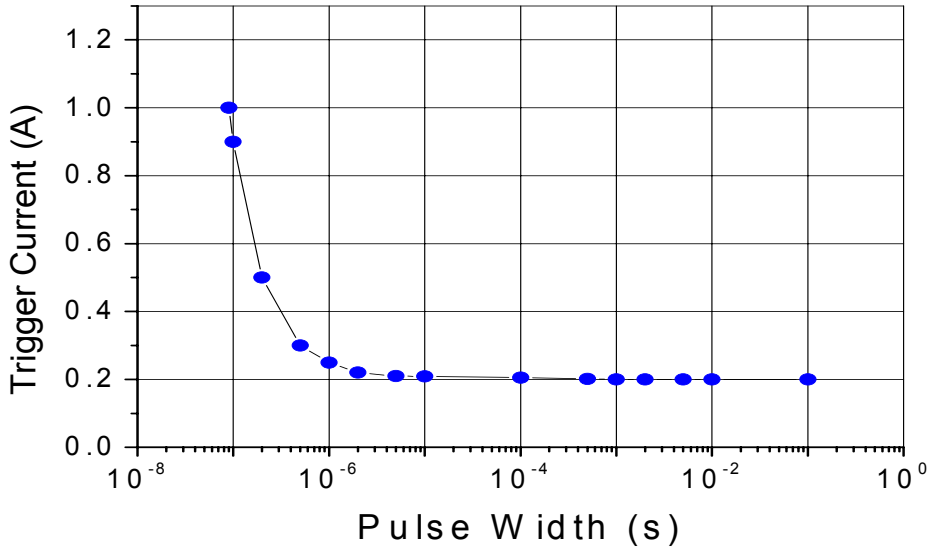

Figure 22: Transient latchup signal pad (negative mode) trigger current vs. pulse width (180 nm bulk CMOS technology node) [19]

More recent work is shown in Figure 23 where positive and negative current injection testing was completed for a 130 nm bulk CMOS technology node [20]. The similar study as shown in [19] was completed for negative mode injection results for varying pulse widths with similar results. In addition, as shown in Figure 23 the work also included positive mode injection results for varying pulse widths, showing very little rise in positive I_{trig} down to pulse lengths of about 20 ns. As seen in Figure 21, the base length of the vertical Q_2 for positive mode, is usually considerably shorter than the lateral base length Q_1 for negative mode, thus explaining the fast response of positive mode. The aforementioned bipolar induced CDE pulse [17] can thus be hazardous unless there is a good p+ collector to raise positive I_{trig}.

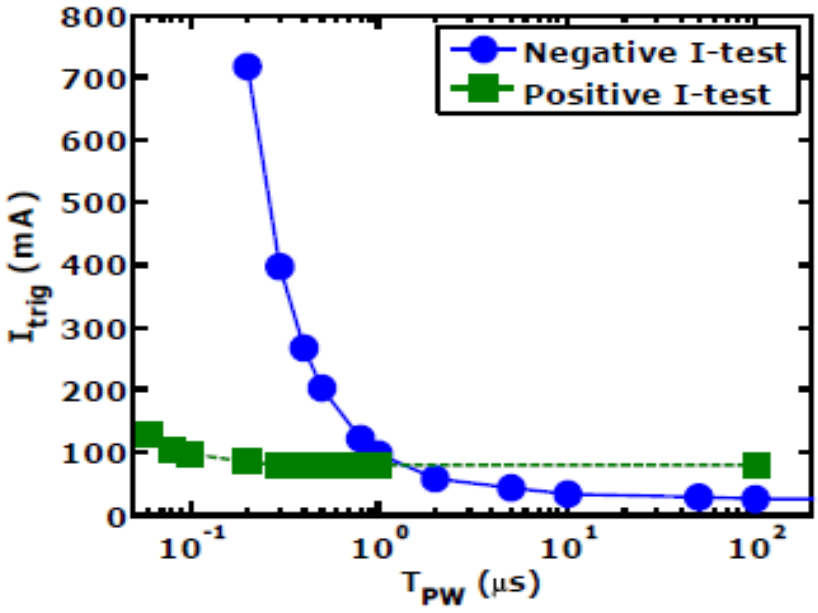

Figure 23: Transient latchup signal pad (negative and positive mode) trigger current vs. pulse width (130 nm bulk CMOS technology node)

Figure 24 shows data acquired using different stimulus sources performing powered latchup testing [19]. The different trigger pulses used have different pulse widths and rise/fall times and give different trigger current values when these pulses are used as the stimulus on the I/O signal pad latchup test (negative mode).

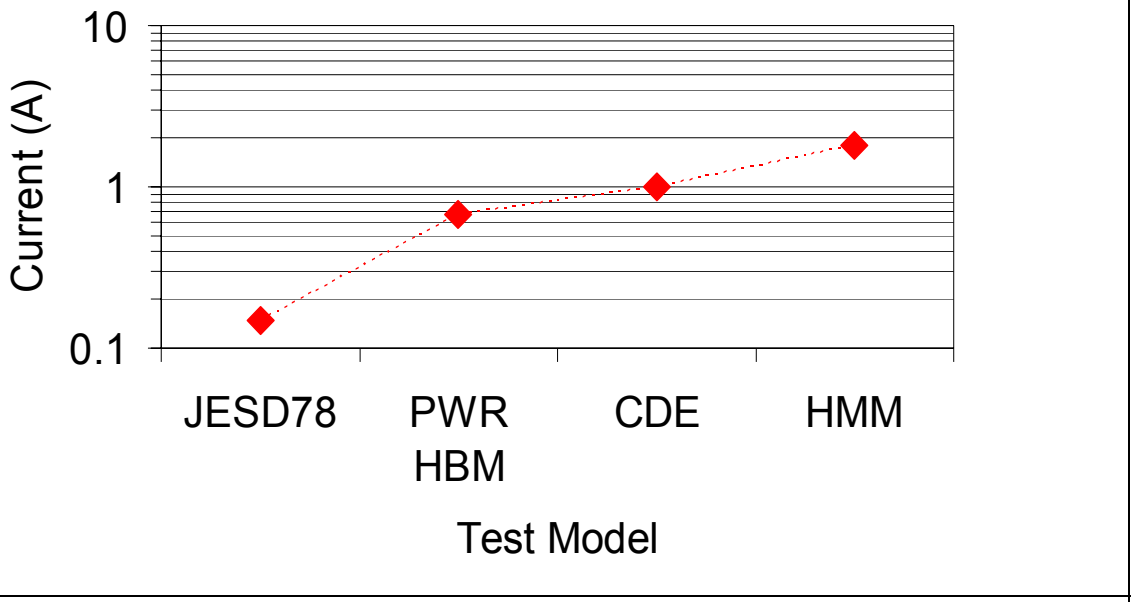

Figure 24: Negative mode transient signal pad latch-up trigger current for different transient trigger sources [19]

One major conclusion, based on a review of published prior work, is that there has been no evidence found showing linkage between reduced ESD targets for HBM, MM or CDM and reduced latchup results [19, 20].

5.3.3 Human Metal Model

We have argued that the standard HBM and CDM thresholds were not good predictors of system level performance. Many system designers and manufacturers have come to accept this fact and have begun looking for a "better" device level test. As was discussed in Chapter 2, many OEMs have begun to require that IC suppliers apply the IEC-defined stress directly to the system external pins of a component, even though direct ESD stress of external system pins is explicitly excluded in the IEC 61000-4-2 standard method. The IEC 61000-4-2 testing of system ports is carefully defined. If the port has a metal shell or cover, contact discharge is to be done to this metal shell, but not directly to the pins. If the port connector has an insulating body, air discharge is to be done to that area of the port. It should also be noted that the ESD and EMI transients from application of this pulse may have an impact anywhere within a system, affecting numerous ICs, and does not permit evaluation of any one particular IC in a system. Additionally, the IEC 61000-4-2 test document identifies several modes of failure, including soft failures, in addition to hard failures. Therefore, it is expected that it will be very difficult to predict the particular pass / fail system level voltage of the IC itself from the system level application of this test.

Round robin testing of this method has begun and is expected to be completed before the end of 2010. If the results indicate the test can be repeatable the standard practice may be elevated to a Standard Test Method. However, this will not change the fact that this procedure is unlikely to be a good predictor of how the IC will react to system level tests according to IEC 61000-4-2.

5.3.4 Extended Pulse Length TLP Testing

There has been investigation into assessing the correlation between the system level ESD pulses and an extended length pulse generated from a TLP tester. TLP pulse lengths in the 400-500 ns range have been used to generate and detect damage and determine if correlation may exist between the voltage of the TLP pulse and the voltage of the IEC pulse. A 2006 study [21] described 500 ns – 1000 ns extended pulse TLP testing to simulate cable discharge events from UTP standard cables on 0.25 um technology ESD structures. The 500 ns TLP compared well with the 56 m cable discharge pulse time of 475 ns in the paper. A 2008 study [22] evaluated the correlation between cable discharge events and a 490 ns TLP pulse on an Ethernet PHY transceiver. Correlation of failure to peak voltage between CDE and the long TLP pulse was achieved.

5.3.5 Charged Board Events (CBE)

Another source of confusion between device and higher-level assemblies relates to failures which occur at the circuit board level and may be caused by electrical overstress (EOS). Indeed the physical failure analysis often suggests this.

It has long been known that ICs and other ESD-sensitive components remain at risk when they are mounted onto printed-circuit boards and other assemblies. However, most ESD testing and characterization of these ICs has been done on stand-alone parts. Further, IC failure analysis data, which is based on knowledge of failure signatures seen in standard HBM and CDM tests, has caused many to conclude that ESD failures are relatively rare when compared to other electrical failures commonly classified as electrical overstress. Recent data and experience [23, 24] now suggest that many failures previously classified as EOS may instead be the result of ESD failures due to Charged Board Events. A charged board stores much more energy than a device (IC) because its capacitance is many times larger. In fact, the charge (energy) transferred in the event can be so large that it can cause EOS-like failures to the ICs on the board. While it is likely that many of these failures occur during handling in manufacturing, some do occur during installation, maintenance and repair. This can be confused with system failures since the failure only becomes obvious when the board is installed and the system is powered up.

5.4 Review of Other Published Case Studies and Investigations

A review of studies done through 2007 was given in White Paper 1. In this section we survey some of the work since then.

In one study [24] the researchers used a field-induced charged-board event stress method to get information on the IC on the board. The waveform had a ringing shape similar to the MM waveform. Stress levels of 500V to 3 kV were investigated. The study did not attempt to find a connection with the IEC stress. Such a comparison was made in [25]. The authors compared

stresses from HBM (JEDEC A114) IC level (from 1 to 8 kV) with IEC system level stresses (from 2 to 8 kV) and found no test result correlation between the models.

In [26], an IEC pulse generator and a TLP test system were both used to deliver a pulse thru a coaxial cable to the DUT, mounted on a test fixture board. The IEC generator used a 330 Ω series resistance and the TLP used both 50 Ω and 100 Ω series resistances. The TLP produced a more repeatable pulse shape than the gun. The waveform had the same general shape; that is, the gun produced a "camel hump" shape but the TLP had a flat plateau shape instead of a hump. The TLP method applied low voltages (up to 450V with I = 1.63 A for the measured pulse current) compared to the IEC Gun (1200V with I = 2.0 A for the measured pulse current). The TLP method showed increasing pulse current at stress levels close to failure. The IEC method did not detect these changes.

In [27], off-chip surface mount protection devices were stressed based on the IEC ESD gun (contact discharge) principle, but the Human Metal Model method, which uses the IEC waveform, was used to get the stress data. These SMDs are used to protect antenna switching pins, which are connected to the outside world. The three different type SMDs passed 8KV using the contact discharge mode.

In [28], the authors used TLP (with parameters assumed to be similar to IEC system level requirements) to stress the high voltage pins of Lateral DeMOS based protection devices. The pulsed voltage ranged up to 50-70 V, with corresponding pulsed current up to 12-15 amps. The authors were testing for transient latch-up and hot plug-in type failures. They reported on the mechanisms, but no comparisons were made to the actual IEC system level procedure.

Finally, in [29], the authors actually define a System to Component Correlation Factor and use thermal failure as the correlatable mechanism. They used the HBM and HMM methods, where the ratio of the two failure voltage levels ranged from 11% to 39% depending on the technology. They further identified the range of similar ratios for transient voltage overshoot as 11-14%, and the range for thermal failure as 29-39%. This study showed potential correlation between HMM and HBM but does not provide any evidence of correlation of either model with the IEC method.

5.5 Conclusion

ESD ratings obtained at the device level using the standard HBM and CDM tests have no useful relation to the impact the device may have in system level stress testing. The differences in the stress testing procedures and the electrical characteristics of the different pulse waveforms [30] make any correlation between the methods difficult and unlikely. Early correlation data confirms this hypothesis. More realistic models and test methods such as cable discharge events, charged board events and others have been or are being developed which are designed to simulate more realistic system level environmental stresses. These new methods should be regarded as complements to the IEC 61000-4-2 standard since the IEC method does not address many of the expected stresses.

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Chapter 6: Relationship between IC Protection Design and System Robustness

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6.0 Introduction

There is a perennial misconception that an IC's ESD protection is intrinsically and critically related to the system level ESD protection when the IC is placed in a PCB application. In Clause 8, this non-correlation of results between IC and system level stresses has been presented. However, when the issue is related to the **external pins**, an IC pin's ESD protection, designed for handling during production, assembly, and test, will influence the effectiveness of the system protection design as indicated in Figure 25. Here, an important distinction is necessary:. if the external pin protection involves an on-chip design strategy, then the design has to directly meet the IEC waveform stress standard. Moreover, designing for excessive HBM and CDM ESD levels does not guarantee system protection against an IEC stress. If on the other hand the external pin's protection is provided by an external clamp then a thorough understanding of the interaction between the IC ESD clamp operation and the external clamp efficiency is required. In this latter case it would be important to note again that the IC's protection is designed only to meet the ESD specifications in a safe, ESD controlled environment. However, to achieve system protection for the external pins to the outside world, rigorous analysis of the interaction between the IC pin's ESD and the external clamp design is necessary.

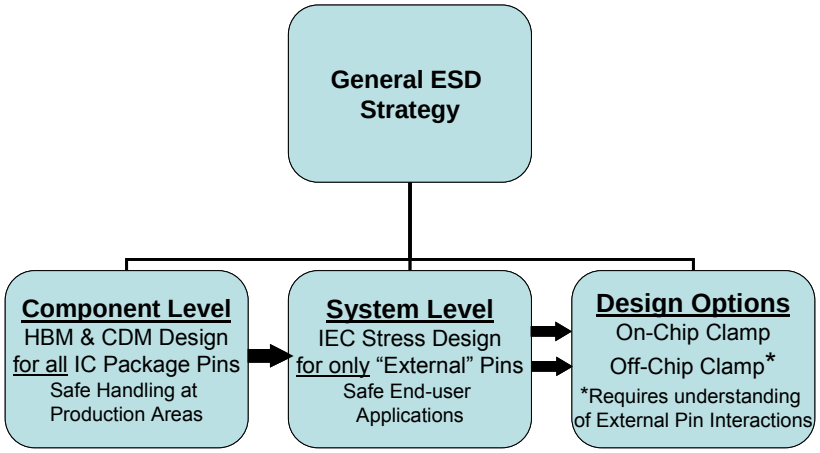

Figure 25: Component vs. System ESD

After a brief background of IC ESD protection methods, the main focus of this chapter will shift to the system protection design techniques from the IC's point of view. Important concepts will include:

1) The relevance of the IC application to the system ESD design

2) PCB protection methods

3) Interaction between the IC pin clamp and the on-board protection

4) Characterization of the IEC pulse

5) Various types of external pins and how the parasitic and components on a board affect design

6) Pros and cons of an on-chip IEC protection strategy

7) The effect of the parasitic components on the IEC pulse stress

Finally, an approach for integrated and compatible design will be offered based on all of these aspects. This will effectively involve a co-design effort between the IC ESD designer and the system board designer.

6.1 IC ESD and Latch-Up Protection Methodologies and Irrelevance for System Robustness

The ESD protection design for an IC package is known to be critical for safe production and handling. It is commonly understood and accepted that this protection design is expected to meet or exceed the required ESD specifications when these ICs are handled in an ESD-safe area also known as ESD Protected Area (EPA). The control method techniques for EPA have progressed sufficiently over the past 30 years such that ICs now require only the minimum specified protection levels [1]. Typical IC level ESD protection requirements, addressing both the HBM and CDM, commonly specify 2 kV and 500 V, respectively. To meet the HBM level of 2 kV the IC pin must survive an equivalent current transient pulse of 1.3 A in magnitude with a rise time between 2 ns to 10 ns, and a decay time of 150 ns. The energy under this pulse roughly corresponds to a 100 ns wide square wave pulse with a magnitude of 1 A. The CDM level in contrast refers to a current pulse with a rise time of ~200 ps and a pulse width of 1 ns, but the current magnitude can vary widely due to large variations in the IC package sizes [2].

ICs also require immunity to latch-up as tested by the JEDEC latch-up test standard JESD78B. While the device is placed in standby mode the IOs are pulsed with +/- current 100 mA injection with a compliance voltage of 1.5×VDD. The test is typically performed at both nominal and high temperature. The device is considered to have failed if the IDDQ current (after the stress is removed) exceeds 140% of its pre-stress value. Therefore the IC protection devices designed at the pins must pass both the ESD requirements and latch-up requirements. Latch-up can have significant impact on the system level ESD design, as will be described in the later sections.

6.1.1 Constraints From Silicon Advances

The IC ESD protection design technique involves protection clamp design to handle the corresponding range of current pulses for both HBM and CDM tests. These clamps essentially are triggered by either type of pulse discharging the current; while preventing any voltage buildup

that might cause damage to the input gate oxide or to the output buffer transistors. However, during the last few years, as silicon technologies have rapidly advanced, compatibility between the IO protection circuit and the increasing demands for IO speed have become an extremely challenging aspect. For data rates above 20 Gb/Sec, HBM and CDM levels cannot be met in a practical situation. The impact on CDM robustness is more serious for the following reason; IC package size has a direct correlation to the discharge current at a given CDM specification voltage. Many of the high speed serial link buffers (HSS) are now commonly designed in high pin count IC packages, producing relatively large peak discharge currents which make CDM protection design difficult. This effect, combined with rapidly shrinking silicon technologies that result in lower oxide breakdown voltages and sensitive transistor junctions, leads to a drastic reduction in the ESD Design Window. For example, large microprocessor chips (used for internet application) at the 45 nm node cannot tolerate CDM peak discharge current levels higher than 4-5 A. In these specific cases, achieving a 500 V CDM passing level becomes impossible to reach, and this situation obviously gets worse as the technologies are scaled further. Detailed and documented work done by the Industry Council on ESD Target Levels addressed these issues and concluded that due to improvements in manufacturing ESD controls and awareness, HBM levels can be dropped to 1 kV and CDM levels to 250 V while still keeping ICs safe during production and assembly [1,2]. The new levels are steadily receiving more support and OEMs are generally starting to accept the new IC ESD specifications.

Silicon technology scaling does not have such a directly negative impact on latch-up immunity. However, the trend towards bulk technologies with high resistance substrates, to achieve better RF performance and cost-effectiveness, can increase latch-up sensitivity. The design for latch-up loses some margin as the devices become more susceptible to accidental latch-up effects, especially when tested with system level IEC pulse tests.

6.1.2 HBM/CDM Events Compared to System Level IEC ESD Stress Pulses

Historically, there has been confusion about the difference between the HBM stress and the system level IEC ESD stress pulse. The models are different: HBM refers to a human discharging through the skin to a pin of the IC, whereas system level IEC ESD stress refers to a human discharging through a metallic tool to the system. As a result, the two models are represented very differently. For HBM, a 100 pF capacitor is charged to 1 kV and discharged through a 1500 Ω resistor. For system level IEC ESD stress, a 150 pF capacitor is charged to 8 kV and discharged through a 330 Ω resistor. When compared to the HBM event, the system level peak current is much higher – 0.7 A/kV vs. 3.75 A/kV, although both event time domains are approximately the same. With the system level requirement of 8 kV vs. 1 kV for HBM, the corresponding IEC peak current level translates to greater than 30 times larger in magnitude. The energy under the pulse for the system level IEC test requirement is thus more than one order of magnitude larger than the required HBM level for safe handling. With this difference in energy, any generated physical failures and their failure modes would be distinctly different. For the system level IEC stress it is not uncommon to see failures resembling an EOS failure mode. The event rise-times are also different: 2-10 ns for HBM compared to 0.6-1.0 ns for the system level IEC stress. But the similarity comes through for the CDM event where the rise time is typically in the 0.2-0.3 ns range. The actual system level IEC pulse has a shape with a CDM-like initial pulse (~30 A at 8 kV) followed by an HBM-like tail pulse (~15 A at 8 kV). Depending on the design, physical damage can be found which mimics EOS damage or HBM/CDM like failure modes. However, the physical damage in total only represents a minority of the relevant system failures due to

system level ESD stress. 'Soft' or resettable failures are more prevalent system level failures . Soft failures do not correlate to any failure mode known from IC-level ESD tests.

6.1.3 Marginal Impact of HBM/CDM Robustness on System Level IEC Stress Robustness

HBM stress testing is intended to gauge the ability of an IC pin to protect against handling in an ESD protected area. The most relevant pin combination is stressing to GND. However when the same IC is now placed on a system board, the internal pins do not directly encounter the HBM event. Even if some *residual noise voltage* appears, it has no relation to the HBM event and thus the reduction in IC ESD levels would play no role for these types of pins. Another distinct difference between HBM and the system level IEC stress testing is that HBM is an unpowered test, while the system level IEC test is usually performed with power applied to the system. As a result, the discharge paths are different. Therefore, predicting the survival of an internal pin during system level ESD events has no correlation to its measured IC HBM performance. Some comments on the CDM reduction are also in order. When an IC IO pin is designed for CDM performance, care is taken to suppress transient voltage overshoots from the very fast rise times. When internal pins are in the system, they do not see the same CDM discharges, and the transient voltage overshoot is not an issue. In summary, reducing both HBM and CDM IC levels while safely meeting all IC handling and manufacturing requirements would have no influence on system level protection for all pins that do not interface with the outside world. Even in the case of external pins, an efficient and systematic procedure can be followed using the transmission line pulse information on these pins without any particular regard to HBM and CDM IC levels. This is a more effective method for system design than relying on specified HBM and CDM IC levels. This method, known as "System-Efficient ESD Design" (SEED), is described in detail in Section 6.6. Demanding artificially high HBM and CDM IC levels for system protection of the external pins can potentially backfire as the internal ESD clamp can severely interfere with operation of the external clamp. An example of this is illustrated in Section 6.7.

6.1.4 Impact of Latch-Up Sensitivity on System Level IEC ESD Stress

As mentioned earlier, increased latch-up sensitivity can impact on the system robustness. This applies strongly to external pins but can also affect internal pins. If a soft failure from system ESD testing is seen on internal pins it could be related to EMI phenomenon and indicate a need for improved shielding of the IC on the board. But if a soft failure is seen at the external pin, the effect could be coming from the fast rise time of the initial spike of the system level IEC ESD waveform. The powered test often exposes this sensitivity. Close attention to the System-Efficient ESD Design is required in these cases.

On a final note, looking forward, system protection issues have to be addressed with the new realistic ESD levels kept in proper perspective. These are described in detail along with a co-design methodology for achieving effective integrated system protection design in the following sections.

6.2 Secondary Effects of System Level ESD Stress - Impact on Internal Pins during System Stress

While internal pins should not be directly affected by system level stress, they can still be stressed during a system level ESD event due to secondary effects such as electro-magnetic coupling from

directly stressed external pins and/or discharge from the case to the circuit board. These secondary risks are described and methods for reducing exposure to them are discussed in the following paragraphs.

A system level ESD pulse injected onto the external ports of a system can either capacitively or inductively couple to PCB traces neighboring the forced trace, inducing a voltage spike on the neighboring traces and any internal pins connected to these traces. The overvoltage spike can disturb the IC function in various ways:

1. It can induce a malfunction of the IC due to a misinterpreted signal.
2. It can cause surges on the supply traces leading to an upset of the IC.
3. It can cause latch-up of the circuit attached to the IC pin (e.g. the on-chip protection element).

All three effects correlate to the magnitude of the overvoltage spike appearing at the IC pin. Since the induced voltage spike is only caused by the sharply rising or falling part of the forced primary pulse, the energy that is electromagnetically coupled to any neighboring trace is typically too low to cause physical damage to internal pins connected to that trace. In extreme cases where no board level measures are taken, physical damage has been observed at higher levels of forced pulses. However, functional problems at lower stress levels are observed even when no physical damage has occurred yet. These functional problems at lower stress levels almost always precede physical damage when the stress level is increased step-by-step.

To control induced voltage spikes on internal pins, board designers must be aware of and work to mitigate electromagnetic coupling between external and internal traces during board design. For example, care must be taken to limit the maximum length the trace of an external pin runs unshielded parallel to the trace of an internal pin. Passive board elements may also be used to damp the voltage spike on both the forced trace and the coupled victim trace(s) next to it. Note that on-chip ESD protection optimized for HBM or CDM stress does not contribute to the reduction of these perturbation effects as they are designed for the protection of the unpowered device. To the contrary, a highly efficient on-chip ESD protection is usually more prone to latch-up which enhances the susceptibility to functional failures.

If there is a direct discharge inside the case to a PCB trace, e.g. arcing from metallic parts of the case, internal pins connected to that trace may be damaged. The mechanism is distinctly different from electromagnetic field coupling and can only be controlled by distance rules and selection of appropriate materials. The case design must provide low impedance from any point on the case to the point where it is connected to ground. If the impedance through the case is too high, arcing to the board at the board attach points or at locations where the case is physically very close to the board may occur. Should this happen, charge may be injected directly into a internal interconnect, leading to destruction of its circuits.

Whenever discharge inside the case cannot be completely eliminated, the pins connected to the endangered traces need to be considered as exposed or ‘external’ pins with appropriate system level ESD protection. The achieved HBM level of the IC has only marginal impact on the system robustness in these types of failures due to the very high energy of the system level ESD discharge pulse. Note that here the design effort for the system and board design will not be different between ICs qualified for 1 kV or 2 kV device level HBM.

6.3 Full IEC Protection On-chip Design Strategies

6.3.1 On-chip System Protection Design

Protecting an IC against system level pulses using only on-chip protection measures is a difficult task for a number of reasons:

- The shape of the incoming pulse is largely unknown as the board surroundings greatly influence the pulse.
- Due to radiation and coupling effects, it is difficult to establish exactly which pins will be stressed – multiple pins can be stressed simultaneously.
- During system level tests, the IC can be in a powered state, possibly leading to latch-up failures.
- Other ESD tests only take destructive failure into account, while for system ESD, system disruption needs also to be considered as failure mechanism, depending on the application requirements.
- At the time of IC manufacturing , the off-chip circuit is most often unknown.

These elements complicate the on-chip protection strategy. In general, the unknown pulse shape and the unknown amount of energy per pin make it impossible to guarantee a certain amount of system level robustness by design of on-chip measures. This design is often done without a worst case analysis and thus may lead to either an overdesigned or insufficient design. To design for an ideal 8 kV system level IEC ESD pulse applied to the IC directly is much more straight-forward from the perspective of the ESD design engineer, as the energy and pulse shape are better known. Unfortunately, this would be insufficient for the final system level test. The standardized IEC test is applied at the system level. Therefore, an IC design which did not consider the influence of the system environment would not lead to the intended system level ESD robustness.

Some ESD protection strategies focus closely on specific ESD stress waveforms like HBM. ICs with such a strategy can be inefficient for system level IEC stress due to the unknown pulse shape (even if scaled up to handle the energy). For instance, the pulse duration during system level ESD can be much longer than during regular HBM. It could be assumed that the pulse rise time should be equal or slower than the system level standard waveform, but this is not guaranteed. Due to switching (e.g. of a snapback clamp), a local parallel (parasitic) capacitance can discharge at rates higher than the system level standard, depending on the size of the capacitor, and the impedance seen during discharge.

In case of system level stress, typically the ground line/plate takes a lot of current. Since the supply voltage level of an IC is referenced outside the IC (e.g. in the battery), this current influences the supply voltage seen by the IC: it can become smaller for positive stress, but larger for negative stress. This means that it should be expected that the power clamp will more likely trigger during negative system level stress than positive stress. The power clamp must be able to survive this stress and recover fast enough from a latched state. In some cases where system upset is not allowed, this poses great difficulties in designing an efficient power clamp.

In Table 6, the merits and demerits of typical on-chip ESD protection approaches are compared in terms of trigger speed, latch-up and long duration pulses.

Table 6 – Comparison of typical on-chip protection concepts regarding IEC stress

	Zener	Snapback		bigFET
		SCR based	*ggNMOS/Bipolar based*	
Trigger	+ ok	+ Can be adjusted	+ Can be adjusted	- Depends on external capacitance
Clamping	+ No latch-up concerns - Too high resistive/huge area	- Latch-up must be avoided + small area possible	Medium area	+ less latch-up critical - Very large (especially if only needed for 1 pin)
Long stress pulse duration	+ ok	+ ok	+ok	- May switch off before stress is finished.

The protection device trigger scheme must be able to handle a broad spectrum of transient pulses, from very fast, to extremely slow. The supply lines are often stabilized with board-level capacitances such that the voltage rise time can be very slow, though the voltage can still rise above the critical level. For transient (rise time) triggered clamps, this can be a critical issue.

During clamping, latch-up must be avoided. Therefore, an approach with a holding voltage below Vdd poses a risk, since the power supply would then inject large currents into the system as the protection device would remain on. The duration of the event is also unknown. Techniques where the clamp's turn off is defined by an RC scheme after a fixed time can therefore be considered risky.

Zeners can shunt system level stresses well, but can consume significant silicon area. They remain fairly popular in some high voltage processes, but are hardly used in advanced CMOS anymore where minimal protection device area is needed.

SCRs are widely popular as ESD protection structures because of their high current capabilities per unit area, low capacitance, and effective clamping behavior (low holding voltage, low on-resistance). They can be used as local clamp and/or as power clamp. SCRs have a number of important advantages for use as system level protection devices. Due to their small area per failure current, it is relatively easy to scale up these devices to dissipate large energies. In many cases the stress needs to be dissipated to the lowest impedance pad, which in most cases is ground due to the many bond pads connected to Vss. Since the SCR can be placed locally, the current can be redirected to ground without passing the supply line. This is an important advantage to avoid system upset.

The drawback of SCRs is their low holding voltage. Thus careful engineering must be applied to avoid latch-up. This can be done either by increasing the holding voltage, or by increasing the trigger/holding current.

Bipolar/ggNMOS based circuits have good properties for dissipating system level stress as well. In general triggering, clamping and turn off behavior can be designed to cover a wide range of specifications. The optimization of these circuits and devices is not easy though, and is often very process dependent. Multi finger triggering issues can be dependent on the applied pulse; trigger voltage engineering is often necessary. For very large energies, the area consumption can be significant.

BigFET are the more risky approach. The trigger voltage is not guaranteed if the higher frequencies are filtered from the ESD pulse. This can result in damage even for a low level pulse. The capacitance seen by the IC is the most critical factor: for small capacitances, the ESD pulse reaching the IC has sufficiently high frequency components to trigger the bigFET clamp. For medium capacitances, the bigFET might not trigger. For large capacitances, the voltage rise will be too small to endanger the core. The risk for latch-up is minimal if guard banding is done correctly. It is however possible that the bigFET clamp will draw some additional leakage current for a small period of time, as the trigger circuit might weakly bias the bigFET gate.

If only one pin needs system level protection, increasing the bigFET for the full 8 kV IEC specification is a significant overdesign. Concerning turn off behavior: if the energy at low frequencies is too high, the clamp's behavior will have increased impedance (i.e. turned off) while significant energy remains in the pulse, again causing damage.

Special care should be taken with high voltage technologies, as the latch-up threat is even more prominent. For high voltage applications, the system level stress is a very hazardous test, since it is extremely difficult to shunt high current at a holding voltage level high enough to avoid any latch-up issue. This often results in very large area clamps. Also, more spacing is needed from the protection device to core circuitry for high voltage technologies, to protect against latch-up to nearby core circuitry. Specific bipolar circuits are commonly used, but they are often very process specific.

6.3.2 Interaction Between On-chip Protection and IEC Waveforms

This section lists various types of devices and their reaction to IEC pulses.

6.3.2.1 Devices that May Not Trigger Properly During 1st Pulse

If the response time of the PCB diode is too slow, or if there is no such protection at all, the on-chip ESD concept has to shunt an initial current peak and clamp the voltage seen by the sensitive nodes. The amplitude of this initial peak is strongly influenced by on-board passives. Usually only a minor part of this initial current spike will reach the IC. Nevertheless, on-chip protection design needs to take into account this part of the system level ESD stress which can be experienced by the external pins of the IC.

The initial rise time described in the IEC standard is fast (0.6 ns – 1.0 ns), but is still slower compared to the CDM specification (~100-200 ps). Taking into account however that the IEC peak current is a factor of three to five times higher compared to CDM specification of 500-1000 V (dependent on package size and characteristics), the dI/dts from both models can be very comparable. However, package and board parasitics, e.g. bond-wire inductance or inductive trace coupling, can slow down the pulse significantly. Therefore, the on-chip protection schemes must

be designed for the resulting wide range of dI/dt. The failure modes due to the non-triggering of the on-board diode during the first transient resemble CDM fails of IO circuitry. High levels of CDM protection at the external pins, able to handle 5-10 A of CDM current, will reduce the risk of this type of failure. However, this may not be practical; especially for large packaged IC devices with high speed serial link (HSS) IO designs [2].

It should also be noted, that only the CDM discharge path to the local ground or the local supply line is relevant for shunting the 1st transient of a system level ESD pulses. IC level CDM testing often addresses different failure mechanisms which are located inside the circuitry of the IC and as such are system level irrelevant.

6.3.2.2 Device Designs that Require Energy Absorption from the 2nd Pulse

If the quasi-static clamping behavior of the on-board diode is insufficient or there is no such protection at all, the on-chip ESD concept has to shunt a large current causing significant energy dissipation in the device. This is ~10 times the energy of the typical HBM protection levels. Accordingly, the area of the protection devices has to scale up by a factor of ~10, increasing the parasitic capacitance of the IO circuit in order to shunt the full system level pulse on chip. On-board protection elements are capable of shunting large stress currents at lower capacitive loads and are beneficial for the overall performance of the system. In an optimum concept, the on-board diode and the on-chip ESD protection respectively act like the primary and secondary stages of a typical input protection scheme, where the current carrying capabilities of both branches are balanced by the serial impedance. Figure 26 illustrates how the TVS is properly isolated by on-board impedance from the IC's ESD clamp.

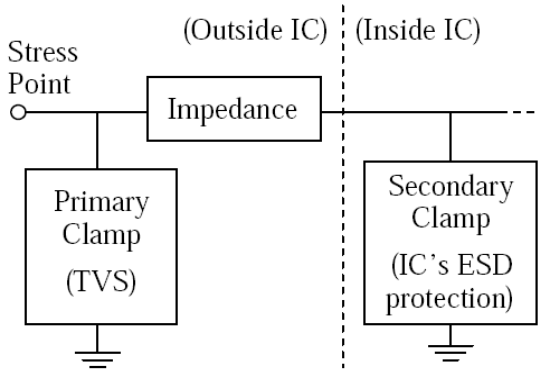

Figure 26: Two stage system level ESD protection by matched primary (on-board TVS) and secondary (IC ESD protection) clamps [3]

6.3.2.3 Devices that Require Latch-Up Immunity from the IEC Pulse

IC and system latch-up immunity depends on how well protection structures can filter different noise and stress pulses. ICs can see mainly two major kinds of high frequency disturbances in a system: direct conducted or radiated current pulses due to ESD and induced radiated noise which is emitted from internal RF lines. Conducted waveforms depend on the source circuit and pulse transmission line impedances and can have high current and voltage amplitudes in the sub GHz range. Radiated noise typically has main frequencies spread from MHz to several GHz range and

has relatively low current and voltage amplitudes compared to lines with direct pulse injection. An example of the noise levels are shown in Figure 27 and Table 7. Capacitively coupled noise has mainly high frequency components remaining as the capacitance acts like a high pass filter. On-board and on-chip protection structures have to be able to filter both these types of high amplitude stress pulses and withstand high frequency interferences without disturbing product operation.

Product ESD/EMC and latch-up immunity is typically validated according to the IEC 61000-4-2 standard by using both contact and air discharges. These stress pulses create both conducted and radiated disturbances in signal and power lines and may lead to damages, system latch-up or product operational failures. Operational failures, such as software resets, are the most common failure symptoms. The level of internal disturbances depends mainly on the system topology, including mechanical design and PCB layout. Latch-up or reset-sensitive components should be protected or located in a layout in such a way that maintains the immunity level. For example, disturbances can be measured with near-field probes if the target area is accessible during the stress. However, very often measurements are challenging to obtain without affecting system configuration and immunity problems are solved just by trying out different designs.

A more sophisticated way to solve immunity challenges is to use simulation. For example, 3D *Time Domain Transient* simulation can be used to calculate induced peak voltages, currents and waveform frequencies with selected stress waveforms [4]. Simulations are accurate if the product physical design, connections and materials are known in detail. Two example cases are shown in Figure 27 and Table 7 where the internal interference frequencies and peak voltages are simulated when a product metal cover is stressed with 1 kV and 8 kV IEC contact pulses. This information can be used to optimize system design either by preventing the interference with mechanical changes (better shield design or grounding), by adding filter components in the PCB layout, or by specifying an appropriate on-chip protection. The pulse resonance frequency is design-specific and the residual voltage depends on the impedance and location of the signal line.

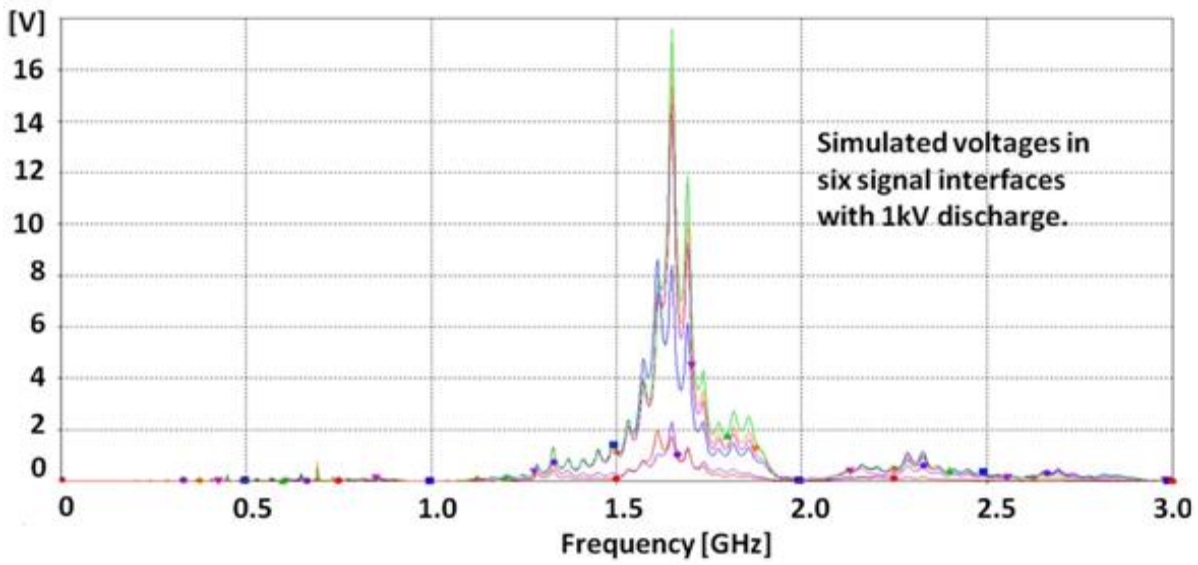

Figure 27: Time domain transient simulation of internal disturbances with 1 kV IEC pulse.
Depending on the components used and the operation voltage for example 10 V maximum induced noise level can be set as a target. More care in ESD/EMC design is needed if a signal line has higher varying voltages and the noise frequency is close to system clock.

Table 7. An example of simulated peak voltages and frequencies with different mechanical designs.

Peak voltages scaled to 8kV discharge and the related ringing frequency				
Cases	GND (0.1Ω)	Conn (10Ω)	CLK (10kΩ)	DATA (10kΩ)
CASE1	0.012V @ 2.2GHz	5.4V @ 1.8GHz	41V @ 1.9GHz	22V @ 1.8GHz
CASE2	0.005V @ 3.2GHz	0.84V @ 1.9GHz	15V @ 2.08GHz	6.3V @ 2.0GHz
CASE3	0.003V @ 2.1GHz	1.5V @ 2.0GHz	15V @ 2.1GHz	11V @ 2.3GHz

6.3.3 Discussion of Pro & Cons of Full On-chip IEC Protection

Based on the preceding information, it is possible to design an IC itself to be robust against an IEC ESD event; however, in the context of robust system level design, the practicality and effectiveness of such an approach must be considered. The typical motivation of equipment manufacturers for pushing IEC protection requirements onto ICs is the reduction of system level costs and area. Consequently, the practicality and effectiveness of IC-level IEC protection should be gauged in terms of its ability to reduce the overall system level protection measures and costs.

- The primary benefit of designing external pins of an IC to be IEC-robust is the IC itself will be more impervious to IEC-induced physical damage and operational upset, i.e. soft failures.
- The primary problems with designing external pins of an IC to be IEC-robust are:
    1) The added IC-level costs

2) The misconception that a single IC can guarantee IEC robustness of the overall system

An IEC-robust IC can eliminate the need for on-board ESD protection devices directly at an interface; however, the costs associated with IC-level IEC robustness – even for only a small set of external pins (typically two to six pins) – should be calculated to determine if overall system cost and performance are optimized. As mentioned previously, without information regarding the overall system design (e.g. what other components will be placed along with the IC) and how the system will be IEC tested, an IC would need to be designed to handle the worst-case IEC stress. Under such an assumption, IC-levels costs are impacted by two main factors.

1) Increased IC area: having to conduct the tens of amperes from an IEC discharge can increase IC area by as much as 30% due to the following determinants (in turn the increased silicon area can then drive the need for a larger package).

    a. For IEC-rated pins, ESD protection area will increase to withstand the higher peak currents of the IEC ESD event compared to HBM and CDM events; in general, an order of magnitude area increase can be expected for 8 kV contact protection compared to 2 kV HBM protection (Figures 28 and 29).

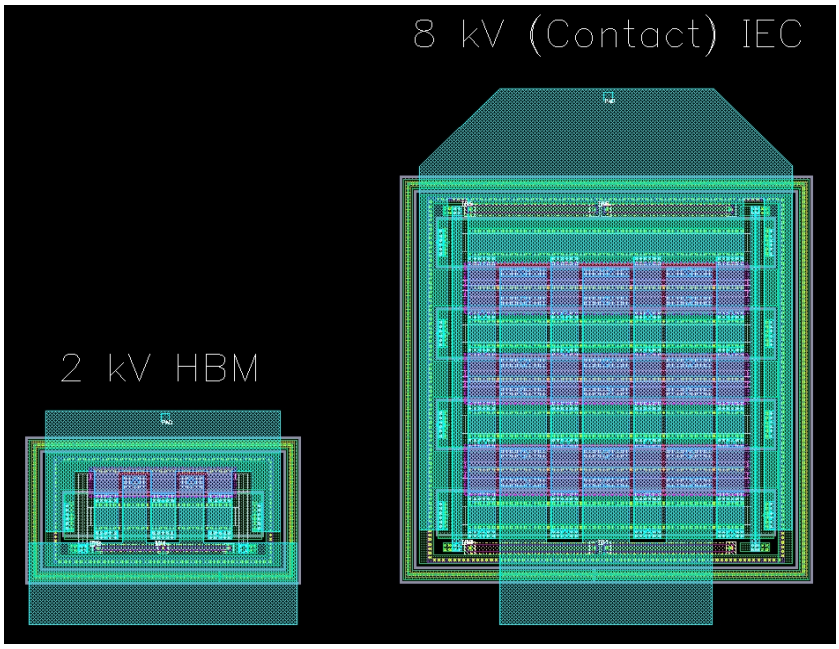

Figure 28: Comparison of 10 V ESD cell size in 1.0 um BiCMOS technology: 2.0 kV HBM version versus 8.0 kV (contact) IEC version.

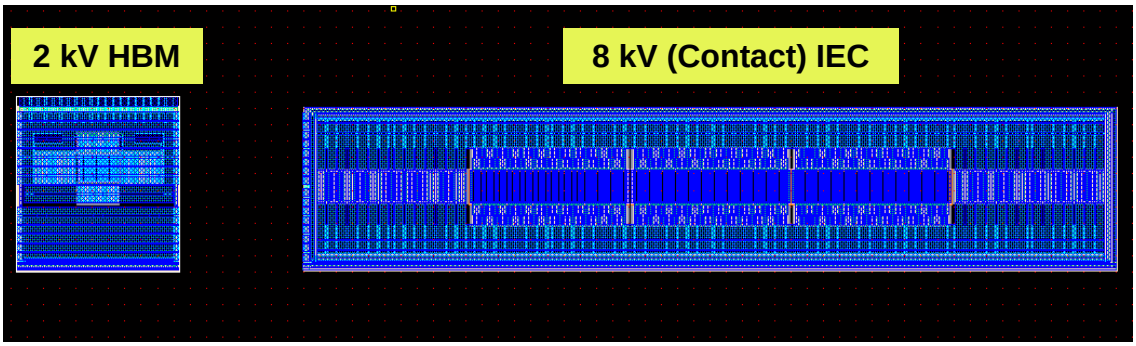

Figure 29: Comparison of ESD cell size in 65 nm CMOS technology: 2.0 kV HBM version versus 8.0 kV (contact) IEC version.

IC silicon technologies are typically optimized for lateral transistor performance; discrete (on-board) IEC protection technologies are specially optimized for vertical current flow. The resulting improvements in active conduction area and thermal impedance mean that discrete IEC protection devices can typically provide greater IEC performance with smaller active area and, consequently, with less degradation of system operation.

b. IC-level metals required to carry the current from IEC discharges will need to be widened by roughly an order of magnitude (comparing 8 kV contact protection to 2 kV HBM protection) to lower resistance and maintain reliable current densities.

c. The higher level of substrate injection that will occur during an IEC discharge drives more stringent guard-ring and inter-device spacing rules to avoid IEC-induced latch-up [5]. Unlike the area impact of ESD protection and its associated metal routing, which is localized to the IEC-rated pins (typically two to six pins), the area impact of IEC LU protection affects the entire IC, making it the most significant source of the area increase.

2) Increase in design time: having to contend with conducted and radiated energies from an IEC discharge increases design complexity. This added design complexity can directly translate to a 2x – 3x increase in the overall design time required to produce a working IC that passes the IEC requirement.

a. Due to IEC testing involving powered-up operation, an IC's functional and reset circuitry must be designed to account for the stress effects. Due to possible coupling effects, the possible impact to circuit design must be considered for all IC pins. As an example, an audio amplifier product in a 1.0 um BiCMOS technology required two additional metal-level design revisions to eliminate LU and functional issues which occurred during IEC testing.

b. As mentioned previously in this section, the possible variations in the stress waveform reaching the IC and the nature of powered-up stress testing restrict the choices for ESD protection on both the external and internal pins. ESD protection that would be optimum for HBM/CDM protection may not be usable due to system level ESD protection requirements; the resulting protection choice can then lead to more stringent protection implementation rules. As an example, an industrial transceiver product in a 0.25 um BiCMOS technology required three all-

level design passes to successfully implement protection compatible with functionality requirements, HBM/CDM protection requirements and IEC protection requirements.

As with a single on-board ESD protection device, a single IC – independent of its IEC robustness – will have little effect on the propagation of the radiated and conducted energies throughout a system if some level of effort and cost is not budgeted for proper system design**.** While an IEC-robust IC can eliminate the need for on-board ESD protection devices directly at an interface, proper enclosure design, proper system functional design, proper overall system protection design and proper circuit-board layout, are all still required to eliminate the occurrences of both system level soft failures and physical damage.

While IEC-robust ICs are relatively new, IEC-robust systems are not. It is known that IEC-robust systems can be built successfully using ICs with typical HBM robustness ratings from 500 V to several kV. It is also apparent that a system can fail IEC testing if an IEC-robust IC is improperly relied upon for protection within a system. A resulting conclusion is that proper system level protection measures are still required along with IEC-robust ICs to ensure overall system level IEC robustness. IC-level IEC protection can be a part of robust system design; however, for IC-level IEC protection to be optimally practical and effective, equipment manufacturers will need to work with their suppliers regarding aspects of their system design and IEC test methodologies.

6.4 Common On-board System level ESD Protection Approaches

6.4.1 General Aspects of System Level Protection

PCB protection strategies depend largely on product physical design and operational requirements. The primary system level ESD protection relies heavily on EMC design of both the system and the PCB that keep most of the ESD/EMC energy outside of the system. With a good cover design, the on-board protection can focus on external connections as well as on the cover hole and seam areas which may leak ESD energy inside. Non-grounded and badly grounded metal structures with high impedance to ground should also be avoided between the covers and electronics as those can leak secondary sparks and high frequency EM noise inside. The PCB ground has to be the first on-board structure to which the residual pulse is directed as the ground spreads and attenuates pulse energies to a safe level. Air gaps between the electronics and covers can also prevent ESD or limit discharge energies, as shown in Figure 30.

External connectors and antennas are typically the most challenging parts from ESD protection point of view. Connectors have signal lines open to unknown stress pulses, and on-board protection methods have to be set to attenuate and guide stress pulses to the electrical ground of the product. At the same time the design must limit electromagnetic disturbances to a level the product can withstand without major faults in operation. Protection must also limit the residual voltage and current to a level which can be handled by the IC's internal ESD protection structures (marked with red dots in Figure 30).

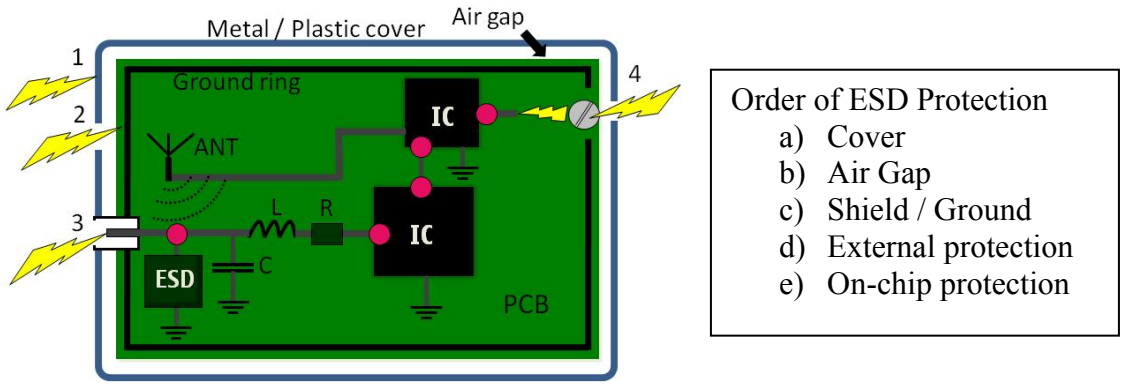

Figure 30: System ESD protection depends on product physical protection (covers), shields and groundings, on-chip and external signal protection and signal integrity targets.

6.4.2 On-board ESD Protection Designs

There are several different methods available to build up an on-board ESD/EMC protection system. The protection can be built with basic passive components or with specified ESD/EMC filters. On-board ESD protection has typically the next common design targets:

- Low capacitive load (especially when used with >100 MHz signal lines)
- Low dynamic resistance after turn on, to drain the ESD current and to keep the residual potential low
- Application specific trigger voltage (e.g. at 1 mA level) and low clamping voltage at relevant current levels of 15 - 30 A (e.g. after 30 ns)
- Low leakage current (especially with portable devices, demand is often <10 nA)
- Sufficient turn on speed to protect against IEC 61000-4-2 pulses
- Capability to withstand multiple ESD pulses with low impedance and return to a normal high impedance state immediately after stress
- Ability to provide both ESD and also EMI protection (depending on the need)
- Ability to withstand IEC 61000-4-2 pulses up to 8 kV contact and 15 kV air
- Ablity to withstand many IEC 61000-4-2 pulses without degradation
- Capability to protect against positive and negative pulses
- Frequency response of the tested circuitry without signal integrity problems while protection component works together with the on-chip protection design
- Easy protection to implement from PCB design point of view
- Small in physical size and low cost

Many of these requirements are mutually exclusive and the protection design must be selected based on PCB level design targets. For example, smaller dynamic resistance may increase protection component capacitance and limit component usage with high speed RF signal lines. The use of ESD protection often requires extra compensation as the impedance match and signal integrity have to be kept along the signal transmission line. This increases component count, requires more space on the PCB and increases product cost.

System designers make the ESD protection component selection based on the parameters described above. However, certain electrical parameters have a major effect on the selection.

- The capacitance of the component can be a major limiting parameter with high speed signal lines. Capacitance should be below 1 pF when frequency exceeds 500 MHz.
- The dynamic resistance strongly affects the residual voltage and current ($V_{clamping} = V_{trigger} + R_{dynamic}$ x current). For example a diode with low R_{dyn}=3 Ω and V_{trig}=7 V can create about 100 V residual peak potential with a 30 A (equivalent to 8 kV contact level) IEC 61000-4-2 peak current pulse. With higher dynamic resistance the residual voltage can be easily hundreds of volts.
- The trigger voltage depends not only on the system operation voltage but also on the inter modulation distortion and harmonics. For example, the coupled voltage amplitude in a 200 Ω trace can be over 15 V when the product has a transmitting antenna close to the PCB.
- The leakage current can be the main limitation, especially with battery operated products where it is often limited e.g. below 10 nA.

The residual potential is typically reported as a voltage left over on a test board when the protection device is used to filter the IEC 61000-4-2 pulse. This voltage waveform is not the same as the one used for IC HBM and CDM validation, and direct comparison between those ESD model current levels and potentials should not be made. Unfortunately, there is no information commonly available about on-chip protection triggering levels which could be used to choose external protection components. The residual potential may also be tested on a board with different impedance than the PCB where the protection component is going to be used. In addition, the protected IC can also be a factor on the residual pulse shape. Some examples of residual pulses are shown in Figure 31 and in Section 6.5.2.

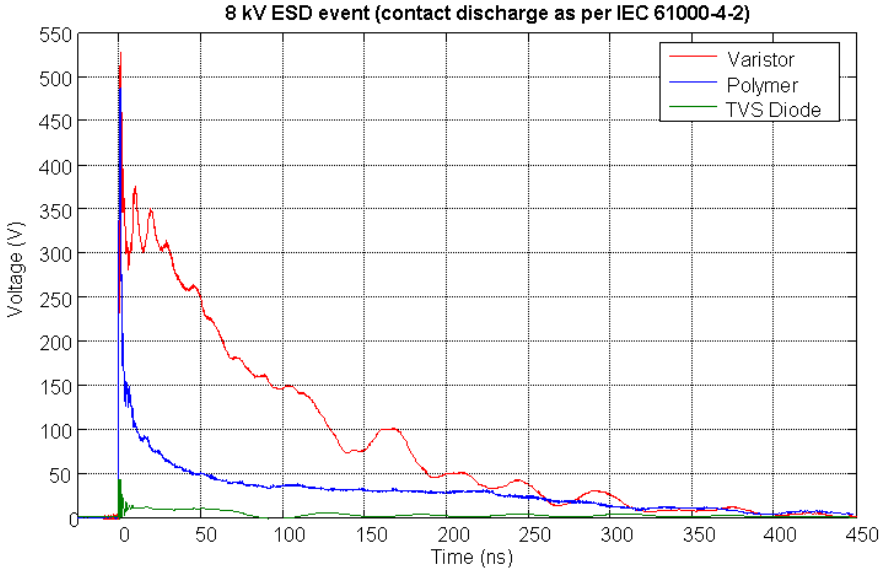

Figure 31: Typical residual potentials for various on-board protection components.

Protection components are also evolving and there are already devices available specifying advanced capacitance, dynamic resistance and leakage current parameters. Impedance matched protection components are also available and can be chosen depending on the case-specific

targets. Some typical electrical parameters for diode, varistor / suppressor, polymer and spark gap protection components are presented in Table 8. Some example protection designs are shown in Figures 32 and 33.

Table 8. Typical parameters for SMD ESD protection components which are used to protect low voltage medium & high speed data lines.

	R_{dyn}	VBR @1mA	Clamping	Capacitance (@1MHz)	Ileak	Turn-on	ESD withstand	Linearity
TVS Diode (C > 2 pF)	typ. 0.3..1 Ω	6…20 V	10…30 V(1)	complete range	1 nA	<1 ns	excellent (2)	depends on application
TVS Diode (C < 2 pF)	typ. 1..1.5 Ω	6…20 V	20…40 V	<< 0.5 pF	1 nA	<1 ns	excellent (2)	depends on application
Varistors (C > 2 pF)	> 20 Ω	30 ...300 V	> 100 V	complete range	< 10 nA	< 40 ns	Ok (3)	Ok
Varistors (C < 2 pF)	> 20 Ω	50 … 300 V	> 200 V	< 2 pF	< 10 nA		limited (3)	Ok
Polymers	< 1 Ω	100 .. 600 V	20 … 100 V	< 0.5 pF	100 nA	< 10 ns	Ok (3)	Ok
Spark gaps	> 30 Ω	> 250 V	> 200 V	< 0.1 pF	< 1 nA	> 5 ns	Ok	Ok

(1) at 30 ns according to IEC 61000-4-2.
(2) multistrike capability beyond IEC 61000-4-2 without degradation effects.
(3) leakage current may stay high after a single pulse. Some components have a good recovery, but not all.

- TVS Diodes typically have lower capacitance and higher ESD multistrike absorption capability than multilayer varistors. Once the ESD strike is absorbed by the TVS diode, the protection device returns to its high-impedance state very quickly.
- Varistors typically have a trigger voltage over 50 V, clamping voltages over 100 V and a dynamic resistance over 20 Ω after turn on. The capacitance of a varistor can be below 1 pF. Some varistors have significant leakage currents after ESD stress.

- Polymer devices typically have lower capacitances (<0.5 pF). The triggering voltage can be considerably higher than the clamping voltage and polymer components may also have a delay before they return to their high impedance condition after stress. Polymer devices also have lower endurance to ESD strikes.

- Spark gaps have a very low leakage current and very low capacitance, but the triggering voltage is typically more than 250 V. The residual voltage and current will stay high due to the high dynamic spark resistance.

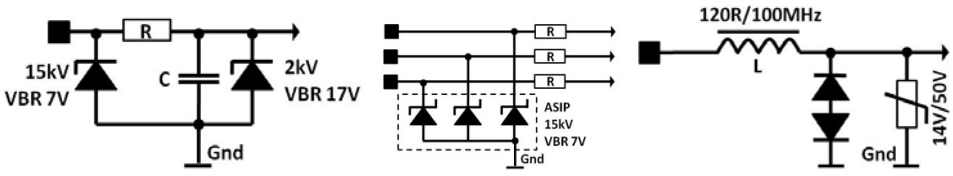

Figure 32: Two level diode, ASIP™ and a choke-varistor-diode designs for IEC 61000-4-2 15 kV air discharge protection.

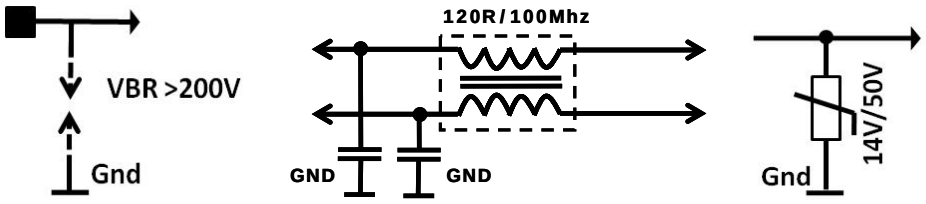

Figure 33: Spark gap, common mode filter and varistor protection.

Passive components can also provide protection against ESD. A series resistor, capacitor to GND or a common mode filter in a discharge path improves system ESD/EMI withstand but may limit signal quality, increase component count and may increase power consumption. Most signal lines have only limited frequency range where the data is transferred and passive components can be used for example to build up a specific LC filter with a low attenuation in the signal frequency. However, there can be space and cost limitations when multiple discrete components are needed for several signal lines. Small SMD passive components do not provide good protection against direct 8 kV IEC pulses but they can be used to protect against secondary pulses.

6.4.3 PCB Parasitic Components

The main purpose of discrete parasitic components, such as common mode filters, capacitors and ferrite beads, is to attenuate noise currents during ESD events. These components are typically not used as primary ESD protection components in a system design, but are located close to a possible ESD stress point in a layout. For example a resistor-capacitor pair or a diode with a known parasitic capacitance and a resistor is used to filter selected noise frequencies.

Parasitic components together with good mechanical protection can be the easiest and lowest cost ESD protection design. Product mechanics can block the major portion of ESD pulses and parasitic components will provide all required protection against residual waveforms and EMC noise. For example a memory card socket is typically accessible in a system and has to withstand contact and air discharge IEC 61000-4-2 pulses. When the socket is made of metal and is grounded to a PCB ground, the spark energy will not flow deep into the card contact pins. However, there will be some induced noise on pins and traces, therefore filter components are needed to prevent EMC disturbances.

6.4.4 'Realistic' Situations in the System

Product shape, the product's position on the test bench and transmission lines can all have an effect on the ESD pulse waveform when it moves through the stressed product. An IEC waveform has a pulse rise time specified from 0.6 to 1 ns when it is measured with a current-sensing transducer [6]. However, extra inductance and impedance mismatch in the discharge path will slow down, reflect and attenuate the current pulse when a real product is stressed with contact discharge. A rise time faster than 1ns with the main frequency of the ESD pulse is rare at the IC pin. Typically main pulse frequencies are below 500 MHz.

The second and third common discharge types are CDE or CBE. One example of fast cable and/or board discharge is shown in Figure 34. If the discharge moves through balanced impedances the waveform can keep its original shape and the component can see the stress

according to the original pulse. This is more or less a special case and can exist only when an impedance matched cable or part such as an antenna is connected to a product.

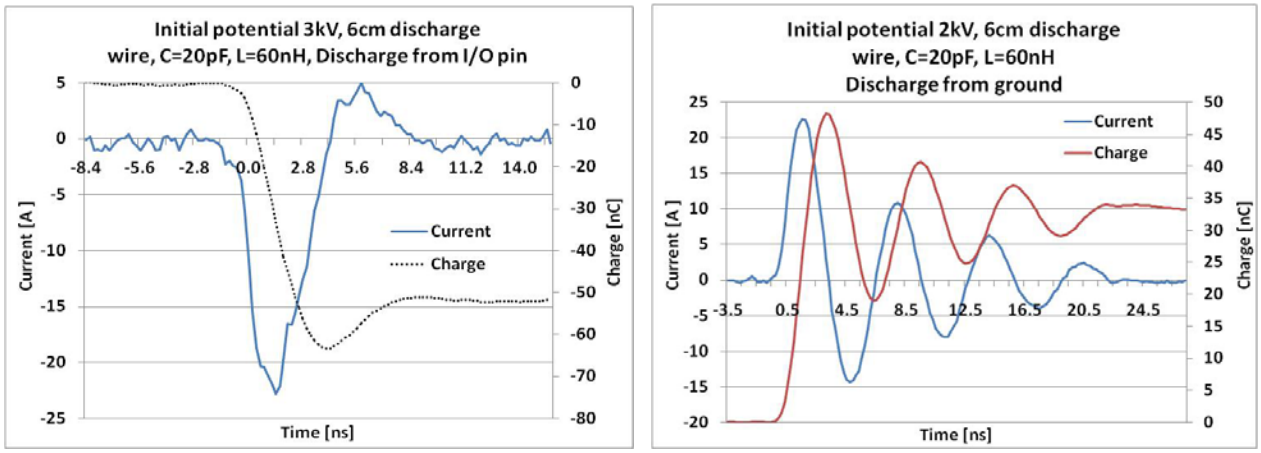

Figure 34: CCE/CBE discharge waveforms from an IO pin and a ground plane.

On-board protection components must trigger before on-chip protection, leaving only the residual current pulse to be handled by the on-chip protection. The residual stress waveform that components would see during IEC system level testing or during a CBE/CDE discharge is very different if compared to an IC HBM and CDM event at the pin. HBM has a time domain in the same range, but the discharge energy is not distributed in a similar way as occurs when the component is part of a system. In a system all IC IOs are terminated to ground, while supply voltages, signal lines and parasitic components vary depending on the PCB design.

A CDM pulse, in comparison, has an extremely fast rise time which typically does not occur when the IC is part of the system. CDM ESD levels are also reported as a voltage withstand levels only. Since package capacitance and effective peak current are not communicated; it is difficult to draw a conclusion on the robustness in terms of ESD current. Also, ICs must withstand high frequency EMC noise in a system, sometimes a fast CDM optimized IO protection may help to handle high frequency EMC noise in a system. However, as these high frequency signals have typically low current and voltage amplitudes (see Section 6.3.2.3), a high current withstand level, which is expected in the CDM validation of a large package device, is in most cases irrelevant.

In summary, both HBM and CDM qualification passing levels of ICs are not very relevant parameters from a system designer point of view and do not provide relevant information for system level ESD/EMC design. Also, on-board protection elements must have the specifications of residual voltage waveforms, dynamic resistance and other important parameters. However, this information varies from supplier to supplier. A System-Efficient ESD Design can only be performed if on-chip and on-board protection component characterization are linked to each other, for example, by using appropriate high current IV data valid for a few nanoseconds to 100 ns pulse duration.

6.4.5 Potential Competition Between on-chip HBM and On-Board System Level Protection

The on-board protection design should take into account the on-chip ESD design window. In other words, the maximum residual voltage over the on-board protection voltage clamping level must be smaller than the ESD failure voltage of the IC pin being protected. Additional margin can be created by the on-chip protection. As the on-chip protection draws current during the ESD event, an additional voltage drop is created over the board parasitics and package bond wires. This voltage drop is distributed over the on-board protection but not over the IC. Although there is no perfect correlation due to the numerous reasons already described, the HBM protection qualities give a reasonable estimate of the on-chip protection capabilities to handle this residual part of the ESD stress.

The time response of the on-board protection can be too slow for the fast rising edge of the system level pulse, depending on the strength of the damping effect of the board parasitics on the system level pulse. The on-chip protection then acts as a first protection.

These calculations are hard to make in the IC design phase, as most of these system related parameters are unknown. Different on-board protection elements can be tested on the final board in a trial and error approach and the best version can be selected. Good on-chip ESD protection can help to increase the number of usable on-board protection devices. Inappropriate on-chip ESD protection might make it impossible to find such a solution. The quality of the on-chip ESD protection is determined by the maximum voltage and current which the discharge path involving the IC pins can withstand. This can be extracted by electrical analysis methods as described in the following section (6.5) and is NOT the HBM withstand voltage!

6.5 Advanced Characterization of ICs for Achieving System Level ESD

6.5.1 IO Characterization of IC

For an effective integrated system protection design, the transient behavior of the ESD clamp at the IO pin must be first understood. TLP is commonly applied for extracting the IV characteristics at high current densities, as any forced DC current at those currents would immediately destroy the device under test. A TLP is a square current pulse generated by discharging a transmission line as shown in Figure 35. Transmission line pulses of 100 ns duration can be related to the energy of an IC level HBM stress pulse, which gives a certain preference to this waveform.

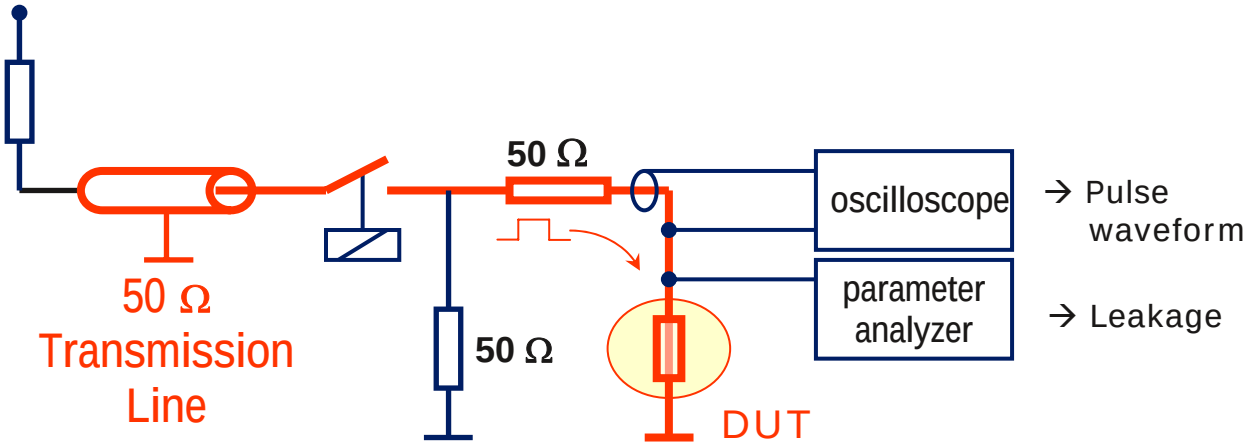

Figure 35: Typical set-up of a Transmission Line Pulse

The current and voltage values are extracted as mean values in the late phase of the pulse, where usually a plateau appears in the waveform (Figure 36).

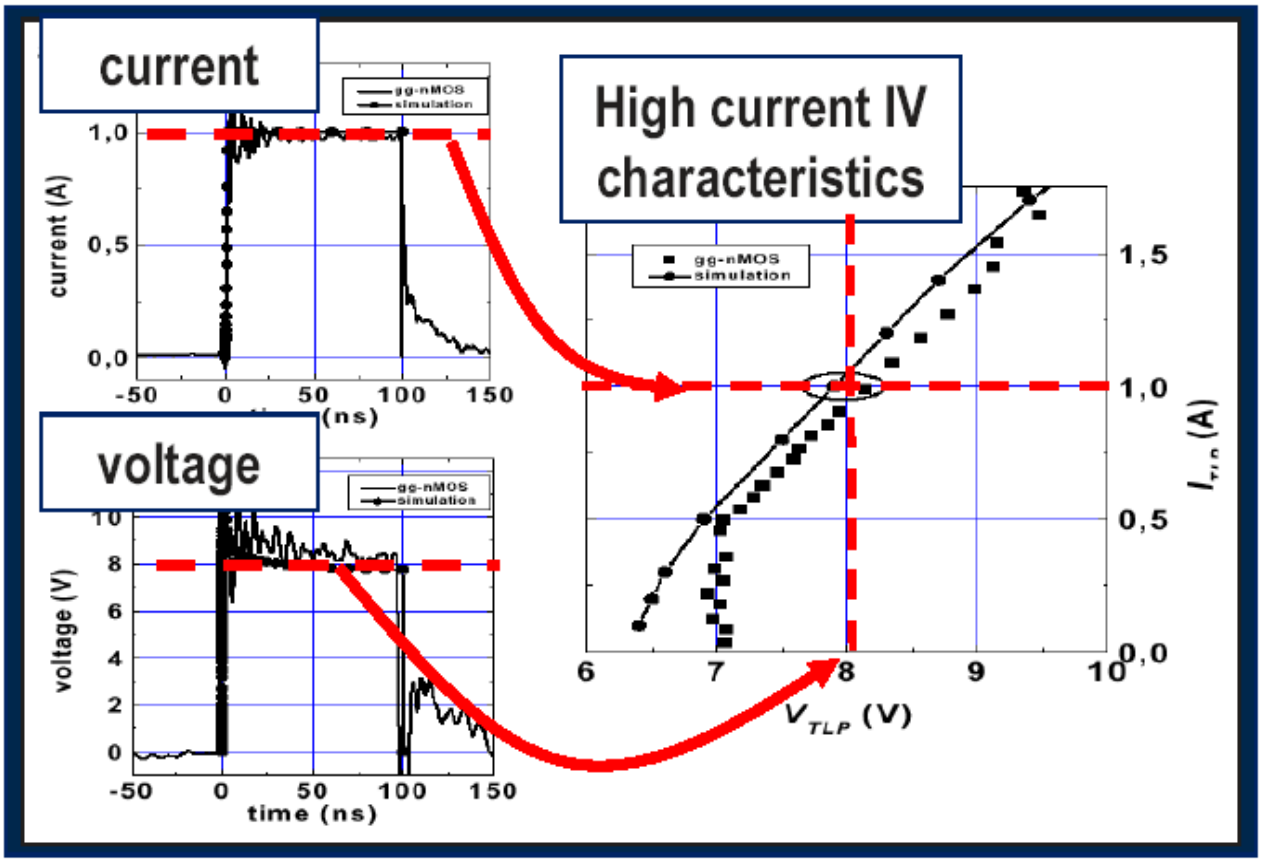

Figure 36: Typical 100 ns TLP I-V characterization for an IC pin.

To assess the possible impact of the initial high frequency (fast slope) contributions of the IEC pulse, very fast (VF) TLP with ns-wide square pulses can be used to sense the transient behaviour of the stressed IO circuit or protection diode. This is especially relevant as fast CDM-like pulses

usually trigger different mechanisms, which occur at different levels compared to HBM or 100 ns TLP.

6.5.2 Characterization for PCB Clamps

The Residual Pulse (RP) results from the limited clamping behavior of the (purple) on-board protection diode (Figure 37). The applied pulse is shunted to the respective rail (typically ground) via an on-board shunt device. A voltage drop appears across the shunt device (e.g. on-board protection diode), which leads to a 'residual' voltage pulse sensed by the protected circuit, e.g. the IO circuit of the IC (green).

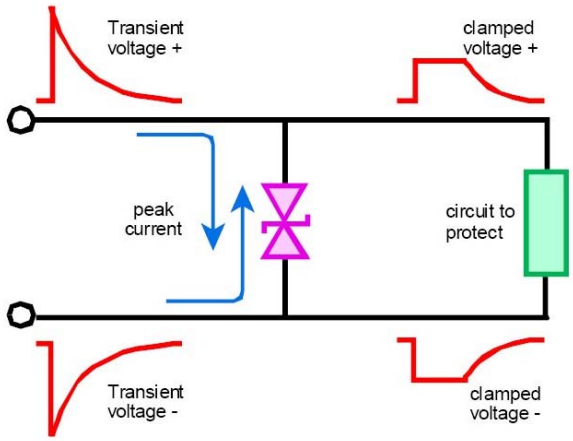

Figure 37: Residual pulse (waveform on the righ hand side) resulting from the finite clamping voltage of PCB diode (purple). Ideal turn-on behavior is assumed.

Typical clamping behavior of various on-board protection diodes is shown in Figure 38. TVS diodes are usually superior in their clamping behavior when compared to varistors for the same application. Figure 38 a) shows the capability to clamp long pulses. However, the transient behavior at turn-on in the first few ns can be even more critical. High voltage overshoots are detected for varistors exceeding the plateau value by more than 100 V as shown in Figure 38 b).

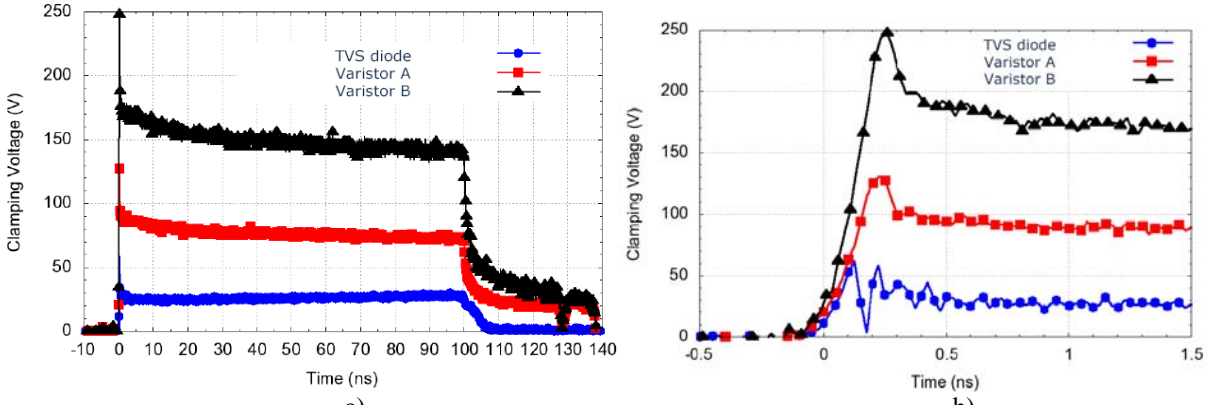

Figure 38: Waveform of various PCB diodes using a)100 ns TLP and b) very fast TLP

A worst case residual pulse can be extracted from the waveforms found in Figure 38 by taking into account the resistance of the PCB trace connected to the IC pin and the voltage drop across the IO circuit.

6.5.3 Characterization of PCB

The purpose of characterizing a PCB regarding system level ESD is to extract a sufficiently detailed RLC network, which allows a simulation of the board that includes the passive components and the ESD voltage clamping elements under system level ESD stress. Commonly an IEC 61000-4-2 pulse waveform is considered. While the initial fast spike might require including even very low parasitic contributions of inductance and resistance to correctly simulate gigahertz transmission, in many practical cases (e.g. automotive engine control unit boards) this initial spike can be neglected due to the large capacitance available on board or in the IC package which damps fast components. 3D field simulators enable the extraction of capacitance and inductance for a given board layout. Cross coupling phenomena caused by mutual inductance and capacitance can be extracted as well. For the sake of simplicity and reduction of the simulation nodes, only the self-inductance and the capacitance to ground will typically be used in a first overall optimization step.
Alternatively, analytical models can be applied to model the various parts of the wiring of the PCB [7, 8].

6.6 System-Efficient ESD Design (SEED) – An Optimized IEC Protection Co-Design for External Pins

6.6.1 Benefits for PCB and IC Designer

When an IEC 61000-4-2 discharge is applied to an external pin on the system board, the main ESD current Ip flows directly to ground through the on-board TVS, but some current Ic will enter a connected IC and flow via its internal protection to ground (see Figure 39).

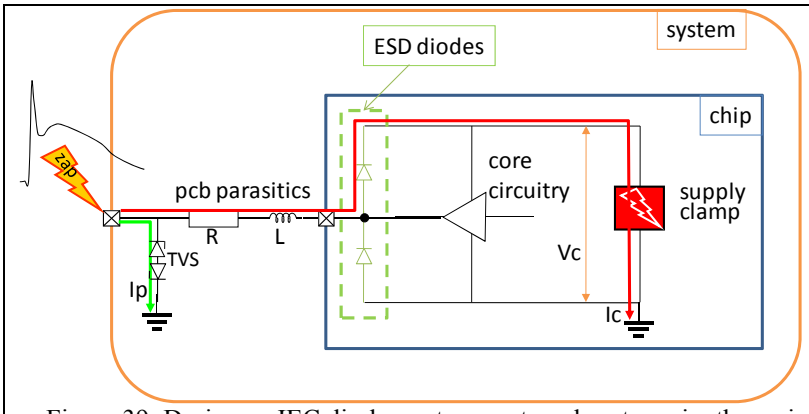

Figure 39: During an IEC discharge to an external system pin, the main current (Iz) flows via the on-board TVS protection to ground, but some current (Ic) will enter the IC and flow via its supply clamp to ground.

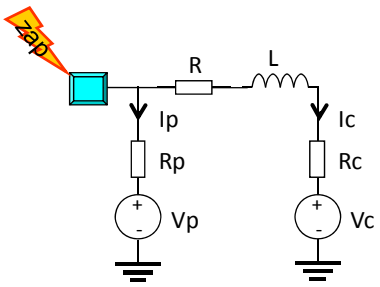

Figure 40: Simplified replacement diagram.

In order to prevent damage to the IC, it is important to assess the amount of current Ic which may enter the IC and the associated (over-)voltage Vc across the connected IC circuitry. The

calculation may be simplified by approximating the TVS and the on-chip protection by diode-like devices, characterized by their on-voltage Von and on-resistance Ron. A simplified replacement diagram is shown in Figure 40. If all parameters of the devices in Figure 40 are known, straightforward application of Kirchhoff's Current Law will yield the current distribution (Ip, Ic). The resistance R and inductance L of the wiring, both on-board and on-chip, play important roles. Particularly for wire-bonded chips, L may be significant, and the additional impedance may reduce the current from the first peak entering the chip to a negligible value. In that case, the IEC robustness may be estimated by considering the current distribution in the second peak only. Since the timescale of the second peak is very close to the HBM timescale (around 100 ns), the relevant I-V characteristics of all ICs may be estimated using a 100 ns TLP test.

6.6.2 Example of SEED Design Using 100 ns TLP Data

As an example, a 5 V audio output designed in 65 nm CMOS and placed on a board is planned to be protected by an on-board 6 V TVS diode. Figure 41 shows the I-V characteristic of the audio output to VDD (forward biased ESD up-diode). Figure 42 depicts an I-V characteristic of the TVS diode. Both characteristics have been measured separately by means of 100 ns TLP.

The 65 nm chip is wire-bonded inside its package. For an estimated wire inductance of about 1 nH, the additional impedance $Z = \omega L$ equals about 12 Ω for 0.5 ns (first peak) and about 0.2 Ω for 30 ns (second peak), which justifies neglecting the first peak.

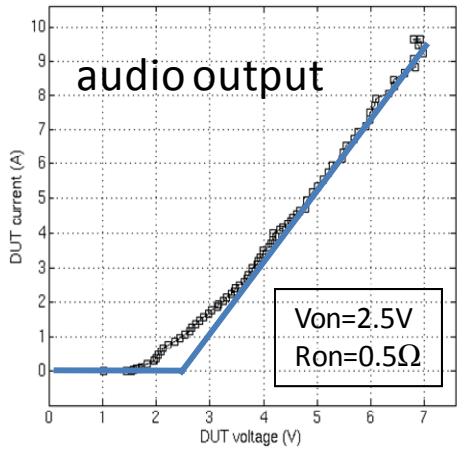

Figure 41: Audio output (+ESD up-diode) I-V curve measured by 100 ns TLP.

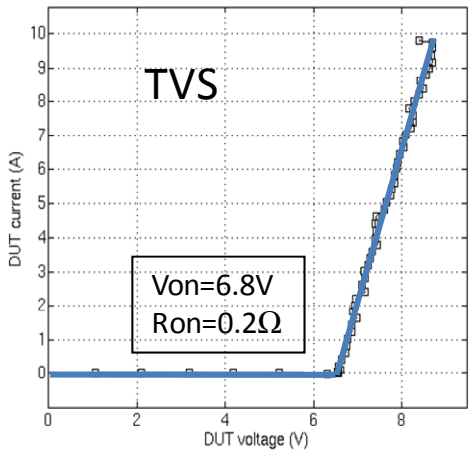

Figure 42: TVS I-V curve measured by 100 ns TLP.

Using the device parameters above, the current into the on-chip supply clamp and the ensuing clamp voltage may be calculated for any given on-board resistance R. Figure 43 shows Vc and Ic assuming no additional board resistance R exists. In that case the 'operating point' of the on-chip supply clamp during an IEC discharge (Vc, Ic) turns out to be outside the safe operating area (SOA) for the output domain on chip, which is defined by the design target for the clamp. The SOA is bounded by the maximum ESD current for which the clamp is designed, e.g. Imax = 4 A, and the maximum voltage on the core circuitry before oxide damage will occur, e.g. Vmax = 11 V (e.g. oxide break of thick oxide transistors).

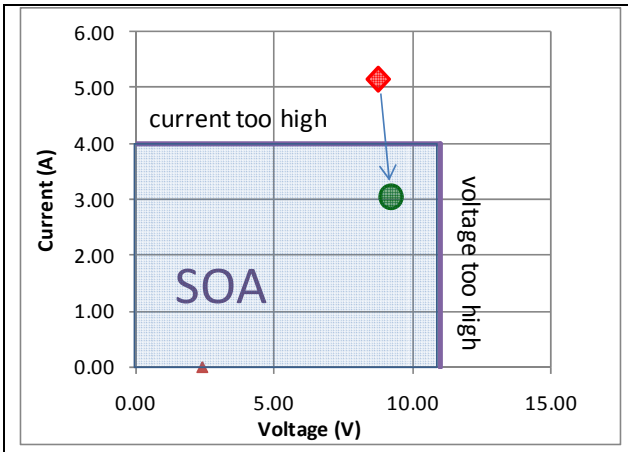

Figure 43: Increasing the series resistance on-board by 1 Ω moves the output 'operating point' (Vc, Ic) during an 8 kV IEC discharge into the SOA.

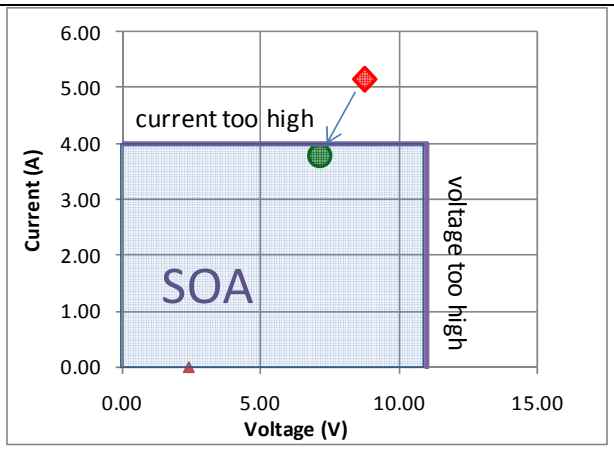

Figure 44: Choosing a different TVS with Von= 6 V and Ron=0.1 Ω moves the output 'operating point' (Vc, Ic) during an 8 kV IEC discharge into the SOA.

By increasing the on-board resistance R, the current into the clamp supply clamp may be reduced. However, in the case of an audio output, the required efficiency of the power stage usually does not allow increasing the output impedance. An alternative solution is to find another TVS which has either a lower on-voltage or a lower on-resistance. Figure 44 shows that by using a TVS with Von = 6 V and Ron = 0.1 Ω, the output (Vc, Ic) point moves into the SOA.

Note that the example shows a situation with limited options for co-design of the on-chip ESD protection and the on-board system level protection since the output impedance of the audio needs to be low-ohmic. The on-chip protection is low-ohmic as well by design. Therefore, in this situation the only solution is to find an on-board TVS with the proper Von and Ron. Von cannot be lower than the maximum operating voltage of the output (in normal operation) plus some margin. So, the proper solution is to find a TVS with a Von as low as possible and a sufficiently low Ron.

6.6.3 Design Verification Using VFTLP Data

In the previous example, the impact of the first peak in an IEC 61000-4-2 discharge has been neglected in a first approximation. In order to verify this approximation is valid for this design case, the response of the system to a fast initial pulse on the order of the first peak (about 0.7 ns rise time) needs to be tested. A 100 ns TLP tester is too slow for this purpose (rise time of about 10 ns), but a very-fast TLP system with a 2 ns pulse width / 500 ps or faster rise time would be well suited for this test.

6.6.4 A Generic Design Methodology for External Pins (SEED)

From the design example in Section 6.6.2 it is clear that the design of on-chip ESD protection and on-board system level protection cannot be performed separately, but co-design is needed to account for the interaction of the on-chip and on-board protection. The approach illustrated by the example may be generalized into a generic design methodology for each external pin. This concept is called System-Efficient ESD Design (SEED) and comprises the following generic steps (see Figure 45 for an illustration):

SEED Concept Details

1. **IC Supplier provides Transmission Line Pulse (TLP) data on the External Pin**
2. **Board Designer characterizes the Transient Voltage Pulse (TVP) to determine the Residual Pulse Stress (RPS) data (Voltage Vs. Time)**
3. **Board components are adjusted to balance the RPS data to the TLP data**

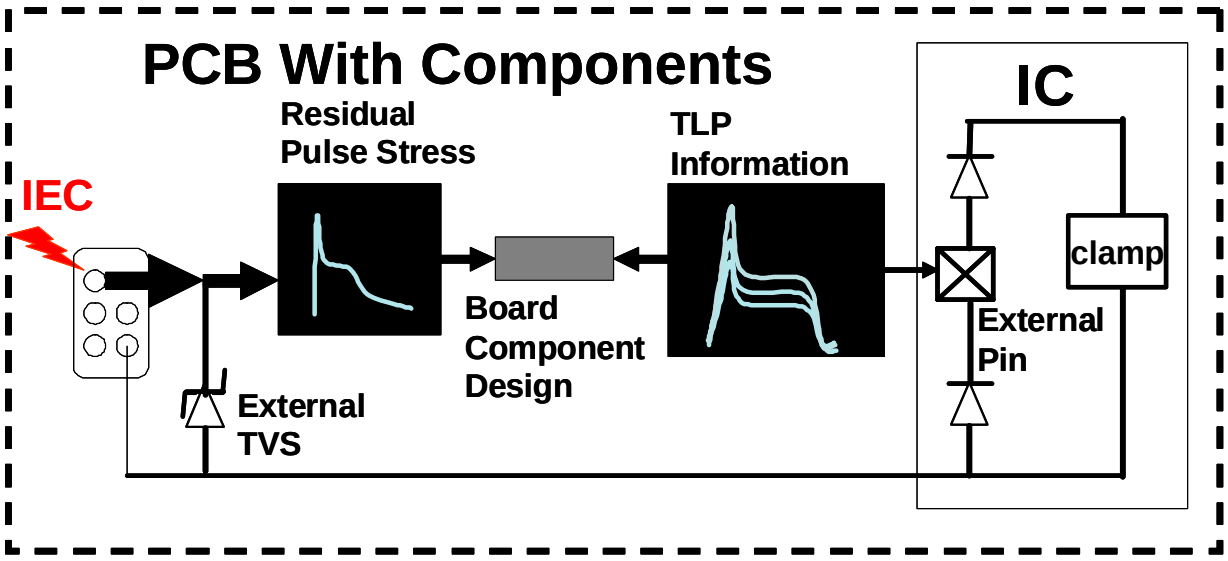

Figure 45: System-Efficient ESD Design (SEED) design methodology

1. For the domain which contains the external pin, design the on-chip protection such that the chip meets the usual 1 kV HBM target as well as a 250 V CDM target, without more than typical margin. This is to ensure that the current path through the on-chip protection circuitry is not lower-ohmic than needed to meet the HBM and CDM targets.
2. For any given pin to be protected, determine the SOA for the on-chip domain connected to the external pin, including both ESD protection and circuitry to be protected. Usually, the current capability of the supply clamp (in case of rail-based protection) will determine the current capability. The maximum ESD voltage will usually be determined by the breakdown voltage of the gate oxide of the core circuitry to be protected.
3. Select a TVS for the external pin with the lowest breakdown voltage which is above the maximum normal operating voltage of the pin plus some sensible margin, e.g. for a 5 V pin, the maximum operating voltage is 5.5 V, so the minimum TVS breakdown voltage should be 6 V.
4. Characterize the external pin under ESD conditions, e.g. by means of 100 ns TLP from pin to ground. Characterize the TVS in the same way.
5. Estimate the resistance and inductance in the path from TVS to chip pin. Determine the current distribution for an 8 kV contact discharge between TVS and external pin.
6. If the (Vc, Ic) operating point of the external pin is outside the SOA, try modifying any of the following parameters to move the operating point inside the SOA:

a. Increase series resistance or inductance of the path between TVS and pin. This is usually not a problem for inputs, but the maximum series resistance for outputs, especially high-power outputs, may be limited.
b. Find a TVS with a lower on-resistance. There will probably be a trade-off between lower on-resistance/capacitance and price.
c. Increase Von of the on-chip protection. This will not always be possible. Usually, the on-chip protection will use library cells which cannot easily be adapted for each new project.
d. Increase voltage level at which damage occurs in the circuit (e.g. by using thick oxide transistors).

6.7 Examples for System Level ESD Protection Design of Typical Interfaces / Ports

6.7.1 USB Designs and Trends

In the USB 2.0 system, the specifications [9] detail the overvoltage conditions as well as the nominal IO voltage range for VSSP of 0 V to VDDP of 3.3 V. An AC stress, which models the reflections at the other termination to support USB 1.1 backward compatibility, spans from -1 V to 4.6 V at 6 MHz with 4 to 20 ns rise and fall time. The short-circuit stress withstand condition requires the circuit to withstand 5.25 V or 0 V DC applied at the pad for 24 hours, which models a short-circuit of the IO pads to bus voltages. In addition, the USB 2.0 IO should support full-speed signaling at 12 Mb/s with a voltage level from 0 to 3.3 V and the high-speed signaling at 480 Mb/s between 0 V and 400 mV. These operational constraints lead to a limitation in the ESD protection concept, e.g. no diode to VDD is allowed. Also the acceptable capacitive load of the ESD protection is limited to a few pF.

In typical usage, cable discharge events are the most relevant and severe ESD threat for the USB 2.0 IO ports. In CDE events, the discharge occurs directly into the pin whereas the system level ESD stress according to IEC 61000-4-2 [6] is not applied directly on the USB pin but to the nearby chassis or connector shield. A typical CDE discharge shows a square-like current waveform overlaid by an initial peak (Figure 46). In an even more critical field event an additional (large) current peak can occur at the end of the pulse due to charge stored on the connecting device.

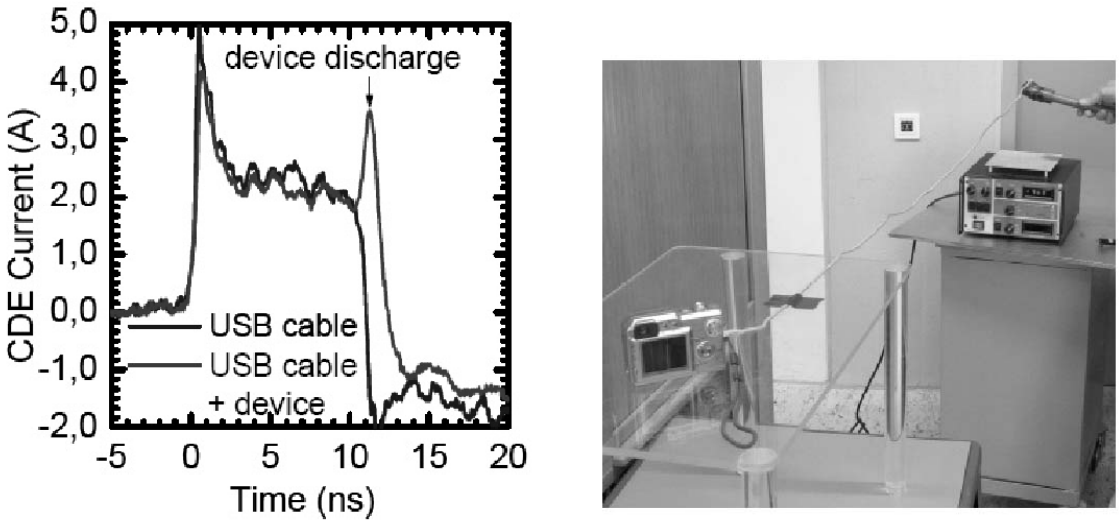

Figure 46: Cable discharge events for USB interfaces [10]

While on-chip only system level ESD protection is feasible for USB interfaces in special cases [11], a combined on-board and on-chip protection scheme is more flexible and better fulfills any EMC constraints. However, on-board and on-chip protection needs to be matched as described in Section 6.6.1, where most of the IEC current is drawn by the on-board shunt element (Figure 47). The relevant parameter is the voltage at fail Vt2, which is not necessarily correlated to the IC level HBM robustness that scales with the failure current parameter It2 (Figure 48). Only a high current IV characterization, acquired by TLP analysis, reveals the matching properties of the on-chip and on-board protection circuitry. In this case any additional serial resistance between the PCB clamping element and IC pin may not be allowed, due to the performance requirements of high speed USB.

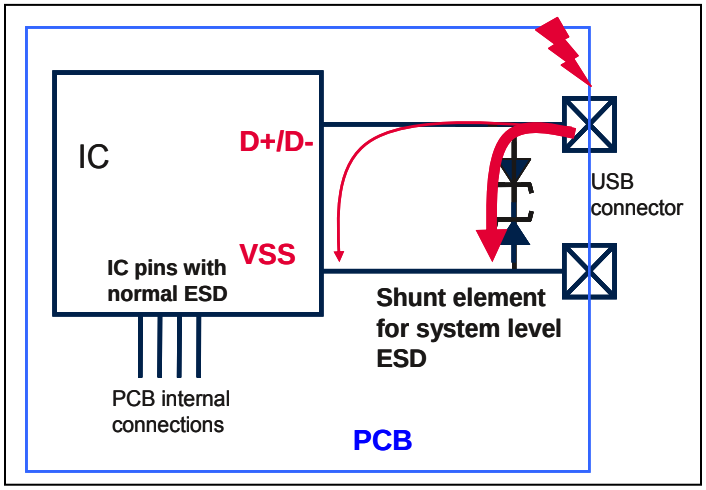

Figure 47: Current paths through on-board PCB and IO circuit

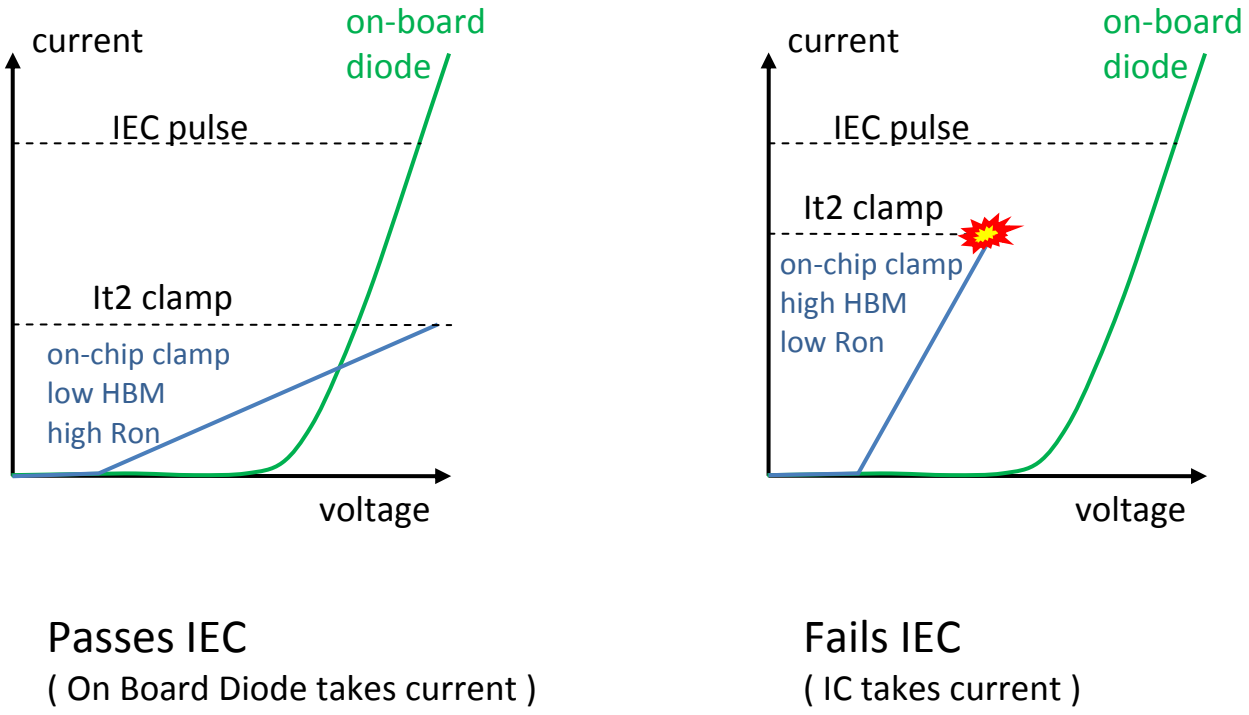

Figure 48: Matching (left) and mismatch (right) of on-board and on-chip protection IV characteristics. To avoid damage by a parallel current path through protected USB circuitry on the IC, the clamping voltage of the on-board diode Vclamp must be lower than the voltage Vt2 at which the IO (on-chip protection) is damaged.

It should also be noted that these harsh requirements are only applicable to USB connectors of the system (e.g. a mobile system). Inter-chip USB lines do not have this critical exposure.

6.7.2 CAN Interfaces

CAN interfaces have to survive high levels of system level ESD events. CAN ICs are tested with an IEC gun while mounted on small test boards [12]. The mandatory inductance of the common mode choke will damp any initial spike of the IEC pulse (Figure 49). The dominating failure mechanism is due to Joule heating resulting from the broad peak of the IEC waveform.

In the typical application, self-protection of the IC pins against IEC pulses is expected. In this case the placement of additional on-board ESD protection elements (ESD1/2/3) is very restricted, and it is highly recommended that SEED design concepts discussed in this section be used by the OEM and supplier. For example, due to overvoltage requirements of the CAN busses, no diode to VDD is allowed.

The required system ESD specific on-chip protection devices have to satisfy stress levels which exceed common IC ESD protection levels by more than an order of magnitude, Typically, more than 10 times the on-chip layout area, compared to a standard solution, is required to achieve the elevated ESD robustness level.

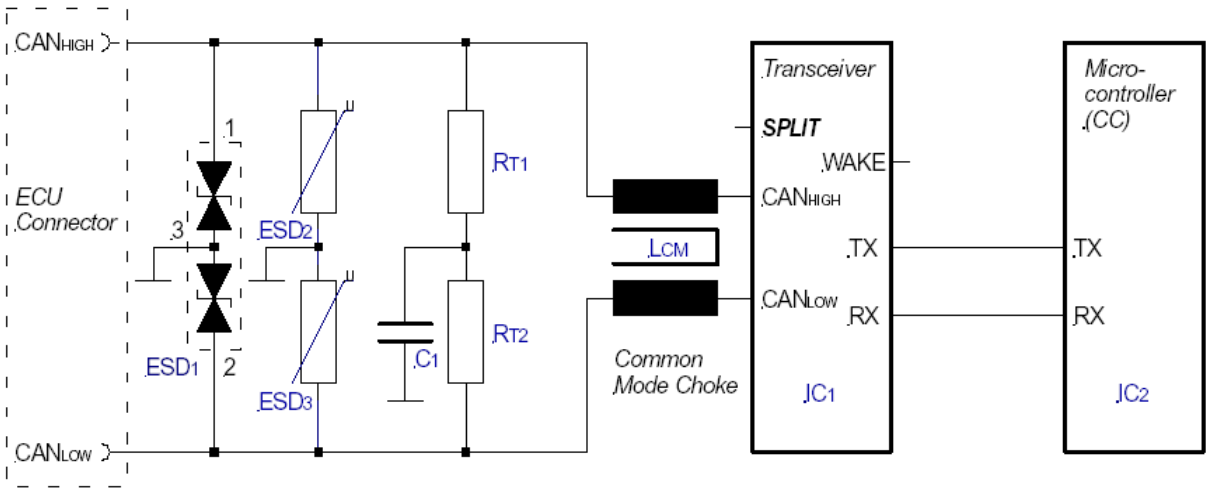

Figure 49: Typical system ESD protection of CANinterfaces [13]. Self-protection of the IC pins, CANlow and CANhigh, is assumed. ESD 1/2/3 can only be placed in exceptions.

6.7.3 Antenna Port Design

The antenna port, e.g. of a mobile device (Figure 50), is not only extremely critical to performance but it also needs to satisfy high system level ESD robustness requirements [14]:

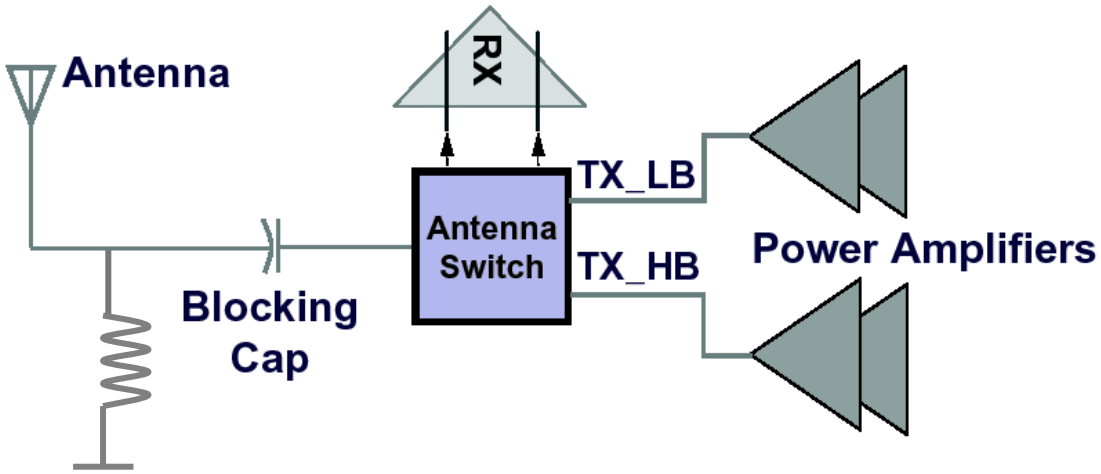

Figure 50: Typical antenna port configuration circuit

Antenna ports apply ac decoupling with a blocking cap. Therefore only limited energy can be transmitted to the chip. Most of the pulse energy is shunted to ground by the inductance of the matching network. However, in a certain frequency range, ESD pulse energy can be transmitted to the pin of the antenna switch. This could be sufficient to damage the sensitive antenna switch or even generate sufficient overvoltage at the receiver (RX) or transmitter (TX) pins to damage SAW filters connected to them. The residual voltage at these ports (RX, TX) is commonly required to be less than 150 V peak-to-peak.

The conventional system level ESD protection approach is to design a RLC network with a sufficiently wideband inductance from antenna port to GND which minimizes the transmission of energy from the IEC pulse into the protected antenna switch. Either an additional PCB clamping device or on-chip protection attached to the antenna IO can shunt the residual pulse efficiently. A cost efficient SEED protection design methodology will be achieved by an on-board protection component integrating filter network and ESD protection diodes.

6.8 Conclusion

6.8.1 Discussion of System Cost for Various Design Strategies

The following list of case histories illustrates that in the past there was no single best solution regarding system level protection design:

1. **DSP product - failed 8 kV air discharge in a system**: The customer insisted on a system level fix, which caused a production delay of 2 months. The engineering effort spent was 3 man-months and the fix involved adding a new component to the board.
2. **DSP product - failed 15 kV contact discharge**: Multiple customers required a fix, which caused a production delay of 3 months. The engineering effort spent was 4 man-months and the fix involved adding a new component to the board. The issue caused a business loss of $1.5 M.
3. **On-chip system level protection** was developed in a 0.13 µm technology, which involved about 4000 μm^2 of additional die area to protect one pin. The total capacitance loading including the metal was 400 fF.
4. **PMU product - failed system level test:** During a system level test the 2 kV HBM protection on the die was destroyed by either CDE or EOS. The solution involved adding TVS protection on-board for some customers and / or improved control for other customers.
5. **Mixed signal product - hot plugging failure:** A hot plugging (powered system connected to powered cable) issue was solved by using shorter cables. In addition the PCB was re-designed to improve system level ESD performance.
6. **Wireless communication product - system failed when using cheap on-board TVS:** The customer discovered that the board worked fine with expensive on-board TVS parts, but with less expensive diodes, system level fails occurred. Reason for the discrepancy was investigated, which involved TLP testing of TVS parts and product pins in order to establish the maximum current flowing into the IC for a given TVS. Based on this data, it was possible to advise the customer to use cheaper diodes on certain pins, while still requiring the expensive TVS for a single pin, which saved 95% of extra cost. The engineering effort was about 2 weeks.
7. **Wireless communication product - On-chip system level protection for FM pin**: On-chip protection for a FM TX/RX antenna pin was developed to allow the customer to save on external components. During system development IEC testing, failures occurred at 7 kV contact discharge. Analysis showed that the TX output buffer was destroyed since it took more current during a system level discharge than originally anticipated. After

redesign of the metal / via connectivity to the on-chip protection, the issue disappeared. The engineering effort was 4 man-months.

8. **Computer type product:** This product had 12 discrete on-board protection components to protect the display driver IC on a motherboard. The driver IC had only moderate on-chip protection, and protection components were used for assembly purposes to limit ESD stress from the charged display. The driver IC was stressed, without protection components, with the same discharge waveform that the charged display was able to produce during assembly phase. The calculated stress level was estimated to be below the driver components withstand level. There were no failures in the final tests, and 11 on-board protection components were removed from the design. One protection component was still needed to prevent system resets during IEC 61000-4-2 validation. The engineering effort was ½ man-months.

Changing to System-Efficient ESD Design, a co-design approach including both on-board and on-chip protection, allows a systematic optimization of system level ESD protection. When deciding about an optimum solution, various aspects have to be considered:

1. **Cost**
   The obvious advantage of using on-chip protection is to reduce the number of individual on-board TVS, of which there may be many dozens on a single PCB. The price of these parts various widely, from less than $0.01 to >$0.3 per piece. In addition, the external protection requires extra cost for assembly, area on the board, etc.

   Although the size of the on-chip protection is independent of the technology, the price of the chip nevertheless goes down with each new technology. So, for the OEM there is an apparent price drop of the product with each new technology. The price of external parts on the board, on the other hand, remains at the same level, independent of the IC technology.

   When looking only at manufacturing cost, the use of additional die area will always be preferred than using external protection components. However, R&D cost due to IC respins might be significantly higher. Also these respins can lead to a major delay in time-to-market of the system.

2. **RF-Disturbance**
   Particularly in RF applications, it is of paramount importance to contain (electromagnetic) disturbances as much as possible at their point of origin, i.e. as close as possible to the gun. By placing the protection on-chip, however, the full ESD current has to enter the IC by default. This increases the risk of internal RF disturbances significantly, possibly to the point where the system level performances can no longer be met. Furthermore, on-chip shielding is very costly in terms of area.

3. **Flexibility**
   On-board protection may be a lot more flexible than on-chip protection. The cost involved in changing a particular protection design on-chip (e.g. mask costs) may be prohibitive. On-board components in combination with board parasitics including track resistance and inductance may be used to build effective filters which block part of the ESD current. Such filters can be relatively easily optimized by re-routing tracks, changing track length, etc.

4. **Debugging**
   Failure analysis at the board level can be done with regular lab tools. On-chip failure analysis

is far more labor/cost intensive. Also, board level modifications are easier to implement, allowing new ideas to be tried out.

There is a major difference in the ESD protection design between high value & low volume and low value & high volume products. High value products can have all needed protection components on a layout, and protection methods are mainly limited by the available space and signal integrity targets. Low value products have the same limitations in space and signal quality, but have also major limitations on the design and material costs. For example, one on-board protection component purchase and assembly can cost 2 cents/piece. When 1 million low value products are made and each product requires 10 devices the protection expenses are >$200k. This represents a significant percent of the product sales price. With a proper mechanical design, layout optimization and good on-chip protection, the number of on-board protection components can be limited and the product can still pass the IEC 8 kV target.

6.8.2 Effort and Benefit of System-Efficient ESD Design (SEED)

The co-design methodology SEED requires a common approach for the protection design, with collaboration from both the IC and system designer. System designers have to specify which IOs require higher withstand levels in a system and then request IC operational parameters with similar I-V curve based specifications. These specifications are used for ESD validation by the IC suppliers. The system designer can use this data with calculation and simulation tools to optimize the on-board design to fulfill the final system requirements. These requirements can be IEC based or some other selected stress events. The primary benefit is that SEED enables a systematic step by step approach for ESD robust system design. SEED reduces costly trial and error rounds and decreases the wrestling between system and IC suppliers over on-chip protection requirements.

6.8.3 Next Steps Required by IC Suppliers, PCB ESD Diode Suppliers, Board and System Designers

The presented extraction and simulation approach enables a systematic development of an optimum and cost-efficient system level ESD protection. To apply this SEED method to regular product design requires certain preparation steps in the industry.

1. Suppliers of ICs and on-board ESD protection ESD elements need to align on a common standard for characterizing the on-board protection elements and the external pins of the protected ICs. A highly accurate TLP analysis up to 30 A is recommended for characterization of on-board protection elements. TLP IV characteristics of external pins have to be provided by the IC suppliers. Also, the transient turn-on behaviour of the on-board protection elements and IO circuitry have to be determined over a wider range of currents (mA to several 10 A), which may require very fast TLP (VFTLP) testing. The extracted parameters and models have to be provided in a standardized way, which allows the system manufacturer to use this input from various suppliers of his board components.

2. The system manufacturer should adjust the requirements catalogue for the IC and the protection devices accordingly. The reliance on HBM robustness of the IC pins must be abandoned and must be replaced by the request for detailed TLP characterization of the system relevant pins of the IC. The selection of on-board protection devices is then based on

the quality of the IC and on-board ESD protection element IV characteristics and the transient behavior of the protection elements up to 30 A (for an 8 kV contact level IEC ESD event).

3. Finally, the board designer must have the capability to use these data in the simulation environment and to perform IEC pulse simulations.

By using such a procedure, the risk and the required effort due to any late changes in the system design can be minimized while the full performance of the semiconductor devices can be exploited.

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Chapter 7: Summary, Conclusions and Outlook

7.0 Summary

In this paper, we have attempted to present the first comprehensive analysis of system level ESD issues including ESD related system failures and design for system robustness. The discussion throughout shows that designing for system level ESD involves bridging the misconceptions between system designers (OEMs) and semiconductor component (IC) providers. We have drawn on the expertise of both OEMs and IC designers to address respective misconceptions and propose a system level ESD analysis and design methodology that increases system level ESD robustness while simultaneously reducing IC-level ESD design difficulty.

We have shown a clear distinction between physical failures and soft failures. Soft failures appear exclusively during powered conditions and are deferred to Part II of White Paper 3. Physical failures, with few exceptions, are related to external pins that are directly exposed to ESD stress, as proven by analysis of field returns and qualification test results. We have demonstrated that both design and robustness evaluations of these external pins have to follow a different methodology than standard ESD qualification. This is especially important since, contrary to the prevalent assumption in the industry, HBM and CDM testing do not provide sufficient information for system robust design.

This paper builds a framework for successful system level ESD protection using the following key concepts:

- ESD test specification requirements of system providers must be clearly understood as a separate domain from IC level ESD specifications. IC level ESD specifications should not be used as a basis for system level requirements.
- Understanding of the ESD failure and upset mechanisms is critical to recognizing their relevance for robust protection design and for correlating them to the IC specifications.
- Responsibility must be shared between system designers and IC providers for proper system level ESD protection.

From these concepts, we have introduced a new methodology described as “System-Efficient ESD Design” (SEED) that promotes a common OEM/IC provider understanding of correct system level ESD needs. The key objective has been the development of a framework for communicating IC / system level circuit information so that best practice ESD protection and controls can be co-developed and properly shared.

7.1 Conclusions

From this extensive collaboration between the IC providers and the system builders, this paper has been able to establish some key conclusions in Part I of the white paper. Our intention has been to remove misconceptions about system ESD design and requirements and at the same time, to present a fully comprehensive view of system level ESD protection design. We can conclude the following:

- Component ESD requirements are critical for IC production and handling, but requiring them to be much higher than the necessary safe levels can have a direct impact on circuit speed and consequently on system performance itself.

- As previously established in White Paper 1 and White Paper 2, and now more importantly confirmed in the present White Paper 3, artificially high HBM and CDM requirement for individual ICs either do not correlate to a robust system ESD performance or do not necessarily add value when designing for better system protection.

- By the same token, components/ICs just passing a certain level of any stress test (such as IEC, HMM, etc. as qualification goals) do not guarantee robustness of the complete system. More work is needed in this area to establish the true nature of system ESD events.

- A good design strategy for system protection requires a clear definition and understanding of *external* versus *internal* IC pins and those conditions under which stress to external pins can couple to internal pins. Only after establishing these distinctions can system design methodology and the process for it be properly and efficiently communicated and practiced.

- Placing large area protection clamps directly on-chip for an IC external pin may not ensure robust system ESD, and the approach will have many disadvantages in implementation for both the IC supplier and the system designer. A better strategy relies on external clamps as much as possible and also involves an understanding of the interaction with the IC pins' internal clamps.

- In order to offer a better and more interactive approach, the System-Efficient ESD Design (SEED) strategy has been introduced. This method uses a TLP based characterization of on-board protection diodes and on-chip protection circuits to co-design on-chip and on-board protection circuits.

- SEED is proposed as a superior design methodology to optimize system cost vs. performance and to reduce overall R&D effort.

- By following the SEED approach, some new efficient ESD systems have already been demonstrated.

7.2 Outlook

The overall system ESD protection can be more complicated when considering both hard and soft failures. The so called soft failures may involve complex EMC/EMI effects and also some Transient Latchup (TLU) phenomenon. The latter TLU effect could come from the technology development along with the system application, and thus requires thorough understanding. In Part II of this White Paper, the Industry Council will address a comprehensive system level ESD design strategy in more detail, using the information from Part I. This information will be used to establish recommendations for IC and system level manufacturers regarding proper protection / controls and best practice ESD tests which can be used to properly assess ESD and related EMI

performance of system level tests. This is intended to better define the IC manufacturer / system level OEM ESD relationship and responsibilities.

Revision History

Revision	Changes	Date of Release
1.0	Initial Release	Oct 2010